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A New ATLAS Muon CSC Readout System with System on Chip Technology on ATCA Platform

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The ATLAS muon Cathode Strip Chamber (CSC) backend readout system has been upgraded during the LHC 2013-2015
shutdown to be able to handle the higher Level-1 trigger rate of 100 kHz and the higher occupancy at Run 2
luminosity. The readout design is based on the Reconfiguration Cluster Element (RCE) concept for high bandwidth
generic DAQ implemented on the ATCA platform. The RCE design is based on the new System on Chip XILINX ZYNQ series
with a processor-centric architecture with ARM processor embedded in FPGA fabric and high speed I/O resources
together with auxiliary memories to form a versatile DAQ building block that can host applications tapping into
both software and firmware resources. The Cluster on Board (COB) ATCA carrier hosts RCE mezzanines and an embedded
Fulcrum network switch to form an online DAQ processing cluster. More compact firmware solutions on the ZYNQ for
G-link, S-link and TTC allowed the full system of 320 G-links from the 32 chambers to be processed by 6 COBs
in one ATCA shelf through software waveform feature extraction to output 32 S-links. The full system was installed
in Sep/2014. We will present the RCE/COB design concept, the firmware and software processing architecture, and
the experience from the intense commissioning towards LHC Run 2.

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