A New ATLAS Muon CSC Readout System with System on Chip Technology on ATCA Platform

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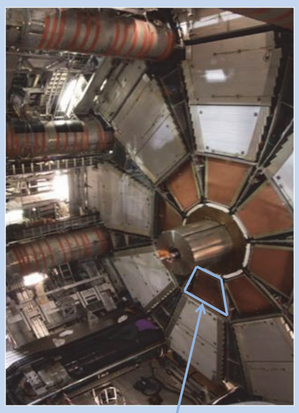
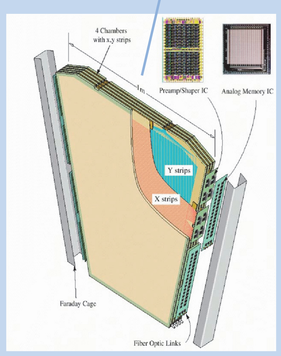
ATLAS Cathode Strip Chambers (CSC)



- Multi-wire proportional chambers designed to detect muons in the high pseudorapidity region:
  - $2.0 < |\eta| < 2.7$
- Consists of 2 end-caps with 16 chambers each
- Each chamber has:
  - 4 precision (η) layers with 768 strips
  - 4 transverse (φ) layers with 192 strips

On Detector Electronics



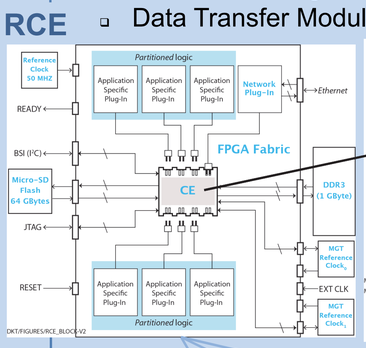
- Front-End-Electronics consists of 5 readout boards (4 precision, 1 transverse) per chamber
  - 192 channels per board
- Readout board preamplifiers and shapers convert wire signals to bipolar pulses with 140 ns shaping time
- Pulses are sampled every 50 ns and stored on a 144 cell analog memory Storage Capacitor Array (SCA)
- Samples are digitized to 12 bits of data
- Data are transferred to off-detector readout drivers (RODs) over high speed fiber-optic G-Links

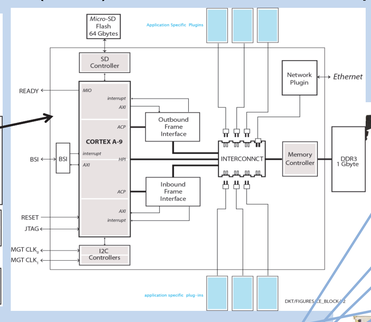
The Run 1 ROD was robust and functional, but dead-time limited to an L1 rate of 75 kHz

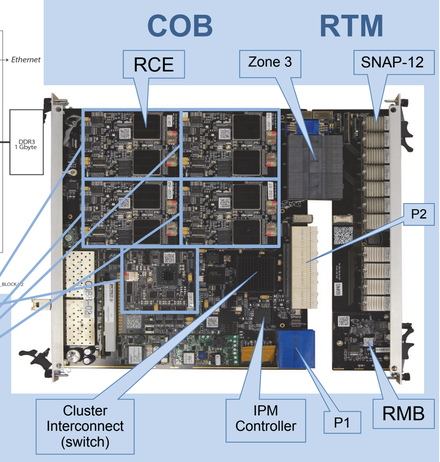
ATCA-Based Generic Data Acquisition System

- A modular data acquisition architecture has been developed as a result of the US DoE's Detector R&D program at SLAC: the Reconfigurable Cluster Element (RCE)
  - Based on System-On-Chip (SoC) technology (Xilinx ZYNQ)
  - Provides a processing component that includes both firmware and software
  - Has large FPGA fabric and dual core ARM processor
  - Choice of OS: RTEMS, LINUX or bare metal
- Host platform is Advanced Telecommunications Computing Architecture (ATCA)
- Cluster-On-Board (COB): carrier board developed to hold 8 + 1 RCEs
  - Cluster Interconnect: on-board 24-port 10GbE low latency L2 switch (Fulcrum)
  - High density zone 3 connector provides 96 channel connectivity with a choice of Rear Transition Modules (RTM) with Rear Mezzanine Board (RMB, for TTC I/O)
- RCEs implemented in two forms:
  - Data Processing Module (DPM): 2 RCEs for application's use
  - Data Transfer Module (DTM): 1 RCE shared with application

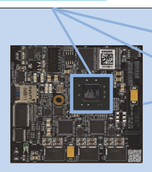
RCE



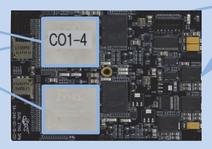




DTM



DPM

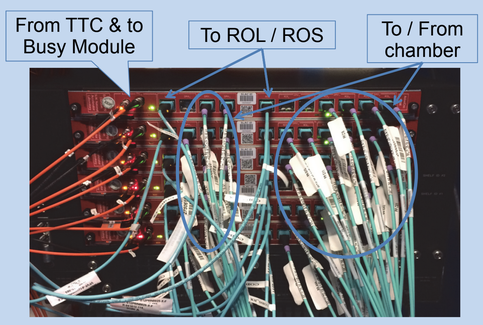


Application of RCEs to CSC

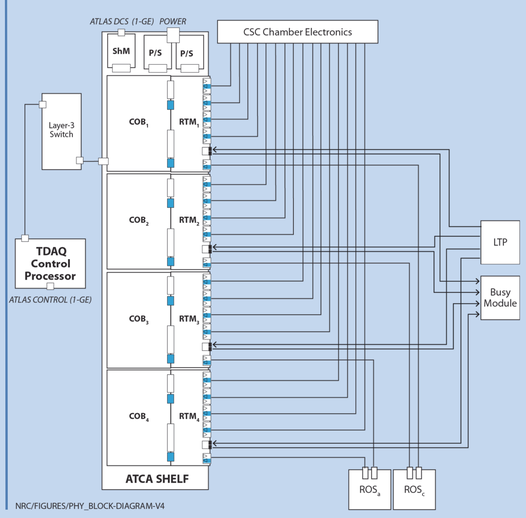
- Each slot of a standard 6-slot ATCA Shelf (i.e., crate) contains:
  - COB: Hosts RCEs that provide Feature EXtraction (FEX) and data formatting
  - RTM: Provides physical interface to chambers and the central TDAQ system

Front View (COBs)

From / to switch & Control Processor



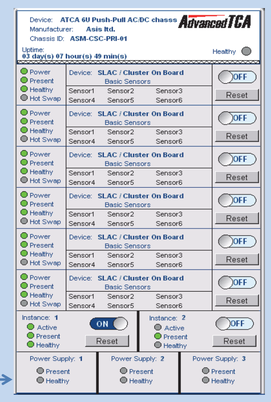
Rear View (RTMs)



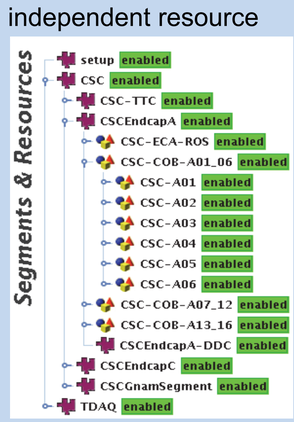
- DPM RCEs:
  - Handle a single chamber
  - Process 4 or more Front-End data samples into event fragments
- DTM RCE:
  - TTC emulator available for testing
- Traditional hardware solutions are implemented in firmware of the SoC, causing smaller footprint and lower power consumption
  - TTC handling is implemented in DTM & DPM firmware
  - S-link is implemented in firmware
  - G-link ASIC (HDMP) is implemented in firmware

Integration with ATLAS TDAQ

- Control Processor PC
  - Interacts with the TDAQ infrastructure
  - Configures the RCE via network, in parallel
- TTC Restart capability
- On-the-fly diagnosis & recovery of issues appearing during ATLAS runs is being implemented at chamber granularity
- GNAM online monitoring
- ATCA shelf is controlled and monitored via DCS:

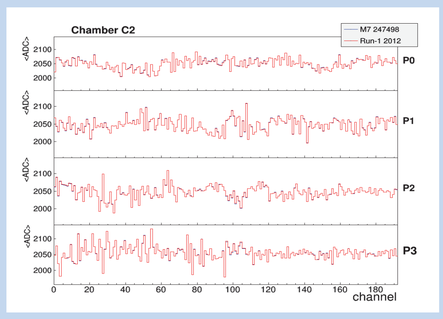


- 1 process per chamber for control / configuration
- Each chamber is a true independent resource

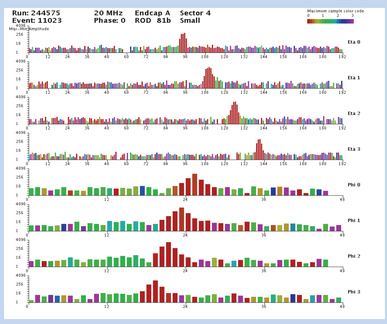


Data Quality

Pedestal measurements performed with the new system are compatible with Run-1 measurements



Cosmic tracks first seen in November 2014



Performance

- Full readout chain can run at 100 kHz with low dead time (<1%)
- High performance FEX code
- Fast configuration due to the parallel operation on each RCE
- Increased bandwidth to ROSes by doubling the number of S-links compared to Run-1

- System is ready to handle the higher Level-1 trigger rate of 100 kHz and the higher occupancy at Run 2 luminosities