

A New ATLAS Muon CSC Readout System with System on Chip Technology on ATCA Platform



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UCIRVINE

RESET -

To / From

SLAC NATIONAL ACCELERATOR LABORATORY **ATLAS Cathode Strip Chambers (CSC)**



Multi-wire proportional chambers designed to detect muons in the high pseudorapidity region: 2.0 < |η| < 2.7

- Consists of 2 end-caps with 16 chambers each Each chamber has:
- 4 precision (η) layers with 768 strips
- 4 transverse (φ) layers with 192 strips

On Detector Electronics Front-End-Electronics consists of 5 readout boards (4 precision, 1 transverse) per chamber 192 channels per board

Readout board preamplifiers and shapers convert wire

From TTC & to

signals to bipolar pulses with 140 ns shaping time

BROOKHAVEN NATIONAL LABORATORY **ATCA-Based Generic Data Acquisition System**

- A modular data acquisition architecture has been developed as a result of the US DoE's Detector R&D program at SLAC: the Reconfigurable Cluster Element (RCE)
- Based on System-On-Chip (SoC) technology (Xilinx ZYNQ)
- Provides a processing component that includes both firmware and software
- Has large FPGA fabric and dual core ARM processor
- Choice of OS: RTEMS, LINUX or bare metal
- Host platform is Advanced Telecommunications Computing Architecture (ATCA)
- Cluster-On-Board (COB): carrier board developed to hold 8 + 1 RCEs
 - Cluster Interconnect: on-board 24-port 10GbE low latency L2 switch (Fulcrum)
- High density zone 3 connector provides 96 channel connectivity with a choice of Rear Transition Modules (RTM) with Rear Mezzanine Board (RMB, for TTC I/O)
- RCEs implemented in two forms:
- Data Processing Module (DPM): 2 RCEs for application's use
- Data Transfer Module (DTM): 1 RCE shared with application RCE





Pulses are sampled every 50 ns and stored on a 144 cell analog memory Storage Capacitor Array (SCA) Samples are digitized to 12 bits of data Data are transferred to off-detector readout drivers (RODs) over high speed fiber-optic G-Links

The Run 1 ROD was robust and functional, but dead-time limited to an L1 rate of 75 kHz

Application of RCEs to CSC

Each slot of a standard 6-slot ATCA Shelf (i.e., crate) contains: COB: Hosts RCEs that provide Feature EXtraction (FEX) and data formatting RTM: Provides physical interface to chambers and the central TDAQ system

From / to switch & Control Processor



Front View (COBs)

ShM P/S P/S

CSC Chamber Electronics



Rear View (RTMs)

DPM RCEs:

- Handle a single chamber
- Process 4 or more Front-End data

- RMB IPM Cluster DTM DPM P1 Controller Interconnect (switch) Integration with ATLAS TDAQ 1 process per chamber Control Processor PC Interacts with the TDAQ Each chamber is a true
 - infrastructure
 - Configures the RCE via network, in parallel
 - TTC Restart capability
- On-the-fly diagnosis & recover of issues appearing during ATLAS runs is being implemented at chamber granularity
- GNAM online monitoring
- ATCA shelf is controlled and monitored via DCS:

	Device: A Manufactur Chassis ID:	er: Asi	ush-Pull AC: is Itd. SC-PRI-01	DC chasss	Advan	cedTCA	
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	Power Present	Device: SLAC / Cluster On Board Basic Sensors			OFF		
	● Healthy ● Hot Swap	Sensor1 Sensor4	Sensor2 Sensor5	Sensor Sensor	-	Reset	
/	Power Present	Device: SLAC / Cluster On Board Basic Sensors				OFF	
	● Healthy ● Hot Swap	Sensor1 Sensor4	Sensor2 Sensor5	Sensor Sensor		Reset	
	Power Present	Device: SLAC / Cluster On Board Basic Sensors			OFF		
	● Healthy ● Hot Swap	Sensor1 Sensor4	Sensor2 Sensor5	Sensor Sensor	-	Reset	
	Power Present	Device: SLAC / Cluster On Board Basic Sensors			OFF		
	Healthy	Sensor1 Sensor4	Sensor2 Sensor5	Sensor Sensor		Reset	
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for control / configuration independent resource setup enabled CSC-ECA-ROS enab CSC-COB-A01_06 enable 🐏 CSC-A01 enabl - 🐏 CSC-A02 enable

> 😪 CSC-A03 enable 😪 🐏 CSC-A04 enable

😪 CSC-A05 enable

🐏 CSC-A06 enable

🐏 CSC-COB-A13_16 enable

CSCEndcapC enabled

📲 TDAQ enabled

📲 CSCGnamSegment enabled

CSC-COB-A07_12 enable

CSCEndcapA-DDC enable

Data Quality

Pedestal measurements performed

Cosmic tracks first seen in

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samples into event fragments DTM RCE:

TTC emulator available for testing Traditional hardware solutions are implemented in firmware of the SoC, causing smaller footprint and lower power consumption

- TTC handling is implemented in DTM & DPM firmware
- S-link is implemented in firmware
- G-link ASIC (HDMP) is implemented in firmware





High performance FEX code

- Fast configuration due to the parallel operation on each RCE
- Increased bandwidth to ROSes by doubling the number of S-links compared to Run-1
- System is ready to handle the higher Level-1 trigger rate of 100 kHz and the higher occupancy at Run 2 luminosities

with the new system are compatible with Run-1 measurements



Performance

FDFP, 24 – 30 May, 2015



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