Design, Fabrication and Characterization of AC Coupled p-on-n Si Strip Detectors furnished with multi-guard-rings

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Frontier Detector for Frontier Physics, 13th Pisa meeting, La Biodola, Isola d'Elba (Italy), 24th - 30th May 2015
**Outline**

- **Introduction**
  - Silicon (Si) Detectors in HEP experiments
  - DU contribution in the development of Si-mini-strip detectors for CMS Preshower

- **Challenges for future Si tracking system**

- **DU Interest for future Si-tracking system**
  - Design: Device Simulation
  - Fabrication: Planar Process
  - Characterization: Setup & Results

- **Summary**

- **Future Agenda**
Silicon Detectors in HEP experiments

Si as a tracking detectors are being used for particle detection and precise position measurement of charged particles in HEP experiments.

Historical Perspective

Present Large Si Tracking System

CMS Tracker
Pixel (1m²)
Strip (200m²)
CMS Preshower Detector (Delhi University Contribution)

Specifications of Si Sensor
- Si sensor: 63×63 mm²
- 32 strips, 1.9 mm pitch
- 4300 modules, 18 m² of silicon
- Si sensors and front-end hybrids glued to a ceramics support
- Everything supported by an Al tile

- Successfully developed Si strip sensors, for the first time in India.
- Delhi University (DU) performed R&D and participated in all the aspects of Si sensor development with BARC, Mumbai & BEL, Bangalore.
- 1000 Si sensors were fabricated and tested and installed in the Preshower Detector of ECAL for CMS Experiment.

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Challenges for future Si-Tracking Detectors

Future HEP experiments (Upgrade of CMS detector at LHC & Proposed International Linear Collider)

CMS Tracker Upgrade
Operation at High Luminosity ($10^{35}\text{cm}^{-2}\text{s}^{-1}$)
Higher Fluence ($10^{16}\text{n}_{\text{eq}}/\text{cm}^2$)

Radiation Damage in Si Tracking Detector
Leads to the deterioration of the electrical properties of Si sensors

Surface Damage
Creates charged states in SiO$_2$
Contributes to the surface charge density ($Q_F$)
$p^+\text{-}n^-$ device $\rightarrow$ Degradation of breakdown voltage ($V_{BD}$)

Bulk Damage
Creation of donor and acceptor traps with energy levels inside the band-gap
- Trapping of charge carriers

Affect on sensor properties
Decrease in the charge collection efficiency
Increase in Leakage Current

Need Radiation Hard Si Sensors with Finer Granularity

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Surface Damage

- Creates charged states in SiO$_2$
- Contributes to the surface charge density ($Q_F$)

- $p^+\text{-}n^-$ device $\rightarrow$ Degradation of breakdown voltage ($V_{BD}$)

- $n^+\text{-}p^-$ device $\rightarrow$ Degradation of position resolution
  (e$^-$ accumulation layers between $n^+$ strips)

- Affect on sensor properties
  - Inter-strip capacitance (noise between the strips)
  - Inter-strip resistance (strip isolation)

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Fluence vs Radius

- Pixel
- Strip tracker

- CMS Tracker Upgrade
  Operation at High Luminosity ($10^{35}\text{cm}^{-2}\text{s}^{-1}$)
  Higher Fluence ($10^{16}\text{n}_{\text{eq}}/\text{cm}^2$)

- CMS
- Tracker
- Upgrade
- Operation
- at
- High
- Luminosity
- ($10^{35}\text{cm}^{-2}\text{s}^{-1}$)
- Higher
- Fluence
- ($10^{16}\text{n}_{\text{eq}}/\text{cm}^2$)

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### Design Challenges for future Si tracking system

#### Si Strip Detectors installed in CMS Preshower

1. Si-Mini-Strip Sensors
2. Large Pitch (1.9mm)
3. DC Coupled Si Strip Detectors
   - Readout directly coupled to implant

#### Future Si tracking system

1. Si-Micro-Strip Sensors
2. Small Pitch (55μm)
3. AC Coupled Si Strip Detectors
   - Capacitive Coupling between implant and readout

#### Comparison

<table>
<thead>
<tr>
<th>Si Strip Detectors</th>
<th>Future Si tracking system</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Si-Mini-Strip Sensors</td>
<td>1) Si-Micro-Strip Sensors</td>
</tr>
<tr>
<td>2) Large Pitch (1.9mm)</td>
<td>2) Small Pitch (55μm)</td>
</tr>
<tr>
<td>3) DC Coupled Si Strip Detectors</td>
<td>3) AC Coupled Si Strip Detectors</td>
</tr>
<tr>
<td>- Readout directly coupled to implant</td>
<td>- Capacitive Coupling between implant and readout</td>
</tr>
</tbody>
</table>

- Large noise and lower charge collection efficiency
- Less noise and higher charge collection efficiency
- 4) Direct biasing
- 4) Biasing through poly Si resistors

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To understand performance of Si sensors at higher fluences, extensive simulations and measurements of Silicon Sensors are required.

Delhi University is involved in the development of AC coupled Silicon Micro-Strip Detector (p-on-n) equipped with multi-guard-rings.

Collaboration with Dr. Marcel Demarteau – Fermilab.

Participation in following three different activities:

- **Design Optimization**
  - Device Simulation
  - TCAD-Silvaco

- **Fabrication**
  - Close coordination with Foundry – Bharat Electronic Limited (BEL), Bangalore, INDIA

- **Characterization**
  - Established characterization set-ups (IV/CV & TCT)
  - Involved in the measurements of both static & dynamic properties of Si Strip Detectors.
Device Simulation (TCAD Silvaco)

Flow Chart for Simulation

- **DevEdit** (Structure & Mesh Editor)
  - Define
    - Region
    - Material
    - Doping
    - Contacts
    - Electrode
  - Generate Structure File “.str”
    - Provide Electric Field, Potential

- **Generate Physics File “.log”**
  - Provide Current, Capacitance, Voltages

- **ATLAS (Physics Model)**
  - Include
    - Method
    - Model
    - Interface
    - Solve

- Solves current density equations, continuity equation along with poisson’s equation using given boundary conditions
- Surface/Volume is subdivided in small discrete regions called “Meshing”
- Good mesh leads to better convergence
### Design Optimization - Double Sided Si Micro-Strip Detectors (p⁺-n⁻-n⁺)

#### Phase-I (p⁺-n⁻)
- To achieve good charge collection efficiency (CCE) after bulk damage, sensors should be over depleted.
- Ensure the operation of Si sensors at high voltage.
- Limited by the breakdown phenomena.
- In p⁺-n⁻ Si sensors, breakdown is due to:
  - Electric field enhancement at edges & corners of pn junction.
  - Presence of $Q_F$.
- To improve the breakdown performance with low leakage current, performed design optimization of p⁺-n⁻ (front side).
- Incorporated guard-ring structures.

#### Phase-II (n⁺-n⁻)
- Generation of $e^-$ accumulation layer on backside (n⁺-n⁻).
- Shortening between n⁺ strips.
- Degradation of position resolution in n⁺-n⁻.
- Need isolation.
- Isolation Methods - Two types:
  - Uniform doping.
  - Heavily doped region.
  - p-spray.
  - p-stop.

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**Design Optimization**

### Phase-I (p⁺-n⁻)

- Eight different layout
- Adding p⁺ intra-guards
- Adding n⁺ intra-guards
- Adding p⁺ intra-guards only
- Adding n⁺ intra-guards only
- Adding left sided MO
- Adding right sided MO
- Adding both sided MO

### Phase-II (n⁺-n⁻)

- Optimization is performed [2] for
  - implant dose profile of the p-spray
  - implant width of p-stop

**Seen effect on interstrip capacitance**

Optimized various design parameters[1]-

- Guard-ring spacing
- Guard ring width
- Incorporation of additional intra-guard rings of p⁺ and n⁺ types
- Incorporation of metal-overhang
- Doping concentration
- Junction depth
- Fixed positive oxide charges

**Output**-Optimized design parameters are delivered to BEL for fabrication


Detector Layout & Specifications (Phase-I)

- Si strip detectors are fabricated on 4" wafer with eight layer mask process using the planar fabrication technology at BEL, India
- Float-Zone n-bulk wafer with resistivity of 3-5 kohm-cm, thickness of 300µm are used for fabrication

Detector Dimensions-
Length: 6 cm
Width: 3.4 cm
Number of strips: 512
Strip width: 30 µm
Strip Pitch: 55 µm

Detector Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Depletion voltage</td>
<td>40 - 150V</td>
</tr>
<tr>
<td>Biasing scheme</td>
<td>poly-resistors on both ends</td>
</tr>
<tr>
<td>Poly resistor values</td>
<td>0.8 ± 0.2 MΩ</td>
</tr>
<tr>
<td>SiO₂ Thickness</td>
<td>250nm</td>
</tr>
<tr>
<td>Metal strips</td>
<td>Al coupled over the p-implant</td>
</tr>
<tr>
<td>Al strip width</td>
<td>3 - 4 mm metal overhang on each side &gt; 1 mm</td>
</tr>
<tr>
<td>Al strip thickness</td>
<td>~ 144 pF ± 10%</td>
</tr>
<tr>
<td>Coupling capacitance per strip</td>
<td>&gt; 350V</td>
</tr>
<tr>
<td>Coupling breakdown</td>
<td>&gt; 100V</td>
</tr>
<tr>
<td>Total detector current</td>
<td>&lt; 100 nA/cm² (at full depletion voltage+10%V)</td>
</tr>
<tr>
<td>Total detector current at 350V</td>
<td>&lt; 16 mA</td>
</tr>
</tbody>
</table>

Test Structures (half moons)

Figure: Detectors & test structures in KLayout

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AC Coupled Single Sided Si Strip Detector ($p^+\text{-}n^-$)

Pictures & Dimensions

- Length: 6 cm
- Width: 3.4 cm
- Number of strips: 512
- Strip width: 30 $\mu$m
- Strip Pitch: 55 $\mu$m

Fabricated Si Strip Detectors at DU in a collaboration with BEL, INDIA
IV/CV Characterization Facility at DU

Electrical Set-up Configurations for IV and CV measurements

Probe to p' bias-ring

SMU
(e.g. Keithley IV 237)

Probe to n' ohmic-side

Sensor

pA

Lo

Hi

Probe to p' bias-ring

Sensor

Probe to n' back-plane

Voltage source
(e.g. Keithley IV 237)

Hi

Lo

CV-590

Make & Model:
SUMMIT 11000B-M
Serial Number: 1260060905
-Precision manual X-Y stage

K-2410   K-237
Global Parameters

**Total Leakage Current**

Total Leakage Current vs Reverse Bias

- Y axis - Log scale

**Total Capacitance**

1/C^2 vs Reverse Bias

- f = 1kHz
- V_{fd} = 100V

1) V_{bias} < V_{fd}, 1/C^2 linear behavior
2) V_{bias} > V_{fd}, 1/C^2 constant
Interstrip Capacitance

Determines capacitive noise between the strips

Agreement between the results of interstrip capacitance for different wafers

Interstrip Capacitance vs Reverse Bias

Interstrip Capacitance vs Nr Strips

Interstrip Capacitance is uniform over the strips

Thanks to Frank, Alexander and Robert
Measurement Results (Strip Detectors)

Interstrip Properties

Interstrip Resistance  ➔ Determines DC electrical insulation between the strips

Agreement between the results of interstrip resistance for different wafers

Higher Resistivity (insulation) between the strips

Thanks to Frank, Alexander and Robert
Measurements Results (Strip Detectors)

Coupling Capacitance

Coupling Capacitance for different wafers

Measurements taken at KIT

Agreement between the results of Coupling Capacitance for different wafers

Coupling Capacitance is uniform over the number of Strips

Thanks to Frank, Alexander and Robert

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Measurement Results (Test Structures)

Effect of Guard-ring Spacing on Breakdown Voltage

Obtained maximum breakdown of 350V at optimized guard-ring spacing of 30µm
Effect of Number of Guard-rings on Breakdown Voltage

On increasing number of guard-rings, Breakdown improves.
**Total leakage current is equal to the sum of pad and guard current**

**Measurement Results**

Graph showing data points for Pad Current, Guard Current, Total Current, and Pad+Guard with axes labeled in appropriate units.
**Transient Current Technique (TCT) Set-up at DU**

**Pad Sensor**
(thickness=320μ m 1cm×1cm)

**Agilent E3632A Function Generator for triggering laser**

**Agilent 33522A Dc Power Supply for reverse biasing diode**

**Keithley 2410 Dc Power Supply for reverse biasing diode**

**Picosecond Bias Tee for filtering dc & ac signal**

**Agilent Cathode Ray Oscilloscope for display of signal**

**PicoQuant : PDL 828 Picosecond Diode Red Laser.**

For detailed description, please keep an eye on DU Poster

“Characterization of Si Detectors through TCT Technique at Delhi University” by Geetika Jain
Summary

1. DU delivered 1000 Si mini strip detectors for CMS Preshower. Worked in all three aspects of Si detector development.

2. Presently DU is involved in the R&D of AC Coupled Si micro-strip detectors (p-on-n) for future HEP experiments.

3. Participation in three activities:
   ✓ Design is optimized in two phases (p⁺-n⁻ & n⁺-n⁻) using TCAD Silvaco simulations
   ✓ Phase-I (p⁺-n⁻) detectors are fabricated successfully (Total 12 detectors)
   ✓ Phase-II (n⁺-n⁻) detectors are under fabrication at BEL, INDIA.

4. Established characterization set-up for measuring both static & dynamic properties of silicon sensors.
   ✓ Measured Global parameters i.e. total leakage current & total capacitance at DU and strip parameters like $R_{\text{int}}$, $C_{\text{int}}$, CC at KIT
   ✓ Results of $C_{\text{int}}$, $R_{\text{int}}$ and CC are in agreement for different wafers & are uniform over the number of strips.
   ✓ Measurements on Test Structures: Obtained maximum breakdown of 350V at optimized guard-ring spacing of 30μm
   On increasing number of guard-rings, breakdown improves.
Future Agenda

- Plans to irradiate strip detectors at KIT and BARC, INDIA.
- Upgrade set-up to measure strip properties at DU.
- Plans of making SQC for CMS tracker upgrade (Phase-II).
Si Group at Delhi University with C. Gallrapp

Two Professors, One Postdoc, Two PhD students, One Project Staff
Thank you!!
Back-Up Slides
Mask layer process- Individual Masks are required for following processing steps-

1) P+ implant for each strip
2) SiO2 for DC pad, bias line and p+ strips
3) Polysilicon contact opening on DC pads
4) Polysilicon b/w DC pads & bias line
5) contact opening for DC pads and bias line
6) Metalization for AC pads, DC-pads and the bias line
7) Protective layers for AC pads, DC pads and bias line

Ion Implantation (Mask2)
Boron E = 80 keV; Dose = 9x10^{13} cm^{-2}
Phosphorus E=50kEV, Dose = 10^{16} cm^{-2}
Drive-in cycle at 1100 for dopant activation and drive-in diffusion of boron
Why increasing the spacing (d(GR)) & no of guardrings improves VBD
When we reverse bias the p+ pad and backside of det where GR are floating,
potential distributes equally From p+ towards the GR and hence Efield
Gets lower and hence breakdown increases.
Strip Leakage vs Reverse Bias

Strip Leakage Current (A)

Reverse Bias (V)

D1-W7
D1-W8
D1-W10
D1-W16
D1-W18
Total Leakage Current

Total Current vs Reverse Bias

Measurement at KIT-

Detectors 1 (D1)

Measurement at KIT-
Fabrication Steps

N type Crystal (doping = 3e12 cm⁻³)

Passivation (Mask 1)
Growth of an oxide layer
Thickness = (1.0 - 1.01 μm)
Photolithography technique

Ion Implantation (Mask2)
**Boron** E = 80 keV; Dose = 9x10¹³ cm⁻²
**Phosphorus** E=50kEV, Dose = 10¹⁶cm⁻²
Drive-in cycle at 1100 for dopant activation and drive-in diffusion of boron

**p-Capacitors (Mask-3)** lithographically defined on front side
P-side capacitor oxidation step employing the Dry-Wet-Dry regime (Thickness = 0.25 - 0.33 μm)

**Oxide openings (Mask4)** over both p+ and n+ strips region to form the poly-silicon layer (Thickness: 2500 - 2530 Å)

**Lithography patterning (Mask5)**
Annealing step (Time = 45 minutes; Temperature = 950°C for dopant activation)

**Contact lithography (Mask-6)** was performed to open windows through the oxide for making contact with Aluminum metal (Thickness = 1.5 microns)

**Lithography (Mask-7)** to pattern the metal layer to define the various electrical connections. Then a short annealing step (Time = 30 minutes; Temperature = 450°C) to create ohmic contact on the front side.

**Lithography (Mask-8)** to open areas over the metal bond pads.
**Fig. 2.** $C_{\text{int}}$ vs $Q_F$ for p-spray and sensors without p-spray sensors at $V_{\text{bias}} = -100$ V.
<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Process Stage</th>
<th>Junction Depth/Thickness (µm)</th>
<th>Sheet Resistance (Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P+ Implant</td>
<td>4</td>
<td>462</td>
</tr>
<tr>
<td>2</td>
<td>N+ Implant</td>
<td>1.1</td>
<td>214</td>
</tr>
<tr>
<td>3</td>
<td>Coupling Oxide</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Oxide between Strips</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Poly Resistor</td>
<td>0.25</td>
<td>10000</td>
</tr>
<tr>
<td>6</td>
<td>Al Metallization</td>
<td>1.5</td>
<td></td>
</tr>
</tbody>
</table>
Global Measurements

1. IV
   - Ramp upto 700V
   - Min. I ~ 12nA/cm³
   
   A = Keithley 6485

2. CV
   - Ramp upto 200V
   - Min. C ~ 20nF
   - No need for isolation box

   C = Keithley 590 / HP4284A
3. $I_{\text{leak}}$

- Ramp upto 700V
- Min. $I \sim 0.1\text{nA/cm}$

4. $R_{\text{poly}}$

- Low voltage = 2V constant

5, 6. CC, $I_{\text{diel}}$

- $A = \text{Keithley 6485}$
- $C = \text{Keithley 590 / HP4284A}$
- $U = \text{Agilent 6614C}$

7. $R_{\text{int}}$

- Low voltage = 0-2V ramp in steps of 0.2V
8. $C_{int}$

9. $C_{strip}$

- Ramp upto 700V
- Min. C ~ 1.6pf/um.cm
Infrastructure Required

- **Space**: At least ~10 m² of clean room are required (class 100,000 or better)
- **The basic equipment for sensor testing (QTC) consists of:**
  - Sourcemeter $\geq 1000\,\text{V}$, $\text{I}_{\text{max}} \geq 1\,\text{mA}$
  - Picoammeter $\Delta I \sim \mu\text{A}$
  - Voltage source $\geq |10\,\text{V}|$, $\Delta V \sim 1\,\text{mV}$
  - Iso-box to decouple from bias voltage
  - Micro-probes ($\sim 7\mu\text{m}$ tip)
  - Storage cabinets with humidity control
  - Microscope
  - (Vacuum) tweezers
  - Temperature controlled vacuum jig ($\sim 20\,^\circ\text{C}$)
  - LCR-Meter $100\,\text{Hz} \leq f \leq 1\,\text{MHz}$
  - Micro positioners for strip measurement
- **Additional equipment for strip sensor characterization (2032 strips, fully automatic probe station required):**
  - XYZ-stage (accuracy $\sim 5\,\mu\text{m}$)
  - Switching-matrix including HV switching
  - Probe-cards/automated movable chuck
  - Long term setup
- **Personnel**: At least one experienced physicist, who should have participated in the development phase already and can cover the production time.
  - Well-trained students to perform the measurements.
Budget for SQC

- We have got our Five year budget (2014-2019), and the total allocated budget seems almost adequate.

- However, the funding comes in phases (first phase has started in 2014) and hence we will be able to develop the full system in ~ 3 years time.

- Will explore the possibility of becoming IT in collaboration with BARC (neutron irradiation facility at Nuclear Reactor, BARC)
Silicon Sensors Qualification & DU’s interest

Options for India

Contact person: Alexander.Dierlamm@cern.ch

- All three Institutes (Delhi, TIFR and BARC) interested in sensors R&D need to substantially improve their lab infrastructure to be able to be effective in testing the Tracker sensors. => mainly lacking in automated strip measurements

- A clear and realistic development plan needs to be defined, targeting specific testing activities in each institute. In the meanwhile, to help the R&D on the 6” sensors processing in SCL and BEL, prompt and thorough feedback can be obtained by testing the prototype sensors in KIT and/or Vienna.

- **Duccio’s comment**: Delhi, TIFR and BARC are possible choices. **Given the availability of students Delhi could perhaps host two activities.** Rad hardness qualification is particularly appropriate for BARC for the possibility of neutron irradiation locally. Developing/procuring and commissioning the needed lab infrastructure is the key issue.

- **Frank’s comment**: We would be happy to transfer our knowledge and like to encourage you to send students/post-docs to Vienna or KIT to have a close look.

Recently Ashutosh and Geetika visited KIT for one for characterization of strip sensors and understanding the setup.
Effect of GR Spacing

About Test Structure-
TS17-30µm x 30µm window for p+ implant for DC Breakdown with metal overhang over the field oxide of 3 µm.

TS19-30µm x 30µm window for p+ implant + 1 GR. GRW=25µm, GRS=20µm for DC Breakdown. There should be option for biasing all the GR. No MO, As per your mail on 11th May 2010.
TS20-30µm x 30µm window for p+ implant + 1 GR. GRW=25µm, GRS=30µm for DC Breakdown. There should be option for all biasing the GR. No MO, As per your mail on 11th May 2010.
TS21-30µm x 30µm window for p+ implant + 1 GR. GRW=25µm, GRS=40µm for DC Breakdown. There should be option for biasing all the GR. No MO, As per your mail on 11th May 2010.
TS22-30µm x 30µm window for p+ implant + 1 GR. GRW=25µm, GRS=50µm for DC Breakdown. There should be option for biasing all the GR. No MO, As per your mail on 11th May 2010.
TS23-30µm x 30µm window for p+ implant + 1 GR. GRW=25µm, GRS=60µm for DC Breakdown. There should be option for biasing all the GR. No MO, As per your mail on 11th May 2010.
Effect of No of GR

GR1-30µmx30µm window for p+ implant + 1 GR. GRW=25µm, GRS=30µm for DC Breakdown. There should be option for all biasing the GR. **No MO, As per your mail on 11th May 2010.**

GR2-30µmx30µm window for p+ implant + 2 GR. GRW1=50µm, GRW2=25µm, GRS1=30µm, GRS2=20µm for DC Breakdown. There should be option for biasing all the GR. **MO of 5µm on P+ implant. MO of 5µm on both side of each GR.**

GR3-30µmx30µm window for p+ implant + 3 GR. GRW1=50µm, GRW2=25µm, GRW3=25µm, GRS1=20µm, GRS2=30µm, GRS3=40µm for DC Breakdown. There should be option for biasing all the GR. **MO of 5µm on P+ implant. MO of 5µm on both side of each GR.**
1. When our second (phase2) Det will be completed. Any date
   3 to 4 months. Mask design is complete
2. Cost of single Det and whole phase 1 det
   Around 2 lakhs. u can convert it to euro. total cost of phase 1 around 50 lakhs
3. At KIT irradiation facility - proton?
   proton, 10 MeV
   And is it allowed to take these Det in India back?

   Yes, within limits as certified by German standards.
4. Confirm date for development of AC coupled Det (starting det) 2009 yr

   Already developed ac coupled detectors. Starting date was around 2010.
   we got the detectors in late 2012, I believe.
5. Radiation hardness test ke liye hum log simulation me I know that we
   optimized radiation damage model at different fluency and at different qf we see the
   effect on interstrip properties and please confirm for measurement we are planning
   to irradiated at KIT not in India as I thought we can irradiated our Det with neutron
   fluence at barc please confirm
   We are in the process of exploring for neutron irradiation at BARC.