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SAMPIC: a 16-channel, 10-GSPS WTDC digitizer chip for picosecond time measurement

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SAMPIC is a Waveform and Time to Digital Converter (WTDC) 16-channel chip (AMS 0.18-µm CMOS) which directly measures the arrival time of fast analog signals without the need of any external discriminator. Each channel associates a traditional DLL-based TDC providing a raw time based on a counter and a DLL with an ultra-fast 64-cell deep analog memory (bandwidth > 1.5 GHz, sampling rate > 10GS/s) allowing fine extraction of the time as well as charge, pulse width or rise-time. Each channel also integrates a discriminator that can self-trigger independently or participate into a more complex trigger embedded on-chip. External trigger is also available. After triggering, analog data is digitized on-chip by a massively parallel low-power 11-bit Wilkinson ADC running above 1 GHz and only selected data is then moved out. Dead-time is of 1.6 µs for an 11-bit conversion and as low as 200 ns for an 8-bit conversion which already provides an excellent time precision. A set of boards and DAQ system has already been developed to take data with detectors in a real environment. This setup, including a powerful software with an original interactive graphical interface, has permitted the characterization of the chip, and the measurements of its time resolution which is as good as 3 to 4 ps rms after a simple correction, itself based on a very simple calibration (14 ps rms without any correction). This calibration remains very stable with time and can thus be stored on-board.

Summary

Time stamping with picosecond accuracy is an emerging technique opening new fields for particle physics instrumentation. For example, it permits the localization of vertices with a few mm precision, thus helping associating particles coming from a common primary interaction even in a high background or can be used for particle identification using Time of Flight techniques. It has recently been demonstrated that ps timing accuracy can be reached by sampling the detector signal in ultrafast analogue memories using Switched Capacitor Arrays (SCA) [1, 2] for reasonable power, space and money budgets. Moreover, the knowledge of the signal waveform permits extracting other useful parameters as charge, pulse width or rise-time and optimizing the timing extraction algorithm during or even after data taking. Contrasting with the existing fast sampler chips usually designed for all-purpose application and requiring external electronics to be used for accurate timing, the SAMPIC chip, presented here, has been designed specifically for this type of application. SAMPIC is actually a technological demonstrator, already usable for measurements with detectors, which is intended to be improved in the future to permit very low dead-time operation. This chip, designed in the 0.18 µm CMOS technology from AMS, integrates 16 measurement channels that can be operated independently or using a common trigger, either internal or external. Each of the channels integrates a discriminator, a 18-bit deep TDC and a 64-cell deep SCA. A 64-step DLL, common to all the channels, provides the multiphase clock used in the SCA and the TDC. The DLL step, tunable from 100ps to 1ns, defines the TDC step as well as the SCA sampling frequency (1 to 10 GSPS). The input analog signal is continuously sampled and stored at a rate between 1.6 GSPS and 10 GSPS in the 1.5-GHz bandwidth analog memory until an event is detected by the discriminator. A trigger signal is then generated, freezing the analog memory, time-stamping the event in the TDC and rising a flag indicating that an event is waiting for conversion and readout. The analog to digital conversion of the waveforms is performed in parallel over up to 11 bits for all the cells of the channels having detected an event. For this purpose, a 1.3-GHz Wilkinson ADC is associated with each analog memory cell. Once the conversion is finished, data can be readout using a 14-bit LVDS bus theoretically able to run up to

400 MHz, starting by the TDC data then followed by the SCA waveform for which it is possible to send only a zone of interest corresponding to the signal pulse. Once the SCA data has been converted, the channel is available for a new event so that the maximum dead-time from a given channel of SAMPIC is of only 1.6 µs if the 11-bit conversion has been chosen, and goes down to 200 ns if the conversion is performed on 8 bits. This dead-time is indeed divided by 2 for each bit removed in the conversion range. It has to be pointed out that no noticeable loss of performance occurs when going from 11 down to 8 bits for pulses with an amplitude above 100 mV. One major benefit of the proposed architecture is that it can use a rather slow discriminator as the latter provides only a trigger signal and not the ultimate timing accuracy which is derived from the sole sampled waveform.
The SAMPIC modules are already being used at CERN by a few experiments like TOTEM (CMS). They are mostly associated with diamonds, fast silicon detectors or MCP-PMTs during their characterization, in lab or on test beams. TOTEM is currently integrating a SAMPIC daughterboard on a CMS-compatible motherboard in order to qualify SAMPIC inside the CMS control and readout environment.
The talk will describe the chip architecture with more details and will give a detailed report of the performances measured with the prototype modules.

[1] J-F. Genat, G. Varner, F. Tang, H.J. Frisch, "Signal Processing for Pico-second Resolution Timing Measurements", Nucl. Instr. Meth. A 607 (2009) 387-393.
[2] D. Breton, E. Delagnes, J. Maalmi, K. Nishimura, L.L. Ruckman, G. Varner, J. Va'vra, "High Resolution Photon Timing with MCP-PMTs: A Comparison of Commercial Constant Franction Discriminator (CFD) with ASIC-based waveform digitizers TARGET and WaveCatcher", Nucl. Instr. Meth A 629 (2011) 123-132.

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