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SAMPIC: A 16-CHANNEL, 10-GSPS WTDC DIGITIZER CHIP FOR PICOSECOND TIME MEASUREMENT

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INTRODUCTION

- Waveform digitization permits extracting all information from signal (including time)
 - High-end oscilloscopes are the grail of most test benches but with only 4 channels ...
 - High precision measurement implies high sampling rate (>> GS/s) => huge amount of data, especially at large scale
 - Usual analog memories (SAM, DRS, ...) nicely solve this problem but readout deadtime (~2 to 100 μs) may be a limitation
- **TDCs** are specifically used for **time measurement**
 - Information is concentrated => reduced dataflow, good for large scale measurement
 - But they do not provide information on waveform, except TOT, and they work on **digital signals**
- Now what about getting a high precision TDC also providing its associated input signal waveform => this is the WTDC

THE « WAVEFORM TDC » Concept (WTDC)

- WTDC: a TDC taking a snapshot of the relevant part of the analog waveform
- Overall time information is obtained by combining 3 times :
- **TDC Coarse** = Timestamp Gray Counter (few ns step) **Medium** = DLL locked on the clock to define region of interest (~100 ps step)
 - **Fine** = samples of the waveform (**digital algorithm** will give a precision of a few ps)
 - Discriminator is used only for triggering, not for timing => no jitter added on measurement, low power
 - Digitized waveform available to extract other parameters (Q, amplitude,...)



THE SAMPIC WAVEFORM TDC

SAMPIC: a TDC also taking a picture of a part of the signal waveform



Global time = counter (~10ns) + DLL (~100ps) + waveform(~ps)

Waveform is available for extraction of other parameters (Q, A)

One Common 12-bit Gray
 Counter (FClk up to 160MHz) for
 Coarse Timestamping.

One Common servo-controlled
 DLL: (from 1 to 10 GHz) used for
 medium precision timing & analog
 sampling

• 16 independent WTDC channels each with :

✓1 discriminator for self triggering
✓ Registers to store the timestamps
✓ 64-cell deep SCA analog memory
✓ One 11-bit ADC/ cell

(Total : 64 x 16 = 1024 on-chip ADCs)

• One common 1.3 GHz oscillator + counter used as timebase for all the Wilkinson A to D converters.

Read-Out interface
SPI Link for Slow Control configuration

GLOBAL ARCHITECTURE OF SAMPIC





- Technology: AMS CMOS 0.18µ
- Size: 8 mm2
- Package: 128-pin QFP, pitch of 0.4mm



SAMPIC TRIGGERING OPTIONS

- One very low power signal discriminator/channel
- One 10-bit DAC/channel to set the threshold (which can be external)
- Several trigger modes programmable for each channel:
 - External

- "Central" trigger (only OR in V1)
- Edge selection
- Enable/disable



Only the triggered channels are in dead time

ANALOG MEMORY (SCA) IN EACH CHANNEL

- 64-cell deep, trade-off between:
 - Time precision / stability (=> short)
 - Bandwidth uniformity (=> short)
 - Time available for trigger latency (=> long)
- No input buffer, single ended
- 3-switch cell structure to reduce leakages and ghosts.
 Switch 3 also isolates from input bus during conversion
- ~ 1 V usable range, > 1.5 GHz BW



 Trigger position marked on DLL cells => medium precision timing and used for Optional Region of Interest Readout (only few samples read)





WILKINSON DIGITIZATION (1 PER CELL) & READOUT



- *a* Trigger: simultaneous digitization of all the cells of all the triggered ch.
 - Starts the on-chip 1.3 GHz timebase and broadcasts selectively its 11-bit output to the channels to convert
 - Starts the ramp generators of the channels to convert
 - When ramp crosses cell value => counter outputs stored in a local register => A to D conversion is done

• At the end of the conversion, the Waveform digitized samples, merged with Timestamps, are read channel by channel, through the 12-bit LVDS bus (up to 4 Gbit/s)

 Ramp slope is tunable: speed/precision tradeoff => 1.6µs for 11bits down to 100ns for 7 bits : main contribution to the Dead Time

A channel is in deadtime only during conversion, not during readout

READOUT PHILOSOPHY

- Readout driven by Read and RCk signals => controlled by FPGA
- Data is read **channel by channel** as soon it is available
- Rotating **priority mechanism** to avoid reading always the same channel at high rate
- Optional Region Of Interest readout to reduce the dead time (nb of cells read can be chosen dynamically)
- Readout of converted data through a 12-bit parallel LVDS bus including:
 - Channel Identifier, Timestamps, Trigger Cell Index
 - The cells (all or a selected set) of a given channel sent sequentially
 - Potentially up to 4 Gbits/s



Channel is not in deadtime during readout, only during conversion (data register is really a buffer stage)

PROTOTYPING & ACQUISITION SETUP

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Infos Warnings Errors

1 0.1000 v

- Chip prototyped in AMS 180nm CMOS (8mm²)
- First version: SAMPIC0. Now using SAMPIC1.
- 32-channel module integrating 2 mezzanines
- 1 SAMPIC/mezzanine
- USB, Ethernet UDP



- Acquisition software and C libraries
- => full characterization of the chip & module
- Timing extraction (dCFD, interpolation...)
- Special display for WTDC mode
- Already usable for small scale experiments



The acquisition

software

XAvia Auto IV On Off Xmin # 40601444 YAvia Auto IV On Off

CHIP PROTOTYPING AND TEST STATUS

- All features are functional.
- Readout currently performed at 1 Gbit/s (firmware to be fixed for higher rates) *First signal digitized by SAMPIC:*
- Sampling is working:
 - up to 10.2 GS/s for the 8 first channels
 - up to 8.2 GS/s and down to 1 GS/s
 - for all the channels



1GHz sinewave @10.2GS/s

- No evidence of cell Leakage for storage times up to tens μs
- Power consumption: 10-15mW / channel
- Characterization reported in this talk performed
- (a) 6.4 GS/s, but no major change for other frequencies



DC PERFORMANCE

- Wilkinson ADC works as expected with 1.1 GHz clock
 ~1 V dynamic range/0.5mV LSB => 11 bit digitizer
- Spread of the DC gain ~ 1% rms
 <1,4 % peak to peak integral non-linearity
 Both effects are systematic (switches' charge injection)
 Corrected cell/cell by software (linear fit)
 => Noise = 0.95 mV RMS (unchanged with freq)
 => ~10-bit RMS dynamic range
- Discriminator "noise" = 2 mV RMS => Reliable Self-triggering for pulses > 15mV







BANDWIDTH AND CROSS-TALK



350 MHz sinewave (0.5V peak-peak) with 64 samples
'Out of the box' (no timing correction) @ 6.4 GS/s

-3dB Bandwidth ~ 1.7 GHz

Ringing effects around 1GHz probably due to non-perfect impedance matching on the board

Crosstalk between channels is smaller than $\pm 1.5\%$



Time Difference Resolution (TDR)



Timing Difference Resolution (TDR)



ΔT RESOLUTION VS DELAY





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ΔT RESOLUTION VS DELAY





- TDR < 5 ps RMS after time cor.
- TDR is constant for $\Delta t > 10$ ns
- ~ unchanged when using 2 chips from 2 mezzanines (slope here comes from slower risetime of 800ps)
 => measurement are uncorrelated
 => channel single pulse timing resolution is < 3.5 ps RMS (5 ps/√2)

EXPLORING LARGER DELAYS: TOWARD AN « ABSOLUTE » TIME MEASUREMENT

- Now we use 2 channels of a TEK AFG 3252 arbitrary waveform generator and program their relative delay (10-ps steps)
- Slower than the previous generator (2.5ns risetime min)
- <u>TEK</u>AFG 3252 <u>is specified</u> for an absolute precision of few 10 ps delay and a 100ps jitter
- => Measurements are clearly much better



TDR is < 10ps RMS, even for delays up to 10 μs => 1-ppm RESOLUTION

Difference between AFG programmed delay and measured value is < +/-15ps

TIMING RESOLUTION VS RATE

1ns FWHM, 400ps risetime, 0.7V signals sent to 2 channels of SAMPIC

- 7.1ns delay by cable, 6.4 GS/s, 11-bit mode, 64 samples, both INLs corrected
- Rate is progressively increased.



The measured delay and its resolution are stable for rates up to 2 MHz

TIMING RESOLUTION (DIGITAL CFD) VS ADC NUMBER OF BITS

- In order to minimize dead-time, ADC number of bits can be reduced: factor 2 for 10 bits (800 ns), 4 for 9 bits (400 ns), 8 for 8 bits (200 ns).
- Looking for the effect of the ADC number of bits on time resolution...
- Signal amplitude is the key element in this case: time resolution degrades for small signals since electronics noise becomes dominant
 - There is very little difference in performance between 11, 10 and 9-bit modes.
 - Where electronics noise dominates, other methods than dCFD can be used ...



No degradation on timing for pulses above 100mV for 8 bits & 50mV for 9 bits

TAKING DATA WITH DETECTORS

- SAMPIC modules have already been used with numerous different detectors on test benches or test beams
- Unfortunately, very little public data available until now (due to collaborations strict publicy rules)
- Tested with MCPPMTs, SiPMs, fast Silicon Detectors, Diamonds: performances are usually equivalent to measurements with high-end oscilloscopes
- SAMPIC has been used for test beams of AFP and TOTEM
- **TOTEM** is developping a CMS-compatible motherboard able to house SAMPIC mezzanines
- **SHIP** included the use of SAMPIC in its technical proposal for its fast timing detector and calorimeter (two-gain version)
- Rising interest from the **TOF-PET** community ...

MEASURING PICOSECONDS ...

- SAMPIC module has been connected to **S.White's fast mesh-APD** at CERN (see S.White's poster).
- Goal : measure the **time difference between the pulser** and the APD signal => detector time resolution
- All measurements below performed in ~1 hour.







Best measurement < 10 ps rms</p>

WORK PLANNED OR IN PROGRESS

- Improvements of Firmware and DAQ software in constant progress
 - Embedded firmware CFD extraction is under study
- Second version was received in April 2015: SAMPIC1
 - Correction of the identified few bugs of SAMPIC0
 - New memory cell with improvement of the linearity
- New submission planned for **Summer 2015 : SAMPIC2**
 - Nb of bits for coarse timestamp => 16 bits
 - Improved "central trigger" (coincidence & or)
 - ADC resolution internally selectable between 7 and 11 bits
 - Channels could be merged by groups of 2 or 4 to be used as multiple buffers to reduce dead time
 - Integrated TOT measurement for signals longer than the clock period
 - PET dedicated version : SAMPET (differential input to fit with NINO output signals)
- 64-channel board and 256-channel mini-crate soon available.

CONCLUSION



A 16-channel self-triggered Waveform TDC chip and its 32-channel module and acquisition system have been designed and characterized:

- Works on **analog** signals with:
 - 1.6 GHz BW
 - Sampling rate between 1 and 10 GS/s
 - Low noise (even with trigger and acquisition running)
 - 10-bit RMS waveform digitizer
 - < 3.5ps RMS single pulse timing resolution
 - 1.6µs (11 bits) down to 100ns (7 bits) deadtime/channel
- Already used for tests with detectors (including test beams @ CERN)
- Work ongoing:
 - Readout (firmware + software) optimization
 - Fine characterization of the second version
 - Third version and PET-dedicated version under design
 - 64 to 256-channel systems soon available

SAMPIC: PERFORMANCE SUMMARY

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV RMS
SCA depth	64	Cells
Sampling speed	1 to 8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	< 1	mV RMS
Dynamic range	> 10	bits RMS
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	μs
Readout time / ch @ 1Gbit/s (full waveform)	875	ns
Single Pulse Time precision before correction	< 15	ps RMS
Single Pulse Time precision after time INL correction	< 3.5	ps RMS

SPARE SLIDES

OUR FORMER DEVELOPMENTS OF ANALOG MEMORIES FOR WAVEFORM DIGITIZING

HAMAC

1998-2002 DMILL

MATACO

2000-2003

CMOS 0.8µ

- We design analog memories since 1992 => first prototype (PIPELINE V1) of the SCA for the ATLAS LARG calorimeter.
 80,000 HAMAC chips (2002) are on duty on the LHC.
- Since 2002, 3 new generations of fast samplers: ARS, MATACQ, SAM => more than **30,000 chips in use**.
- Our favourite structure is a sampling matrix.
- A few ps time resolution was demonstrated at system level (up to 64 channels) with SAMLONG, but deadtime can be a limitation.



THE SAMPIC PROJECT

- Generic R&D funded by "P2IO Labex" grant
- Initially intended as a common prototype ASIC for high precision time of flight measurement (5 ps rms) in ATLAS AFP and SuperB FTOF



- Goals for the first prototype (SAMPIC0, received in June 2013):
 - Validation of the Waveform TDC structure
 - Evaluation of AMS 0.18μm technology for mixed design
 - Design of a multichannel chip usable in a real environment
 => connected to detector with a real readout and DAQ system
- Core of a future "dead-time free" chip

A FEW COMMENTS ABOUT USUAL TDCs

Most ASIC or FPGA fast TDCs are using:

- digital counters (coarse timestamp)
- servo-controlled Delay Line Loops (DLLs) (fine timestamp)

Their resolution is limited by the DLL step



In a timing chain: a **DISCRIMINATOR** is required

- critical and often high power
- Add additional jitter and residues of time walk effect

WHY AMS 0.18M ?

- Based on IBM 0.18µm : IBM quality & documentation
- Good Standard Cells Library
- Good lifetime foreseen (HV module, automotive)
- 1.8V power supply: nice for analog design/ high dynamic range
- Reasonable leakages
- Good noise properties (already checked with IdefX chips for CdTe)
- Reasonable radiation hardness
- Less complex (and less expensive) than IBM 0.13μm
- AMS high quality Design Kit
- Easy access (CMP, Europractice, AMS)

SIMPLEST OPERATION: 1 HIT, 1 CHANNEL



MULTIPLE HITS, 1 CHANNEL



HITS ON 2 CHANNELS, 2 CONVERSIONS



HITS ON 2 CHANNELS, SIMULTANEOUS CONVERSIONS



SAMPICO: XTALK MEASUREMENT

- 800mV, 1ns FWHM, 300ps risetime and falltime injected on **channel 7(blue)**
- Signal measured on the other channels
- Xtalk = derivative and decrease as the distance to the injection channel
- Xtalk signal is bipolar with ~ equal positive and negative lobe
- Similar plot, but shifted if injection in another channel (red)





SELF-TRIGGER EFFICIENCY AND NOISE

- Tested 150 mV, 1 ns- wide pulses (3.1 kHz repetition rate)
- Threshold (internal or external) sweep => trigger efficiency curve
- Discriminator performance extracted by fitting the S curve by an error function
- Better noise if threshold internally set (decoupling problem on board)



ΔT RESOLUTION VS DELAY



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TIMING RESOLUTION VS AMPLITUDE & RISETIME (1 NS FWHM)- 15 NS DELAY, DIGITAL CFD ALGORITHM



- 2 zones: sampling jitter or S/N limited zones.
- TDR < 10 ps RMS for pulse amplitudes > 100mV
- TDR < 20 ps RMS for pulse amplitudes > 40 mV
- Can be improved by using mores samples (if feasible and uncorrelated) since dCFD uses only 2 samples

CALIBRATION PHILOSOPHY

- SCAs-based chips are suffering from reproducible non-idealities which can be easily corrected after calibration:
 - The goal is to find the set with the **best performance/complexity ratio**.
 - But also to find the right set for the **highest level of performance**.
- SAMPIC actually offers very good performance with a reduced set of calibrations :
 - Amplitude: cell pedestal and gain (linear or parabolic fit)
 - **Time: INL** (one offset per cell)
 - This leads to a limited volume of standard calibration data (6 Bytes/cell/sampling frequency = > 8 kBytes/chip/sampling frequency)
 => can easily be stored in the on-board EEPROM.
- These simple corrections could even be applied in the FPGA.
- Highest level calibrations permit debugging the chip and pushing the performance to its limit (still unknown).

TIMING NON-LINEARITIES

- Dispersion of single delays => time DNL
- **Cumulative effect** => **time INL**. Gets worse with delay line length.
- Systematic & fixed effect => non equidistant samples => Time Base Distortion

If we can measure it => we can correct it !

But calibration and even more correction have to remain "reasonable".



TIME INL CALIBRATION AND CORRECTION



Method we introduced in 2009 and used since for our analog memories, assuming that a sinewave is nearly linear in its zero crossing region: much more precise than statistical distribution

• Search of zero-crossing segments of a free running asynchronous sine wave

=> length[position]

- Calculate the average amplitude for zero-crossing segment for each cell.
- Renormalize (divide by average amplitude for all the cells and multiply by the clock period/number of DLL steps)
 => time duration for each step = "time DNL"
- Integrate this plot:
- ⇒ Fixed Pattern Jitter = correction to apply to the time of each sample = "time INL"

Time INL correction:

- Simple addition on T_{sample}
- Also permits the calculation of real equidistant samples by interpolation or digital filtering.