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A 12-bit SAR ADC integrated on a multichannel Silicon Drift Detector Readout IC

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A 12-bit analog-to-digital converter (ADC) addressed to Silicon-Drift Detectors (SDDs) multichannel readout front-ends for X and gamma-ray applications is presented. Aiming at digitizing output multiplexed data from the upstream analog filters banks, the converter must ensure at least 11-bit accuracy and a sampling frequency of about 5 MS/s. The ADC architecture is the charge-redistribution (CR) successive-approximation register (SAR). A fully-differential topology has also been chosen for better rejection of common-mode noise and disturbances. The internal DAC is made of binary-scaled capacitors, whose bottom plates are switched by the SAR logic to perform the binary search of the analog input value by means of the monotonic switching scheme. The A/D converter is integrated on SFERA, a multichannel ASIC fabricated in a standard CMOS 0.35 um 3.3 V technology and it occupies an area of 0.44 mm2. Simulated static performance show monotonicity over the whole input-output characteristic while differential (DNL) and integral nonlinearity (INL) appear to be lower than half LSB. Dynamic performance are instead expected to be higher than those of the first ADC prototype, which consisted in 68 dB SFDR, 66.5 dB SiNAD and an effective number of bits (ENOB) equal to 10.75 at full-scale and 4 MS/s sampling rate.
The description of the circuit topology and of inner blocks architectures together with the experimental characterization of both static and dynamic parameters is here presented.

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