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Electronics Design and Layout Complexity of the ATLAS New Small Wheels

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The LHC resumes its operation in 2015 aiming to deliver an average luminosity of 1×10^34 cm^−2 s^−1. Further upgrades of the experiments and the accelerator in 2018/19 and 2022/23 will allow to further increase the luminosity to 2×10^34 cm^−2s^−1 and 5×10^34 cm^−2s^−1, respectively. For the ultimate HL-LHC phase the expected mean number of interactions per bunch crossing will increase from 55 at 2×10^34 cm^−2s^−1 to ~140 at 5×10^34 cm^−2s^−1. This increase, drastically impacts the ATLAS trigger rates. For the ATLAS Muon Spectrometer, a replacement of the innermost endcap stations, the so called "Small Wheels", is therefore planned for 2018/19 to be able to maintain a low pT threshold for single muon and excellent tracking capability also in the HL-LHC regime. The New Small Wheels will feature two new detector technologies, Resistive Micromegas and small strip Thin Gap Chambers conforming a system of ~2.4 million readout channels. Both detector technologies will provide trigger and
tracking primitives to the muon trigger system and are already designed as fully compliant with the post-2024 HL-LHC operation. The electronics design of such a system will be implemented including the design of 4 custom front-end ASICs capable to drive trigger and tracking primitives. Among them the 64 channels VMM, a common frontend ASIC providing amplitude, timing measurements, per channel analog-to-digital conversions and in parallel direct trigger outputs. The design integrates the
Gigabit transceiver and Slow Control ASICs developed at CERN. The data flow is designed through a high-throughput network. The overall design along with the first ASIC and board prototypes will be presented.

Collaboration

ATLAS Muon Collaboration

Summary

The LHC resumes its operation in 2015 aiming to deliver an average luminosity of 1×10^34 cm^−2 s^−1. Further upgrades of the experiments and the accelerator in 2018/19 and 2022/23 will allow to further increase the luminosity to 2×10^34 cm^−2s^−1 and 5×10^34 cm^−2s^−1, respectively. For the ultimate HL-LHC phase the expected mean number of interactions per bunch crossing will increase from 55 at 2×10^34 cm^−2s^−1 to ~140 at 5×10^34 cm^−2s^−1. This increase, drastically impacts the ATLAS trigger and trigger rates. For the ATLAS Muon Spectrometer, a replacement of the innermost endcap stations, the so called "Small Wheels", is therefore planned for 2018/19 to be able to maintain a low pT threshold for single muon and excellent tracking capability also in the HL-LHC regime. The New Small Wheels will feature two new detector technologies, Resistive Micromegas and small strip Thin Gap Chambers conforming a system of ~2.4 million readout channels. Both detector technologies will provide trigger and tracking primitives to the muon trigger system and are already designed as fully compliant with the post -2024 HL-LHC operation. To allow for some safety margin, the design studies assume a maximum instantaneous luminosity of 7×10^34 cm^−2 s^−1, 200 pile-up events, trigger rates of 1 MHz at Level-0 and 400 KHz at Level-1. It is also foreseen that the New Small Wheels will

operate inside a magnetic field. A radiation dose of ~ 1700Gy (inner radius) is expected. The electronics design of such a system will be implemented in some 8000 front-end boards including the design of 4 different custom front-end ASICs capable to drive trigger and tracking primitives with high speed serialisers to drive trigger candidates to the backend trigger processor system. Among them the 64 channels VMM, a common frontend ASIC for both detector technologies and charge-interpolating trackers, providing amplitude, timing measurements, per channel analog-to-digital conversions and in parallel direct trigger outputs. The candidate selection is designed within the budget latency of 1us, and 6us after 2024. Moreover, the design integrates the GBTx (Gigabit transceiver) ASIC and a Slow Control ASIC developed at CERN. The data flow is designed through a high-throughput network approach. The overall design along with the first ASIC and board prototypes will be presented.

Primary author: Dr STELZER-CHILTON (PLACEHOLDER, SPEAKER TO BE SELECTED), Oliver (TRIUMF)

Presenter: Dr YACOOB, Sahal (University of KwaZulu-Natal)

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