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CITIROC 32channel ASIC for SiPM readout

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CITIROC is a 32-channel front-end ASIC designed to readout Silicon Photo-Multipliers (SiPM) for the proposed ASTRI SST-2M Small Size Telescopes of the Cherenkov Telescope Array (CTA). CITIROC is an evolution of EASIROC/SPIROC, chip proposed by INAF/Palermo to readout efficiently and at low power the focal plane made of SiPMs. Based on variable gain/low noise preamplifiers and high speed discriminators, it allows easy triggering down to 1/3 of photoelectron (50fC) and provides the 32 discriminator outputs to extract timing down to 50 ps. A second set of 32 discriminators also allows fast event validation with a higher threshold. Each channel is also equipped with a variable bandpass shaper (12.5 ns to 87.5 ns) and peak-sensing holder to provide a multiplexed charge readout up to 2500 pe.(400 pC). As for previous chips, a channel-wise 5V 8-bit DAC allows individual adjustment of the SiPM overvoltage. The power consumption is around 2.5mW/channel allowing two naked chips (64 channels) to be mounted on a small size board. 37 boards equipped with CITIROCs has been realized by INAF/Palermo and successfully tested. In this paper we give a description of the main features of CITIROC.

Summary

Citiroc is a new ASIC designed by Weeroc, a start-up company from the Omega microelectronics group of IN2P3/CNRS. Each channel of this new ASIC embeds a front-end read-out chain composed of two AC-coupled voltage low-noise preamplifier with variable-gain adjustment. The utility of the gain tuning on the preamplifiers is twofold. On the first hand it allows to compensate non-uniformity between channels by finely adjusting gain channel by channel, on the second hand, it allows to adjust the general gain of the amplification chain to adjust the read-out chain to the SiPM gain, allowing a large choice of SiPM on the system to be used. Citiroc has a new channel-by-channel trigger chain composed of a fast shaper followed by two discriminators with individual channel-by-channel threshold adjustment to be able to trig on the first photo-electron and validate the trigger on the first few photoelectrons. That double trigger allows a great dark noise rejection at the first stage of the read-out chain and avoids saturating the DAQ with noise events. Each trigger channel can be masked in case of noisy channel, latched, or output the discriminator output as is depending on user needs. A general ASIC trigger is also outputted through a 32-input trigger OR. Citiroc energy measurement is composed of two variable-gain shapers to get energy measurement from one to 2500 photoelectron with 1% linearity and a photo-electron to noise ratio of 10. Charge proportional to energy can be stored in an analogue memory using either an analogue memory or a peak-sensing detector to get rid of the hold signal versus trigger delay. A channel-by-channel input DAC allows adjusting the high voltage of the SiPM over 5V with 8-bit resolution to correct for SiPM over-voltage non-uniformity. Citiroc outputs 32 trigger outputs as well as a multiplexed tri-state hit-register to allow several Citiroc to be serialized on a single hit-register serial bus. Citiroc outputs two multiplexed analogue outputs to read-out the charge on both low and high gain to ease the low-gain and low-gain channel inter-calibration. Citiroc also embed a general 10-bit DAC for coarse general threshold adjustment. Voltage references in the ASIC are done with a bandgap to improve power supply rejection ratio and temperature sensitivity of the ASIC. Citiroc is aimed to be mounted very close to the SiPM in the systems it will be used in. A temperature sensor has been embedded to allow users to finely sense the temperature within their multi-channel system to correct for SiPM gain over voltage adjustment with temperature.

The chips have been qualified by INAF/Palermo group to equip a small hybrid with 16 SiPMs matrixes that

compose the focal plane of the SST CTA ASTRI project. Experimental results with the chips and sensors will be presented

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