Outline

• Motivations for the tracker detector upgrade for the HL-LHC
• Pixel Tracker
• Outer Tracker
• Level 1 Tracking and Performances
• Summary
Phase-2 Motivations

Major achievement of the LHC: **Higgs boson discovery in 2012.** But we want to go further…

- **Investigating the Higgs sector:**
  - Higgs couplings and properties
  - Higgs self coupling by searching di-Higgs production
  - Vector Boson Scattering properties

- **Standard Model (SM) measurements:**
  - Precision measurements (e.g. $M_W$, $\sin\theta_W$, $\alpha_s$)
  - Search for rare SM processes, enhanced by BSM (e.g. $B_{s,d} \to \mu^+\mu^-$)
  - Differential measurements of $W$, $Z$, di-bosons, top

Goal: increase the luminosity by a factor of $\sim 10$
CMS toward HL-LHC Upgrade

<table>
<thead>
<tr>
<th>E_{CM} (TeV)</th>
<th>L (cm^{-2} s^{-1})</th>
<th>PU</th>
<th>∫Ldt (fb^{-1})</th>
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</thead>
<tbody>
<tr>
<td>7-8</td>
<td>2 x 10^{34}</td>
<td>~50</td>
<td>~300</td>
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<tr>
<td>7 x 10^{33}</td>
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<td>~20-30</td>
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<td>30</td>
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Phase-0
- past 2012, 2013, 2014

Phase-1

Phase-2
- 2023, 2024, 2025

Phase-2 Pixel Detector Requirements:
- ~3 times the hit rate of Phase-1
- ~10 times the radiation dose of Phase-1
- ~10 times the particle fluence of Phase-1

Phase-2 Outer Tracker Requirements:
- ~6 times the radiation dose of Phase-1
- Trigger information at level 1 needed

Tracking degradation of Phase-1 tracker if used in HL-LHC conditions:
- Impact parameter degradation > 50% after 500 fb^{-1}
- Data loss of ~7% at PU = 140

We are here
Installation of the new CMS Phase-1 pixel detector during extended winter shut-down

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Phase-2 Tracker Layout

Outer Tracker

Pixel Detector
Pixel Detector
Pixel Detector Requirements

Increase of granularity
- Motivation: pixel occupancy reduction, resolution on high-pT tracks and two-tracks separation improvement
- Solution: small pixel size (100×25 or 50×50 μm²)
- Hit rate up to 2 GHz/cm² → 100 kHz/pixel
- Outer layers with larger pixels if necessary, with the same chip
- Read-Out Chip (ROC) technology: 65 nm CMOS (RD53 Collaboration)

Increase of forward acceptance
- Motivation: to cover jet region of Vector Boson Fusion and Vector Boson Scattering
- Coverage up to pseudo-rapidity η ~4 (now η = 2.4)
- 4 barrel layers + 10 forward disks (now 3 barrel layers + 2 disks)
Radiation Hardness

**ROC radiation hardness**
Expected dose: ~1 Grad @ r = 30 mm (most internal layer)
Solution: 65 nm CMOS technology

**Sensor radiation hardness**
Expected fluence: $\sim 2 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$ @ r = 30 mm
Solution: reduction of the drift distance to reduce the charge lost by trapping:

**Thin planar sensors**
- 100 $\mu$m < thickness < 200 $\mu$m
- n-in-p implant
- for strip structures $\sim 4000 \text{ e}^- @ 800 \text{V}$ after $1.3 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2$

**3D sensors**
- columnar electrodes
- higher radiation hardness
- lower depletion voltage
- $\sim 7000 \text{ e}^- @ 150 \text{V}$ after $5 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$
Pixel Detector Layout Studies

Configuration #1
- Inner BPIX: layer 1 and 2
- Outer BPIX: layer 3 and 4
- Inner FPIX: inner modules
- Outer FPIX: outer modules

Configuration #2
- Inner BPIX: layer 1 and 2
- Outer BPIX: layer 3 and 4
- Inner FPIX: inner modules
- Outer FPIX: outer modules

Configuration #3
- Inner BPIX: 25x100
- Outer BPIX: 50x200
- FPIX: 50x50

Configuration #4
- Inner BPIX: 25x100
- Inner FPIX: 50x50
- Outer BPIX: 100x100
- Outer FPIX: 100x100

Configuration #5
- Inner BPIX: 25x100
- Inner FPIX: 50x50
- Outer BPIX: 50x200
- Outer FPIX: 100x100

- Too much d_0 degradation with pure squared pixels in BPIX → square pixels not suitable for the barrel
- Two extreme configurations, #1 and #5, have comparable tracking performance
- Config. #5 has ~1/2 channels of #1

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Pixel Detector Perspectives

Sensors:
- Thin Planar: submission expected in 2015 to study feasibility of small pixel, p-spray and p-stop insulations, radiation tolerance and resolution (in test-beam)
- 3D: 2 submissions expected in 2015:
  - CNM: trial of Phase-2 pixel size with thicker wafer
  - FBK: see talk of Prof. Gian-Franco Dalla Betta

Front-end ASIC:
- Good progress in RD53: see poster of Prof. Valerio Re

Tracker Layout:
- Ongoing full simulation studies to estimate hit resolution, occupancy and hit rates as a function of pixel pitch, thickness and electronic threshold
Outer Tracker
Radiation Hardness

- Expected fluence up to $1.5 \times 10^{15}$ n$_{eq}$/cm$^2$
- Investigation based on Hamamatsu test samples:
  - standard, oxygen-rich ([O] > $2 \times 10^{16}$cm$^{-3}$) materials
  - p-in-n, n-in-p implant;
  - Float-zone, Magnetic Czochralski, Epi substrate;
  - 300, 200, 100, 50 µm active thickness

Conclusions:
- n-in-p better: higher radiation tolerance with respect to p-in-n
- MCz sensors: charge collection not dependent on annealing
- 200 µm sensors have lower current and same signal as 300 µm at highest dose
- cold operation (-20°C) is needed at the high doses
pT-module Concept

**Trigger requirement:**
Despite the foreseen improvements, muon and calorimeter-based L1 will not be able to stand the rates due to the PU and the limited resolution: e.g., in the muon case, no pT threshold is effective in reducing the rate → the Tracker must provide informations to the L1 system

Thanks to the CMS 3.8 T magnetic field, it is possible to discriminate high-pT tracks

Stubs are processed in the back end to build L1 track primitives

- @ 40 MHz (BX rate)
- @ 750 kHz (L1A rate)
PS and 2S Modules

**PS modules: Macro Pixel + Strip**

- Macro Pixel: 1.5 mm $\times$ 100 $\mu$m DC coupled
- Strip: 2.4 cm $\times$ 100 $\mu$m AC coupled
- Module area: $\sim$5 $\times$ 10 cm$^2$
- Power: $\sim$6-8 W

**2S modules: Strip + Strip**

- Strip: 5 cm $\times$ 90 $\mu$m AC coupled (both sides)
- Module area: $\sim$10 $\times$ 10 cm$^2$
- Power: $\sim$4-5 W

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**Low-power GigaBit Transceiver** current under development

**Silicon strip sensor**

**Macro-Pixel ASIC (MPA)**

**Silicon pixel sensor**

**Flexible hybrid**

**DC/DC converter**

10-12V lines: lower current, lower material

**Concentrator IC (CIC)**

FE chip data sparsification

**Low-power GigaBit Transceiver** current under development

**Silicon strip sensors**

**CMS Binary Chip (CBC)**

**Flexible hybrid**

**DC/DC converter**

10-12V lines: lower current, lower material

**Concentrator IC (CIC)**

FE chip data sparsification
Modules Prototypes

2×CBC functional module

Characteristics:
- 2 CBC chips (instead of 8)
- Electrical readout (not optical)
- No data concentrator
- Rigid hybrid
- Stub-finding logic
- Nominal noise and threshold
- Tested on beam (December 2013)

8×CBC prototype

Characteristics:
- 2×8 CBC chips
- Flex hybrid
- Just produced
- Used to validate the full-scale assembly

Efficiency vs $p_T$

- Module tilted to emulate $p_T$

EXP $p_T$ cut = 2.14 GeV/c
FIT $p_T$ cut = 2.17 GeV/c
FIT $\alpha(p_T$ cut) = 0.1 GeV/c
Sensor spacing optimised as a function of $p_T$ threshold (2 GeV), module position and sensor pitch. Further tuning performed by adjusting hit-matching windows.

**Outer Tracker Shopping List**

- ~7100 PS modules: higher granularity, $z/\eta$ info provided
- ~8400 2S modules: lower costs and lower power density, used at larger radii
Outer Tracker Perspectives

Sensors:
• Several submissions ongoing from different vendors to evaluate different processes, materials (FZ or MCz), design aspects (slim edge, width/pitch variations, inter-strip insulation)
• Market survey
• Radiation qualification

Front-end ASICs:
• Good progresses on $p_T$ module ASICs
• Different prototypes for 2S module ASICs already available, new version submissions expected in 2016
• PS ASICs under development, test on prototypes ongoing and new designs in progress

Modules:
• Beam test in the summer on irradiated 2S prototype 2xCBC
• Beam test in autumn on unirradiated 2S full-size module

Tracker Layout:
• Study of different Outer Tracker geometries using the tkLayout simulation tool, for example tilting PS modules in the barrel as a function of $\eta$
Level 1 Tracking and Performances
Level 1 Tracking for Phase-2

**Extreme challenge:** reconstruct $O(100)$ tracks from $\sim 15000$ stubs at 40 MHz

**Associative Memories**
Track matching with a $10^8$ pattern database (custom processor)

Fitting method: PCA, Hough transform or Retina

Slices: $48 = 8 \times 6 \ (\phi \times \eta)$
MUX Time: Load balancing

**Time Multiplexed Trigger**
Multiple detectors send data to a single destination for complete event processing

Fitting method: under study

Slices: $5 = 5 \times 1 \ (\phi \times \eta)$
MUX Time: 24 Bunch Crossing

**Tracklet Algorithm**
Track seeded by finding pairs of stubs in adjacent layers (tracklet)

Fitting method: linearised $\chi^2$

Slices: $28 = 28 \times 1 \ (\phi \times \eta)$
MUX Time: 4 Bunch Crossing
L1-Tracking Performances

Good track-parameter resolutions obtained by L1-tracking simulation, here using tracklet algorithm (similar figures for Associative Memories)
L1-Tracking Perspectives

Next steps:
• Preparing demonstrators in one-two years
• Firmware for data sourcing preparation in progress

Associative Memories:
• Production of AM chip and mezzanine prototypes in progress
• Before AM chip arrival, AM functionality will be tested on FPGA (already implemented)
• Optimisation of the AM pattern bank ongoing
• Simulation of different track fitting methods ongoing

Time Multiplexed Trigger:
• Implementation feasibility of track finding algorithm under study
• MP7 demonstrator in preparation for first proof of concept (by August)

Tracklet Algorithm:
• Improving electron tracking efficiency
• Study of the barrel-endcap transition region
• Study of fake rate

See talk of Prof. Geoff Hall, posters of Dr. Giacomo Fedi and Davide Cieri
Phase-2 Tracker Performances

Track seed from pixel detector, seeds from $p_T$ modules not considered: **Improvements expected!**
Summary

- **Phase-2 Tracker Key Features to Address Physics Challenges**
  - $\eta$ coverage extended from 2.4 to ~4
  - Transverse momentum resolution increased
  - Level 1 tracking

- **Pixel Detector**
  - Being defined, very challenging
  - Pixel size under discussion
  - Front-end development by RD53
  - Radiation damage studies on sensors and electronics in progress
  - Thin planar and 3D sensor submissions foreseen this year

- **Outer Tracker**
  - Irradiated 2S prototypes at beam test in summer
  - PS prototypes will be available soon
  - Layout configuration almost defined; detailed simulations ongoing

- **Level 1 Tracking**
  - 3 R&D strands:
    - Associative Memories
    - Time Multiplexed Trigger
    - Tracklet Algorithm
  - Good efficiency and transverse momentum resolution obtained with simulations
  - Hardware demonstrators under study
Backup
Compact Muon Solenoid

Superconducting Coil, 4 Tesla

CALORIMETERS
- ECAL 76k scintillating PbWO4 crystals
- HCAL Plastic scintillator/brass sandwich

IRON YOKE

TRACKER Pixels
Silicon Microstrips
210 m² of silicon sensors
9.6 M channels

Total weight: 12500 t
Overall diameter: 15 m
Overall length: 21.6 m

2900 scientists from
182 Institutes from
38 countries

MUON BARREL
Drift Tube Chambers (DT)
Resistive Plate Chambers (RPC)

MUON ENDCAPs
- Cathode Strip Chambers (CSC)
- Resistive Plate Chambers (RPC)
Current Outer Tracker

Volume: 24.4 m³
Strip length 10 cm (innermost) to 20 cm (outermost)
Strip pitches 80 μm (innermost) to 205 μm (outermost)
Qualified up to $2.1 \times 10^{14}$ n$_{eq}$/cm$^2$

Readout chip:
APV25 (0.25 μm IBM CMOS)
128 Channels
Qualified up to 50 Mrad
Phase-1 Pixel detector

• The Phase-1 pixel detector is an improved version of the current pixel detector
• 4 layer / 3+3 disks (100×150 μm², n-in-n): improved track resolution and efficiency
• New readout chip: reduced dynamic inefficiency at high rate and PU
• Reduced material: CO₂ cooling, new cabling and DC-DC powering scheme
• It will be installed during the 2016 Technical Stop; a pilot disk 3 blade is already installed for testing
## The LHC Timeline

<table>
<thead>
<tr>
<th>E</th>
<th>Run 1</th>
<th>Run 2</th>
<th>Run 3</th>
<th>HL-LHC</th>
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<tr>
<td>7-8</td>
<td>7 x 10</td>
<td>2 x 10</td>
<td>2 x 10</td>
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<tr>
<td>L (cm)</td>
<td>LS 1</td>
<td>LS 2</td>
<td>LS 2</td>
<td>LS 3</td>
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### HL-LHC environment:
- Upgrade of low-β triplets and installation of crab-cavities to optimise bunch overlaps
- $L_{\text{inst}} = 5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1} \approx 10 \text{ times Run 1} \rightarrow L_{\text{tot}} \sim 3000 \text{ fb}^{-1}$ in 10 years
- Bunch crossing (BX) 25 ns (double BX rate of Run 1)
- Pile Up (PU) $\sim 140 \approx 6 \text{ times Run 1}$

**We are here**

Installation of the **new CMS Phase-1 pixel detector** during extended winter shut-down

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Limitation of the Current Tracker

Phase-2 pixel tracker requirements with respect to the Phase-1

- Hit rate ~5 times larger
- Radiation dose ~3 times larger
- Radiation fluence ~10 times larger

Phase-2 outer tracker requirements with respect to the Phase-1

- Radiation dose ~6 times larger
- Trigger information needed

Tracking degradation:

- Impact parameter degradation > 50% after 500 fb⁻¹
- Data loss of ~7% at PU = 140
- Muon and calorimeter-based Level 1 (L1) trigger will not withstand the rates due to Pile-Up (PU) and limited resolution
HL-LHC CMS Upgrade

NEW TRACKER
Radiation tolerant - high granularity - less material
Tracks in hardware trigger (L1)
Coverage up to $\eta \sim 4$

ECAL Barrel
Replace FE electronics

New Endcap Calorimeters
Radiation tolerant - high granularity
Investigate coverage up to $\eta \sim 4$

TRIGGER/DAQ
L1 (hardware) with tracks and rate up to 500 kHz to 1 MHz
Latency $\geq 10$ µs
HLT output up to 10 kHz

MUON
Replace DT FE electronics
Complete RPC coverage in forward region (new GEM/RPC technology)
Investigate Muon-tagging up to $\eta \sim 4$
Alternative Outer Tracker Layout
DAQ Concept

### TRIG: (stubs) [40MHz]
- **Data Trigger & Control**
  - μTCA board

### DAQ: full data [500kHz-1MHz]
- Reduced data
- ~<stubs/mod/BX>
Stub Rate

Cluster over stub multiplicity - barrel

Cluster over stub multiplicity - endcap

Stub rate - barrel

Stub rate - endcap
L1 Track Fitting

**RETINA**

- Principal Component Analysis (PCA)
  - Orthogonal linear transformation of variables in a new cartesian coordinate system in which variable with maximum variance is projected on the first axis, second maximum variance on second axis and so on. Algorithm can be implemented efficiently on FPGA.

**Hough transformation**

- In a real space there are $\infty$ circle passing by a points and the axis origin. Circle center lies on a straight line in the Hough Space.

- Hits lying on a circle will correspond to lines meeting at the same point in the Hough Space.

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[Nicola Neri, TREDI 2015]
CO₂ Cooling

Advantages of CO₂:
- Large latent heat
- Low viscosity
- Very small pipes → Low mass
- Cheaper than fluorocarbon refrigerant
- Low impact on environment

CO₂ cooling foreseen for Phase-1 upgrade
The technology in principle allows scaling to full tracker (between 5× and 10× w.r.t. pixel)
Phase-2 Tracker Performances

Obtained with the **Phase-1 CMS track reconstruction**:
Track seed from pixel detector, seeds from $p_T$ modules not considered:
**Improvements expected!**

- CMS Phase-1
- CMS Phase-2