Research and Development for a Free-Running Readout System for the ATLAS LAr Calorimeters at the High Luminosity LHC

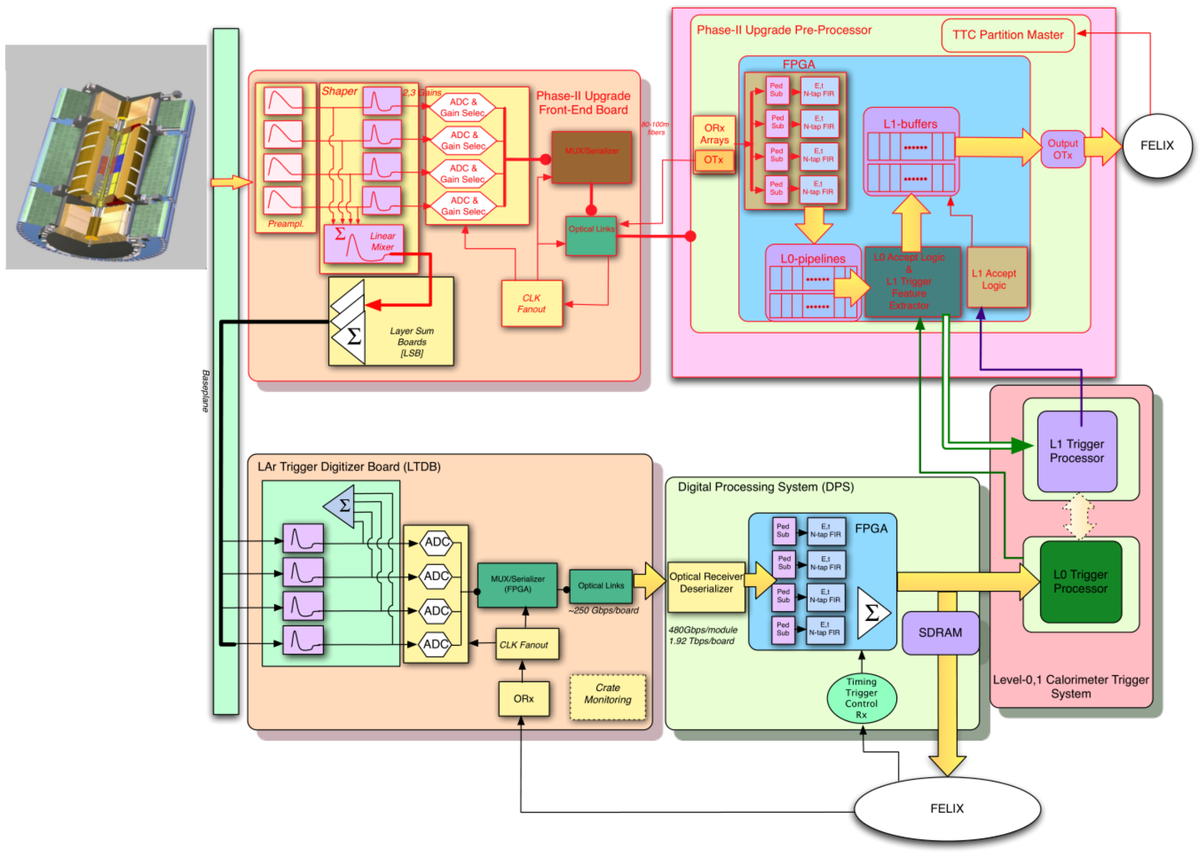
M. Hils on behalf of the ATLAS Liquid Argon Calorimeter group – maximilian.hils@tu-dresden.de

Motivation

For 2024 an upgrade of the Large Hadron Collider (LHC) is planned which forsees a further increase in luminosity. During the so-called high luminosity phase of the LHC (HL-LHC) integrated and instantaneous luminosities of 3000 fb^{-1} and 7×10^{34} cm^{-2} s^{-1} are assumed. The ATLAS detector [1] is planned to be operated with Level-0 and Level-1 trigger accept rates of 1 MHz and 400 kHz and trigger latencies of 6 µs and 30 µs, respectively. These conditions will bring the current read-out electronics of the ATLAS liquid-argon (LAr) calorimeter system beyond their design specifications. A complete replacement of the LAr Calorimeter front-end and back-end electronics is therefore foreseen which provides larger data buffers, a high-bandwidth data transmission and an improved radiation tolerance of the front-end components.

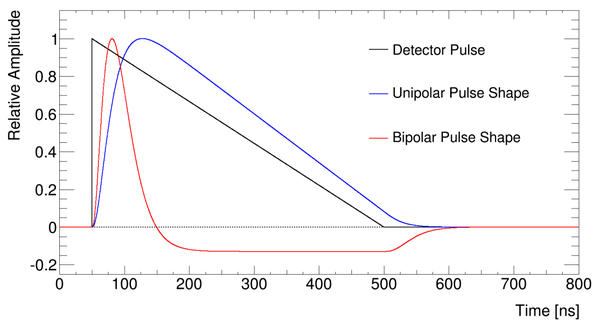
Architecture of the Phase-II Readout System

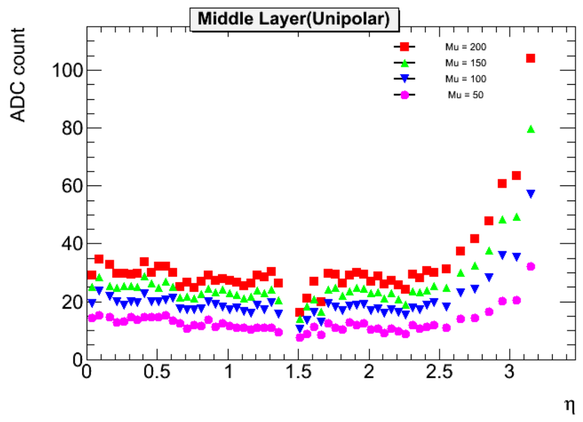
The figure below shows an overview of the Phase-II front-end and back-end electronics.



Pulse Shapes

An optimisation of the pulse shaping scheme is investigated. Simulations with an unipolar pulse shape instead of the currently used bipolar pulse shape show that this would not lead to a „run-away“ of the baseline due to signal pile-up.





Radiation Tolerance Criteria

Since the front-end electronics of the LAr calorimeters are located on the calorimeter cryostats they are subject to significant radiation exposure. The radiation tolerance criteria for the HL-LHC including safety factors are listed in the table below [2]. The numbers in the brackets are the safety factors which account for simulation uncertainties and variations in the production process.

	TID (kGy)		NIEL (n_{eq}/cm^2)		SEE (h/cm^2)	
ASICs (current, 1000 fb^{-1})	0.58	(5.25)	1.7×10^{13}	(5)	3.2×10^{12}	(5)
ASICs (Phase-II, 3000 fb^{-1})	1.74	(5.25)	5.0×10^{13}	(5)	9.6×10^{12}	(5)
COTS (single-lot)	5.7	(17.5)	5.0×10^{13}	(5)	9.6×10^{12}	(5)
Powering ASICs (EM barrel and endcap)	0.1	(5.25)	5.8×10^{12}	(5)	1.5×10^{12}	(5)

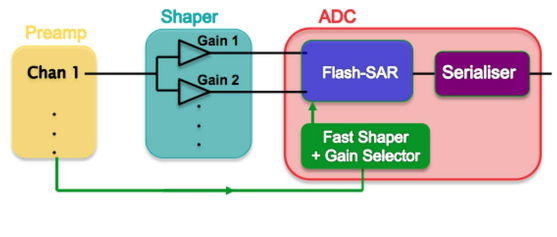
Design Parameters for Middle Layer Electronics

Beside the radiation tolerance, there are several other design parameters which should be met by the new electronics. In order to capture the expected range of deposited energies per calorimeter cell, a dynamic range of 16.25 bits per channel is required. The maximum input current per channel is about 10 mA and the noise should therefore not exceed 100 nA. Cooling capabilities require the power per channel to be less than 50 mW. Furthermore, the serializer and optical transmitter should provide a data rate of at least 9 Gb/s per fiber excluding packaging and forward error corrections.

Technologies under investigation

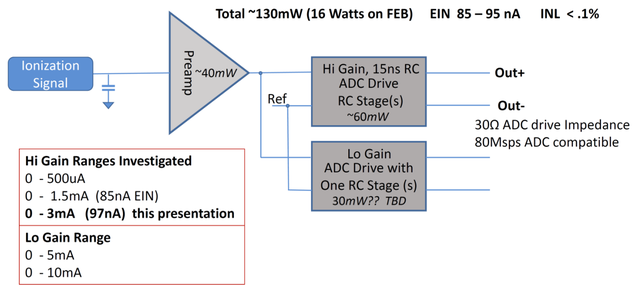
The table below gives a summary of two different technolgies under investigation which include 65 nm CMOS and 180 nm SiGe technologies. The goal is to use a single technology for the pre-amplifier, shaper and ADC, in order to reduce power and complexity of the system. A gain selection may be applied on the digital data in the back-end processing.

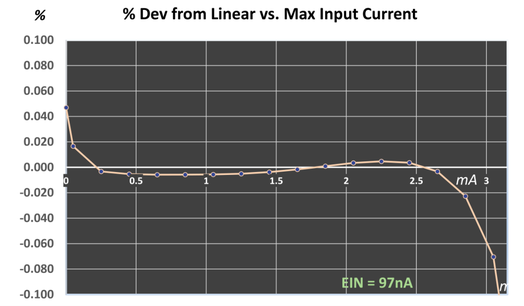
	Plan I	Plan II
Gain Segmentation	4 scale	2 scale
ADC Resolution	10 / 12 bits	14 bits
Sample Rate	40 / 80 MS/s	40 / 80 MS/s
Technology	CMOS	SiGe + CMOS



180 nm SiGe technology

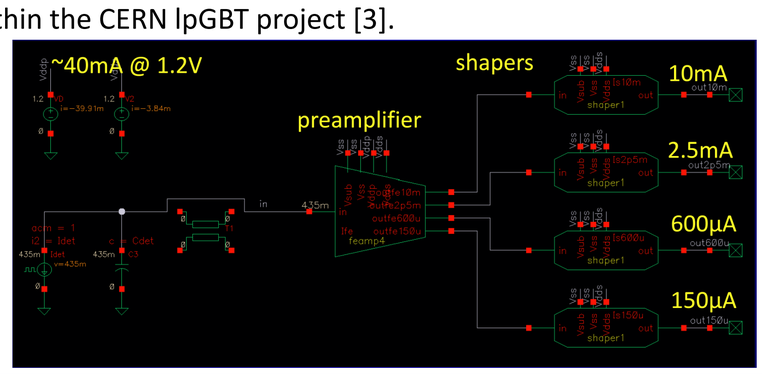
A design study in 180 nm SiGe technology shows that 2 gain stages combined with 14-bit ADCs fulfill the requirements on noise, dynamic range and radiation tolerance. A programmable shaping furthermore allows a better pile-up mitigation.





65 nm CMOS technology

The benefits of a smaller feature size are reduced power consumption and improved radiation robustness. An example layout in 65 nm CMOS technology implements 10-bit ADCs and four gain stages, but other designs are possible. The 65 nm technology would allow an integration with the serializer and optical link components, which are also foreseen to be developed in this technology within the CERN lpGBT project [3].



Back-End Electronics

The back-end Pre-processor system will apply digital filter algorithms for energy reconstruction and will prepare the input to the Level-1 trigger system and the data acquisition. The FPGA-based processing boards will be an evolution of the currently developed LAr Digitial Processing System (LDPS) [4], for which a demonstrator board is shown below.

	Phase I LDPS	Phase II Pre-processor
# or channels	34,000	183,000
ADC number of bits	12	12-14 + gain bits
Sampling rate	40 MHz	40-80 MHz
Rate from front-end	25 Tb/s	200-300 Tb/s
Fiber speed from front-end	5.4 Gb/s	10 Gb/s
Channels per FPGA	320	380-640
Input per FPGA	205 Gb/s	400-800 Gb/s
Output per FPGA	280 Gb/s	>30 Gb/s

References:
[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3 (2008) S08003
[2] ATLAS Collaboration, *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*, CERN-LHCC-2012-022
[3] Paulo Moreira, *GBT Project: Present & Future*, ACES 2014 - Fourth Common ATLAS CMS Electronics Workshop for LHC Upgrades, CERN 2014
[4] ATLAS Collaboration, *ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report*, CERN-LHCC-2013-017

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