ScalTech28

INFN Proposal (Gr. 5)

Piero Malcovati, Marco Grassi

Low-power rad-hard circuit design in scaled technologies

Outline

… send some scouts in advance

- The problem
- The proposed research project
  - Technology choice (28nm)
  - Project participant
    - Responsible
    - Partners
  - Technical activity
  - Milestone & Deliverables
  - Budget
  - PV Activity

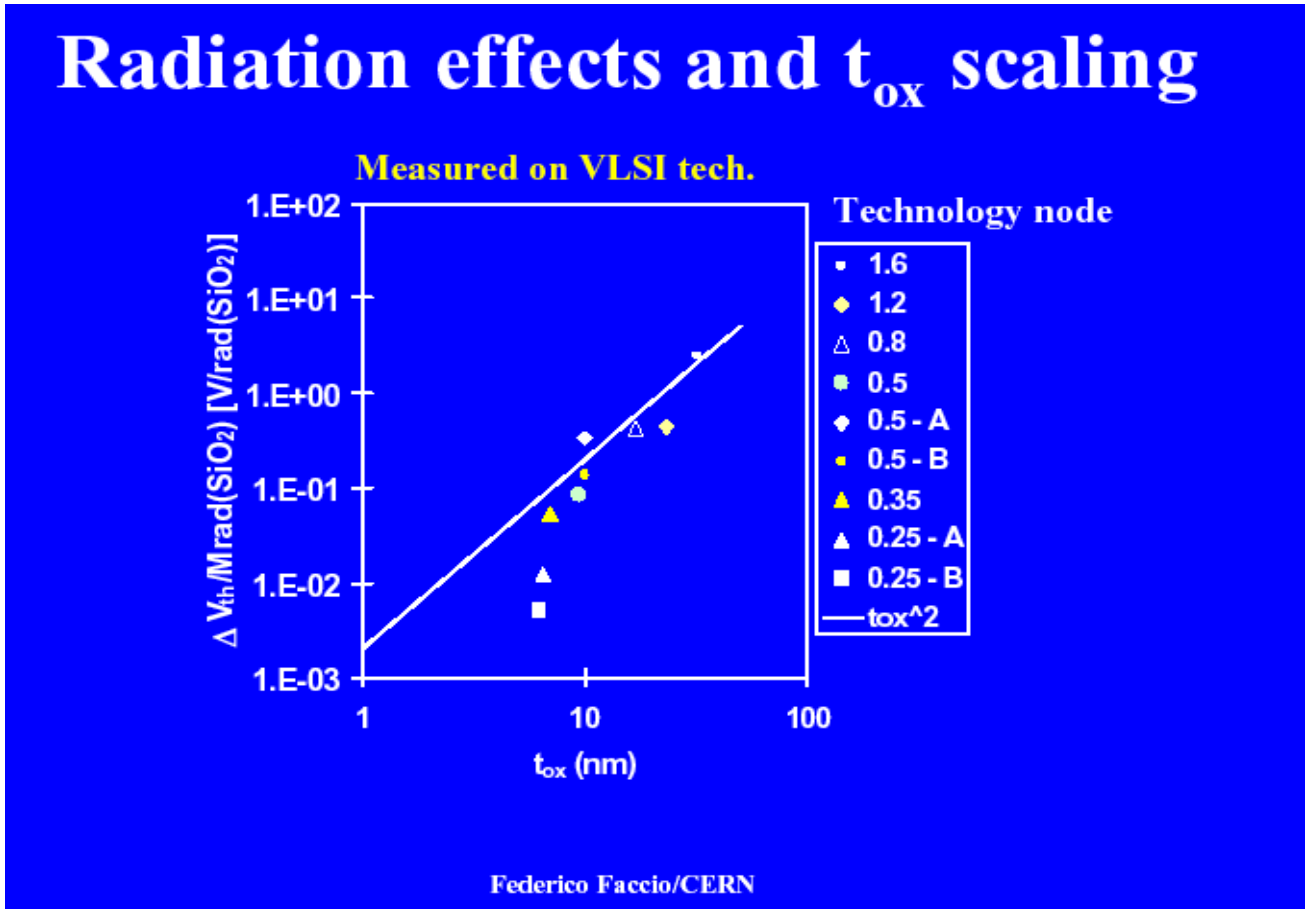
The problem

- Future Experiments read-out will have to face two key problems
  - An extremely large radiation dose
    - Up to 1Grad in 10years
      - Much larger than in any previous situation
  - An extremely large number of channels
    - Increasing power consumption
  - ➔ New electronics has to be designed
    - To guarantee rad-hard performance
    - To reduce power consumption
- Open questions
  - Which technology to be adopted ?
    - Which circuit solutions to be used in scaled technologies ?
      - Circuit solutions depend on adopted technology

The problem

Radiation damage vs. Technology node

- Radiation damage effects reduce with oxide thickness
  - ➔ with technology scaling



Saks, IEEE Trans. on Nucl Science, 1984

- ➔ ***Technology scaling helps Radiation Hardness***

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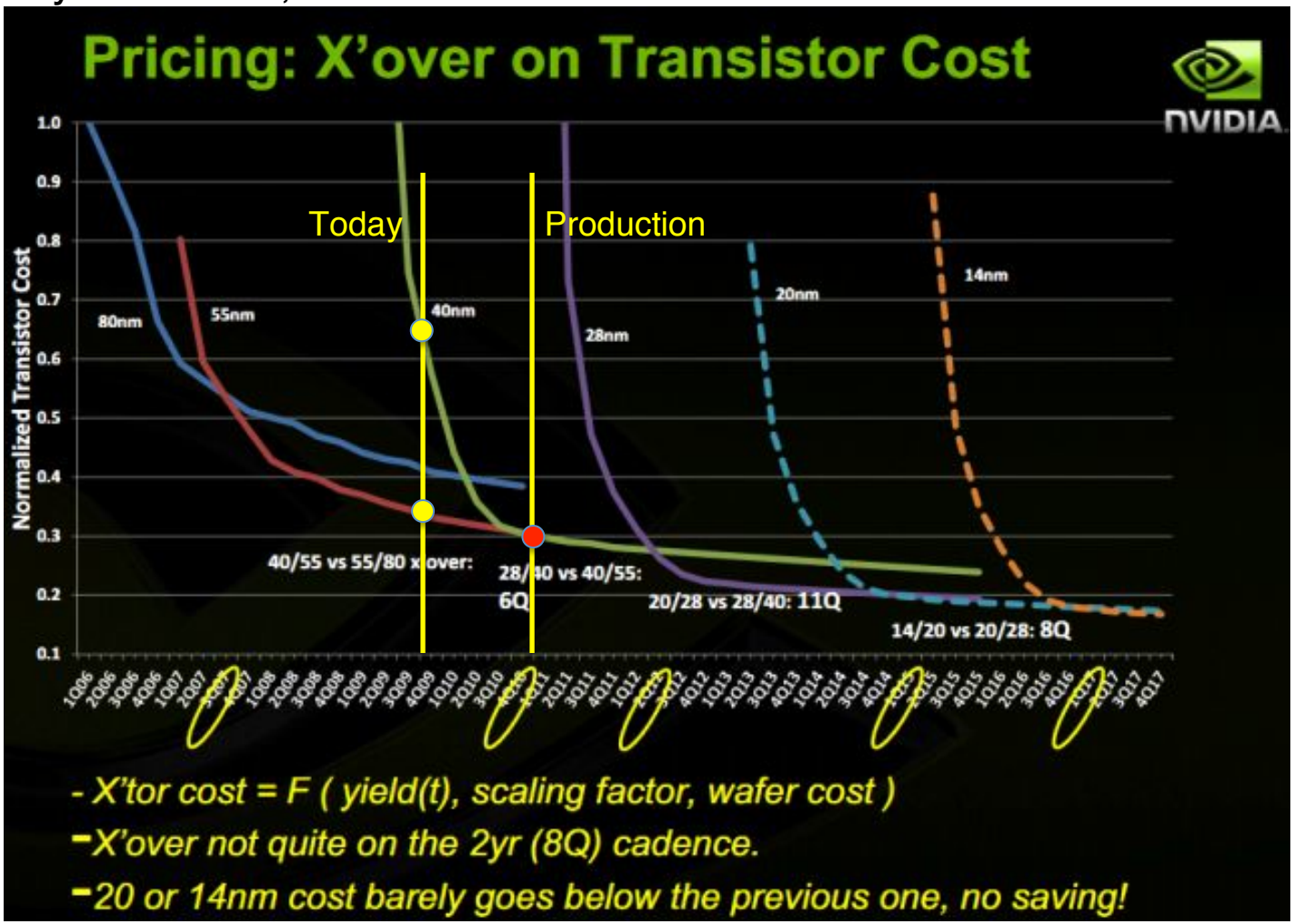
The technical proposal – ScalTech cost & access

- Technology cost
  - In few years 65nm, 45nm and 28nm costs will be the same



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The technical proposal

ScalTech cost & access

- EUROPRACTICE (IMEC)
  - delivers 45nm-TSMC prototypes
  - does not allow 28nm opan access
  - **BUT**
  - **Selected "Pilot sites"** can access to **28nm** for key project with final prototyping
  - **Baschirotto@MiBicocca** selected as **"Pilot site"**

Leuven, 4 June 2013

Dear prof. Baschirotto

I am here to communicate you that in consideration of the research activity proposal you sent us and your outstanding experience in the design of mixed-signal and RF integrated circuits in scaled technologies, we have decide to allow you the access to the TSMC 28nm technology.

This access will be allowed only to few outstanding sites in Europe and to your site among them.

The necessary administrative procedure has to be completed as we will communicate to you later on.

Best regards

Carl Das
Director ASIC services

IMEC

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The technical proposal – The coordinator (Short CV)

- Associate Professor @ Univ. of Milan-Bicocca (Italy)
  - Responsible of the Microelectronics Group (2 post-doc, 6PhD, etc…)
  - Responsible of several research projects
    - 2x PRIN, Regional, etc….
- >24 years experience in microelectronics for teaching, researching, and industrial design
  - Collaboration with several companies and research institutions
    - IMEC, Astri, CERN (L3, etc…), Infineon, Chipidea, ReadyTrace, STMicroelectronics, Accent, Conexant, Marvell, Ublox, etc.
- > 400 scientific publications
- 36 USA patents
- Member of the Technical Program Committee of several international conferences (AACD, ISSCC, ESSCIRC, DATE, etc.)
- IEEE SSCS Distinguished Lecturer
- IEEE Fellow

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The technical proposal

- Basic question ??
  - What is the best tech-node for future implementations in terms of
    - Radiation hardness to 1Grad
    - Low-power consumption
    - Technology access (availability, cost, etc..)

- **Proposal activity**
  - Select an advanced tech-node ➔ 28nm
  - Study radiation damage effects (**WP2**)
  - Design *few significant blocks* in 28nm Scaled Technology (**WP3-&-WP4**)
    - Rad-hard (RH) & Low-power (LP) - & - High-speed
  - Compare the achieved results with similar activities in different nodes
    - ➔ Take the best technology node choice for final production
  - Develop a simulation environment for circuit with radiation damaged devices (**WP5**)

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The technical proposal – Blocks & Specs

- Single devices
  - MOS (different sizes)
  - Passive (Capacitors and resistors)
- Complete blocks
  - Analog read-out Front-End (AFE)
  - Mixed-Signal/Digital (ADC)
  - Optical link (TIA)

- To have a *fair comparison* of achieved performance in different tech-nodes
  - ➔ Target specs defined in parallel to other running activities in different tech-nodes
    - Benchmark circuits
      - **AFE** ➔ Low-power ➔ RD35/Chipix65
      - **ADC** ➔ High accuracy ➔ PIXFEL
      - Optical link - **TIA** ➔ High-speed ➔ GB-TIA link

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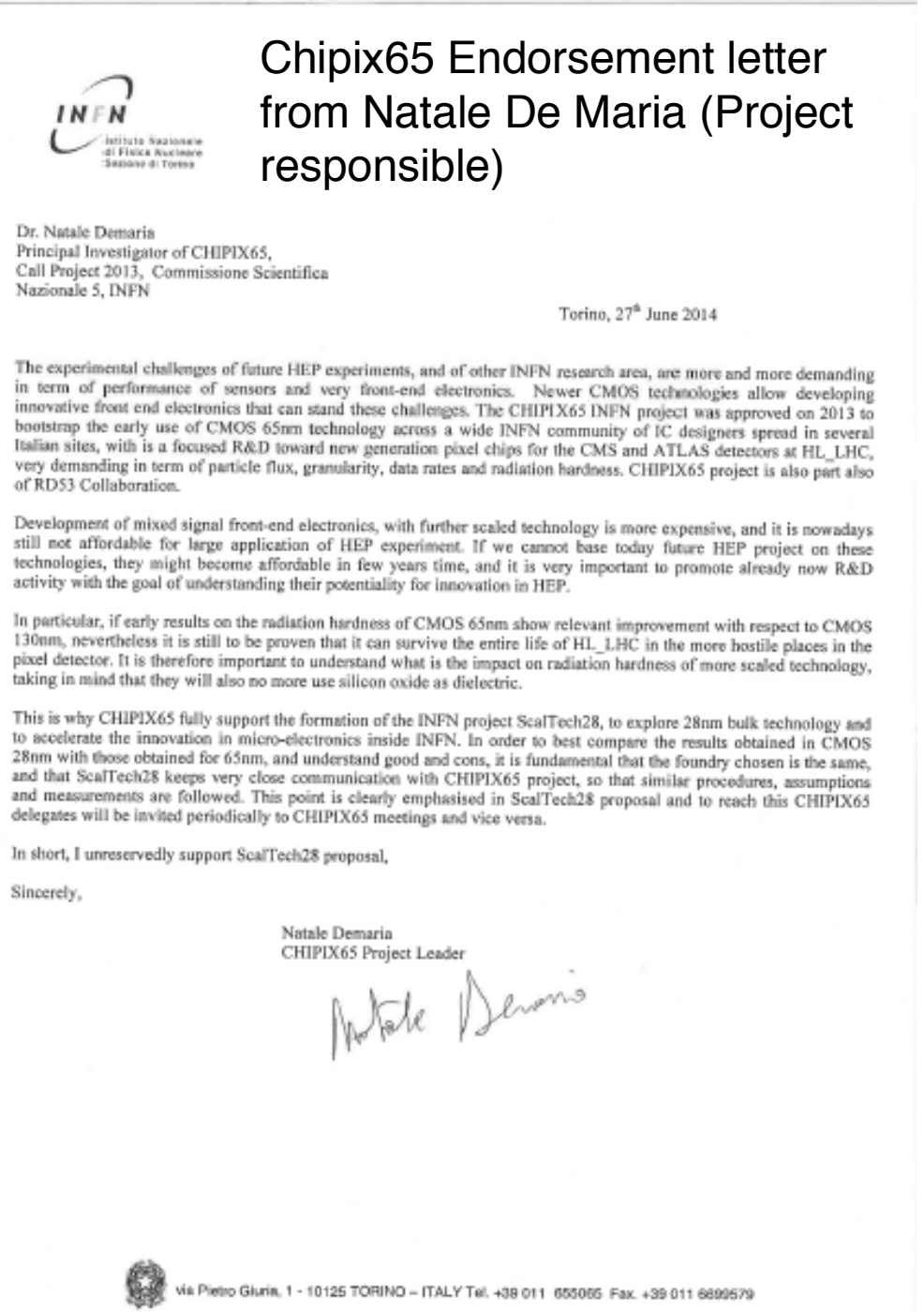
Interaction with running projects

- RD53, Chipix65, PIXFEL, GBT
  - No activity duplication
    - Same target specification
    - Same silicon foundry (TSMC)
    - Share arrangements
      - eventual design solutions
      - layout solutions

Chipix65 Endorsement letter from Natale De Maria (Project responsible)



Dr. Natale Demaria
Principal Investigator of CHIPIX65,
Call Project 2013, Commissione Scientifica
Nazionale 5, INFN

Torino, 27th June 2014

The experimental challenges of future HEP experiments, and of other INFN research area, are more and more demanding in term of performance of sensors and very front-end electronics. Newer CMOS technologies allow developing innovative front end electronics that can stand these challenges. The CHIPIX65 INFN project was approved on 2013 to bootstrap the early use of CMOS 65nm technology across a wide INFN community of IC designers spread in several Italian sites, with is a focused R&D toward new generation pixel chips for the CMS and ATLAS detectors at HL_LHC, very demanding in term of particle flux, granularity, data rates and radiation hardness. CHIPIX65 project is also part also of RD53 Collaboration.

Development of mixed signal front-end electronics, with further scaled technology is more expensive, and it is nowadays still not affordable for large application of HEP experiment. If we cannot base today future HEP project on these technologies, they might become affordable in few years time, and it is very important to promote already now R&D activity with the goal of understanding their potentiality for innovation in HEP.

In particular, if early results on the radiation hardness of CMOS 65nm show relevant improvement with respect to CMOS 130nm, nevertheless it is still to be proven that it can survive the entire life of HL_LHC in the more hostile places in the pixel detector. It is therefore important to understand what is the impact on radiation hardness of more scaled technology, taking in mind that they will also no more use silicon oxide as dielectric.

This is why CHIPIX65 fully support the formation of the INFN project ScalTech28, to explore 28nm bulk technology and to accelerate the innovation in micro-electronics inside INFN. In order to best compare the results obtained in CMOS 28nm with those obtained for 65nm, and understand good and cons, it is fundamental that the foundry chosen is the same, and that ScalTech28 keeps very close communication with CHIPIX65 project, so that similar procedures, assumptions and measurements are followed. This point is clearly emphasised in ScalTech28 proposal and to reach this CHIPIX65 delegates will be invited periodically to CHIPIX65 meetings and vice versa.

In short, I unreservedly support ScalTech28 proposal,

Sincerely,

Natale Demaria
CHIPIX65 Project Leader

via Pietro Giuria, 1 - 10125 TORINO – ITALY Tel. +39 011 655065 Fax. +39 011 6699579

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The technical proposal – The Research Partners

- ScalTech28 (INFN Founded project)
  - **INFN-MiB (Baschirotto)** with ***Alessandro Marchioro (CERN)*** support
    - Project coordination
    - Prototype run coordination
    - Rad-Hard LP-AFE design
    - Optical link GBT-TIA design
  - **INFN-PD (Bisello)**
    - Prototype radiation
    - Radiation damage measurement
  - **INFN-PV (Malcovati)**
    - Rad-Hard ADC design
- **EPFL-Neuchatel (Enz)** – Founded by Swiss NFS
  - BSIM6 model of irradiated devices for simulations

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The technical proposal – Manpower (2-year activity)

Unit			Name	Title	% in ScalTech28	FTE	Total FTE
1	INFN	Milan-Bicocca	BASCHIROTTO Andrea	Associate Professor	50%		
1		Milan-Bicocca	DE MATTEIS Marcello	Research Fellowship	40%		
1		Milan-Bicocca	PEZZOTTA Alessandro	PhD student	30%		
1		Milan-Bicocca	PIPINO Alessandra	PhD student	80%		
1		Milan-Bicocca	RESTA Federica	PhD student	40%		
1		Milan-Bicocca	VERGINE Tommaso	PhD student	80%	3.20	
2		Padova	BISELLO Dario	Full professor	10%		
2		Padova	PACCAGNELLA Alessandro	Full Professor	20%		
2		Padova	CANDELORI Andrea	INFN Associate	20%		
2		Padova	WYSS Jeffery	Associate Professor	30%		
2		Padova	DING Lili	Research Fellowship	40%		
2		Padova	SILVESTRIN Luca	Research Fellowship	30%	1.50	
3		Pavia	MALCOVATI Piero	Associate Professor	40%		
3		Pavia	GRASSI Marco	Research Fellowship	40%		
3		Pavia	DE BERTI Claudio	PhD student	100%	1.80	**6.50**
4	External	CERN	MARCHIORO Alessandro		20%	0.20	
5		EPFL	ENZ Christian	Full Professor	20%		
5		EPFL	TBD	Post-doc	40%		
5		EPFL	TBD	PhD student	100%	1.60	**1.80**
				Grand Total			**8.30**

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The technical proposal – Project management

Work Package		Leader	Unit
WP1	Project management (including chip integration)	Andrea BASCHIROTTO	Milan-Bicocca
WP2	Radiation Hardness	Dario BISELLO	Padova
WP3	Digital/Mixed-Signal Electronics	Piero MALCOVATI	Pavia
WP4	Analog FE Electronics & Optical Transceiver	Marcello DE MATTEIS	Milan-Bicocca
WP5	Radiation Damage Modeling	Christian ENZ	EPFL

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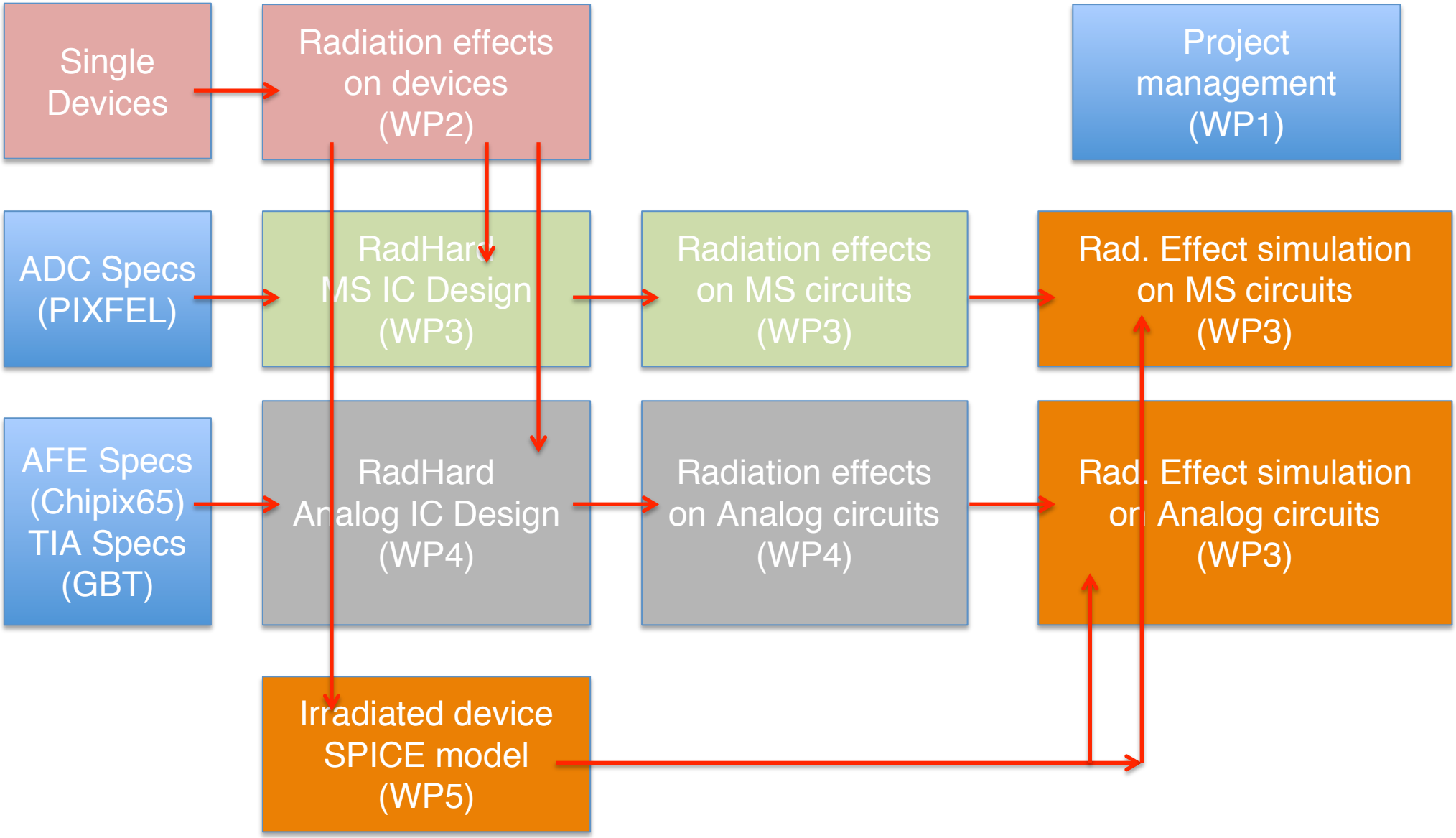
Full project flow-chart



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Activity scheduling – GANTT Chart

- Two-years project

Month	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
INFN-MiB	1	1	1													8	8	8	8	8	8	8	8	8
			4	4	4	4	4	4	4	4	4	9	9	9	9									
	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10									
INFN-PD	1	1	1					3	3	3	6	6	6	6		3	3	3	8	8	8			
INFN-PV			4	4	4	4	4	4	4	4	4	9	9	9	9	8	8	8	8	8	8	8	8	8
EPFL	1	1	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
External Europractice				2	2	2	2					5	5	5	5									

1st prototype Layout	1
1st Silicon Fabrication	2
Prototype irradiation	3
2nd prototype Design&Layout	4
2nd Silicon Fabrication	5
1st Prototype measurement	6
Radiation damage model development	7
2nd Prototype Measurement	8
Board design	9
Optical Transceiver	10

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Milestone & Deliverables

Milestone	Time	Kind	Short description	Participants
01	Month 02	Report	Definition of the simple devices for 1st prototype	All
02	Month 04	PGtape	1st PGtape	MiB
03	Month 07	Report	Definition of the circuit target specification	MiB PV
04	Month 08	Samples	1st PGtape prototype delivery	MiB
05	Month 11	Report	Non-Damaged & Rad-Damaged devices characterization	PD
06	Month 12	Model	Preliminary SPICE Model for the Non-Damaged & Rad-Damaged devices	EPFL
07	Month 13	PGtape	2nd PGtape	MiB
08	Month 18	Samples	2nd PGtape prototype delivery	MiB
09	Month 21	Model	Final SPICE Model for the Non-Damaged & Rad-Damaged devices	EPFL
10	Month 22	Report	Rad-Damaged & Non-Damaged circuits characterization	MiB PD PV
11	Month 23	Report	Simulation vs. measurement for target circuit using developed SPICE Model	EPFL
12	Month 24	Report	Wrap-up report and future prospectives	All

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Detailed Budget (two years activity) – in k€

Type of Cost	2015				2016				Total	Total	
Prototype Fabrication	MiB	PD	PV	Tot	MiB	PD	PV	Tot		**185.0**	**60%**
Prototype fabrication (Europractice charges 100k€ for a single 6mm² miniasic prototype)	80.0	=	=	80.0	80.0	=	=	80.0	160.0		
Prototype packaging	10.0	=	=	10.0	15.0	=	=	15.0	25.0		
Consumables & Services										**66.0**	**22%**
Board for IC testing	2.0	6.0	2.0	10.0	4.5	6.0	2.5	13.0	23.0		
Irradiation Consumables	=	10.0	=	10.0	=	=	=	=	10.0		
External consultancy	8.0	=	=	8.0	25.0	=	=	25.0	33.0		
Instrumentation										**26.0**	**8%**
Consolidation of PC Cluster for verifications and simulations	6.0	=	6.0	12.0	3.0	=	3.0	6.0	18.0		
Software (software to be acquired for the new DK tools)	4.0	=	=	4.0	4.0	=	=	4.0	8.0		
Travels										**33.0**	**10%**
Project meetings	3.5	3.5	3.5	10.5	3.5	3.5	3.5	10.5	21.0		
Conference participations	2.0	2.0	2.0	6.0	2.0	2.0	2.0	6.0	12.0		
Total	**125.5**	**21.5**	**13.5**	**150.5**	**137.0**	**11.5**	**11.0**	**159.5**	**310.0**	**310.0**	**100%**

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PV Activity (WP3) – Mixed-Signal Electronics (SAR ADC)

- M01-M03: Design and layout of test structures (capacitors and resistors)
- M02-M03: Definition of detailed ADC specifications
- M03-M11: ADC design and layout
- M12-M15: Chip Fabrication and test board design
- M15-M18: ADC measurements before irradiation
- M19-M21: ADC measurements after irradiation
- M21-M24: Radiation damaged device models validation through ADC simulation