CHIPIX65

Sviluppo di un pixel chip innovativo in tecnologia CMOS 65nm per altissimi flussi di particelle e radiazione agli esperimenti di HL_LHC e futuri collider di nuova generazione

CALL CSN5 – Responsabile Locale: D. Bisello

Challenges for CHIPIX65

- Design of innovative electronics in strategic area of INFN, using the "novel" CMOS 65nm technology, with a large participation of INFN community

- INFN is one of founding members of RD53, an international collaboration for the R&D phase of an innovative chip for the pixel detectors of ATLAS and CMS at HL_LHC, and the goals of RD53 are the main focus of CHIPIX65 milestones:
  - Small pixels: 50 × 50 μm^2 (or 25x100um^2)
  - Large chips: >2 × 2 cm^2 (~1 billion transistors)
  - Hit rates: ~2 GHz/cm^2
  - Radiation: 1Grad, 10^{16} neu/cm^2 (unprecedented)
  - Trigger: 1MHz, 10 µs (~100× buffering and readout)
  - Low power - Low mass systems

CHIPIX65 CALL Project Proposal 2013 – CSN5

Principal Investigator: L.Demaria

Project Outline (from Project Abstract)

- The goal of this three years project is the development of an innovative **CHIP** for a **PIX**el detector, using the **65**nm CMOS technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. New circuits will be built and characterized, a digital architecture will be developed and eventually a final assembly of a first prototype will be made.
- CHIPIX65 a unique opportunity for an efficient propagation across INFN of 65nm CMOS technology and constitutes the greatest collaboration on a microelectronics project ever made across INFN.

Participant Research Units: Bari, Milano, Padova, Pavia, Perugia, Pisa, Torino

35 members of which 20 are micro-electronics designers. **9.85 FTE**. 6 units involved in CMS, 1 in ATLAS. New members from this year (2 new PhD students)

Work Packages:

- Radiation Hardness – D. Bisello/P. Giubilato (Pd)
- Digital Electronics – R.Beccherle (Pi)
- Analog Electronics - A.Rivetti (To)
- Chip Integration - V.Re (Pv), V.Liberali (Mi)

International Collaborations / supports: RD53, ATLAS, CMS – All wrote support letters

Funding: ~700 kEuro for a three year project, subject to yearly peer review (milestones achieved).

- Mainly consumables and foundry submissions, no man power.

RD53: the international context for CHIPIX65

- ~ 100 members, 19 Institutes (2 new institutes have joined)
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, **Milano**, NIKHEF, New Mexico, Padova, Perugia, Pisa, **Prague IP/FNSPE-CTU**, PSI, RAL, Torino, UC Santa Cruz.
    - 2 institutes requesting to join: LAL/OMEGA, Seville
- Spokes persons: Maurice Garcia-Sciveres, LBNL (ATLAS), Jorgen Christiansen, CERN (CMS) [2 year terms]
- Institute Board (**IB chair: LD, Torino**)
  - Regular IB meetings
  - MOU drafted and ready to be signed
- Management board: Spokes persons, IB chair, WG conveners
  - Monthly meetings
  - **V. Re WG-conver Analogica**
- Technical Working Groups have started
  - WG conveners
  - Regular WG meetings
- First official RD53 collaboration meeting (pre-RD53 meeting in Nov. 2012)
  - CERN April 10-11, 64 participants: https://indico.cern.ch/event/296570

RD53 Global Schedule as today

- 2014:
  - Release of CERN 65nm design kit: Very soon !
  - Detailed understanding of radiation effects in 65nm
    - Radiation test of few alternative technologies (backup solution).
  - IP block responsibilities defined and appearance of first FE and IP designs/prototypes
  - Simulation framework with realistic hit generation and auto-verification.
  - Alternative architectures defined and efforts to simulate and compare these defined
  - Common MPW submission 1: First versions of IP blocks and analog FEs
- 2015:
  - Common MPW submission 2: Near final versions of IP blocks and FEs.
  - Final versions of IP blocks and FEs: Tested prototypes, documentation, simulation, etc.
  - IO interface of pixel chip defined in detail
  - Global architecture defined and extensively simulated
  - Common MPW submission 3: Final IPs and Fes, Small pixel array(s)
- 2016:
  - Common **engineering run**: Full sized pixel array chip.
  - Pixel chip tests, radiation tests, beam tests , ,
- 2017:
  - Separate or common ATLAS – CMS final pixel chip submissions.

Main CHIPIX65 contributions to RD53

- **Radiation WG** (Padova):
  - Irradiation campaign at Legnaro with low energy protons (**TID+TDD studies**)
  - foreseen also irradiation with x-ray machine (**TID studies**)
- **Analog WG** (Pavia, Torino)
  - Design of Very Front end chain, low power, low threshold (<1000e-) with synchronous and asynchronous comparators
- **IP-block WG** (Bari, Milano, Pavia, Padova, Pisa, Torino)
  - **16 out of 34** IP-block under INFN responsibility
- **Simulation WG** (Perugia)
  - Main contributor to the development of the simulation and verification framework
- **Top Level WG**:
  - Activity is at a preliminary stage. Contribution mainly from LBNL (USA)
- **IO WG**:
  - Activity will start during the second half of 2014. New convener being identified now (Roberto Beccherle – Pisa)

CHIPIX65 Milestones

- 2014:
  - **disegno, sottomissione, test di IP blocks analogici e digitali**
  - risultati sull'irraggiamento di strutture diu test di base
- 2015:
  - qualifica radiation hardness della tecnologia
  - design methodology and verification of high dense IC
  - **ottimizzazione architettura digitale:** globale, regionale, della cella pixel
  - **architetture del very front end analogico**
- 2016:
  - integrazione el.analogica nel chip; power distribution, clock distribution
  - primo prototipo chip, con architetettura digitale e readout semplificati

CHIPIX65 2014 submissions

- IP-block submission (2x2 mm^2)- **October 2014**:
  - SLVDS (Pavia)
  - Band-Gap (Pavia, Milano)
  - SRAM (Milano)
  - DAC (Bari)
- Analog Very Front End submission (2x2 mm^2)**- October 2014**
  - Synchronous, Auto-zeroing, FAST ToT analog front end (Torino)
  - Asynchronous analog front end (Pavia)

  Analog readout: max (12x12) pixels + Matrix: (12x32) pixel
- In the pipeline
  - IP blocks:
    - ADC (Bari), Serialiser (Pisa), Digital Logic RadHard (Milano)
  - Pixel-Matrix with complex synthetized digital logic (pixel and readout) [Torino, Pisa, Pavia, Milano]

CHIPIX65 activities for 2015

Details under discussion:

- Test from late 2014 submissions
- IP-block submission:
  - INFN: February and June
  - Shared with RD53: June or October
- Pixel matrix submission:
  - INFN: early summer
  - Shared with RD53: autumn

NB: time-line subject to discussion and to project evolution. For RD53 no precise timing being discussed.

IP Block for RD53

Group		Bari	Pav/ Berg	(Milano)	Padova	Pisa	Torino
ANALOG: Coordination with analog WG							
Temperature sensor.							
Radiation sensor	to be evaluated						O*
Band gap reference	O		O				
MIXED							
8 – 12 bit biasing DAC	O	O					
10 - 12 bit slow ADC for monitoring	O	O					
PLL for clock multiplication	P				P	P	P
High speed serializer (~Gbit/s)	P					P	
(Voltage controlled Oscillator)	x				x	x	x
DIGITAL							
SRAM for pixel region	O			O			
SRAM/FIFO for EOC.	P			P			
DICE storage cell ?	O			O			
LP Clock driver/receiver	P		P				
(Dedicated rad hard digital library)	to be clarified					x	
(compact mini digital library for pixels)	to be clarified					x	
IO: Coordination with IO WG							
Low speed SLVS driver (<100MHz)	O		O			P	P
High speed SLVS driver (~1Gbits/s)	O		O			P	P
SLVS receiver	O		O			P	
POWER							
LDO(s)	P					P	P
SOFT IP: Coordination with IO WG							
Control and command interface	O	P				O*	
Readout interface (E-link ?)	O	P				O*	

Out of 34 IP-block identified in RD53, INFN has proposed to contribute at ~16 of them:

- as main organizer (11)
- as participant (5)

In the following few slides on first prototypes ready for submission in a short time (design in 65nm already present):

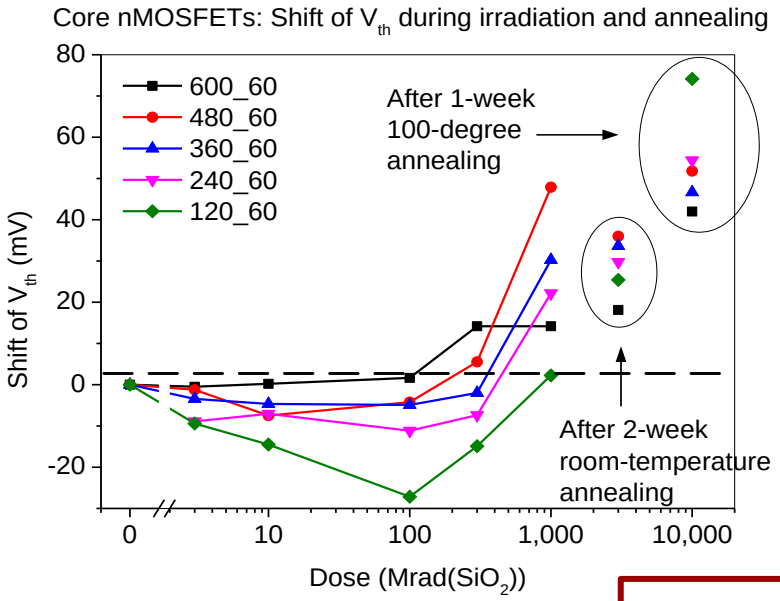
- Band-Gap
- SLVS driver
- SRAM

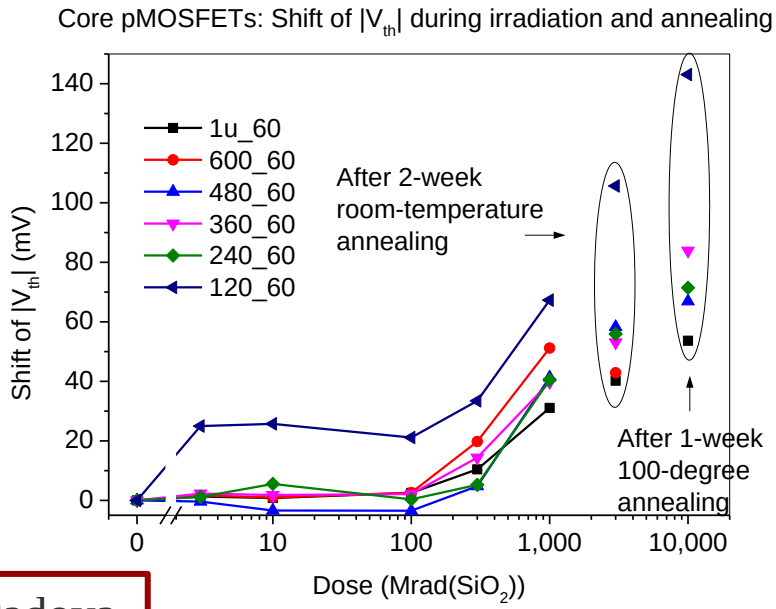
others IP-blocks could be ready for end of year

- serialiser

RD53 WG1 (Radiation test/qualification): ***Summary***

- CERN test structures (65nm nMOS & pMOS transistors)
  - ✓ CERN: 10-keV X ray (CERN), till 200 Mrad(SiO_2)
  - ✓ CPPM: 10-keV X ray (CERN), till 1Grad(SiO_2) , 20 & 100 ºC annealing
  - ✓ Padova: 3-MeV proton (Padova), till 1Grad(SiO_2), 20 & 100 ºC annealing
- TSMC test structures - FNAL layout (65 nm nMOS & pMOS transistors)
  - ✓ Fermilab: Co-60 γ ray, -20 ºC irradiation, till 1Grad(SiO_2)





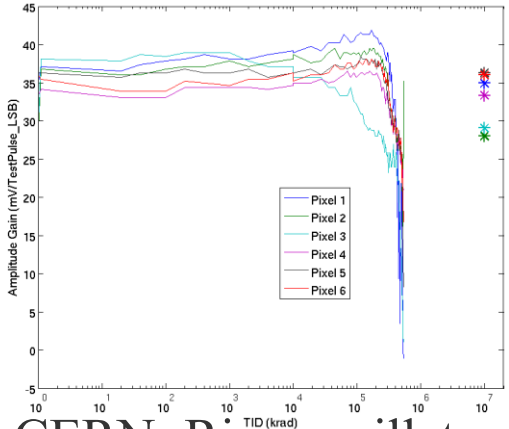
Results from Padova

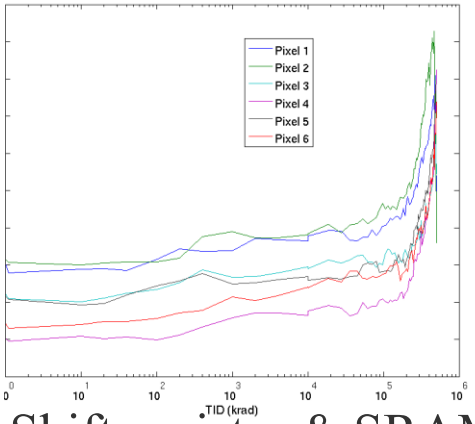
RD53 WG1 (Radiation test/qualification): ***Outlook***

- CERN:
  - ✓ Annealing studies on Ring oscillator & Shift register & SRAM
- CPPM:
  - ✓ New test interface and software. Hardware compatible to low temperature operation at CERN X-ray machine
- Padova:
  - ✓ 10-keV X ray irradiation of 65 nm CERN test structures
  - ✓ Setup of low temperature operation at Padova 3-MeV proton environment
- Fermi lab:
  - ✓ Data analysis and annealing tests of 65 nm transistors (2-week Co-60 γ ray irradiation just finished)
- Others…

RD53 WG1 (Radiation test/qualification): ***Summary***

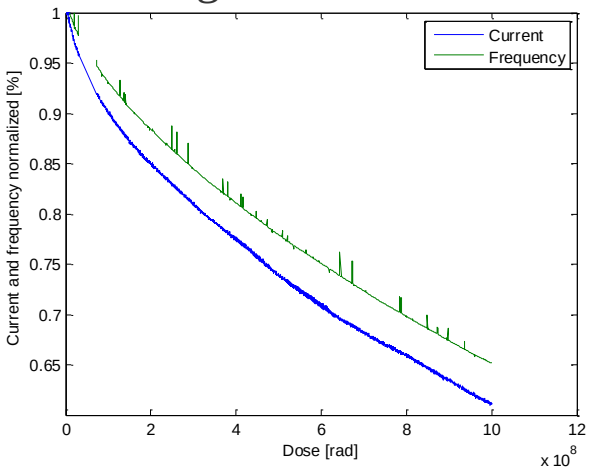
• CERN: pixel detector (to be used as the CLIC vertex detector, 65 nm technology): CERN: 10-keV X ray (CERN), till 1 Grad(SiO_2) , 20 ºC annealing.

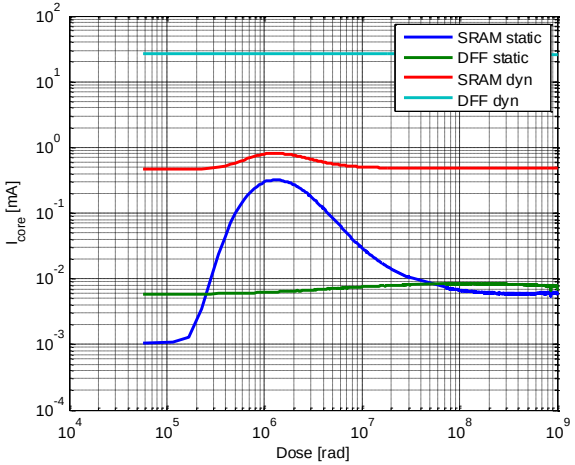




At doses > 200 Mrad(SiO2), severe degradation can be observed. Big variation for front- end gain (left), ToT gain (right) and basic structures (switch, current mirror).

• CERN: Ring oscillator & Shift register & SRAM (65 nm technology): CERN: 10-keV X ray (CERN), till 1 Grad(SiO_2) , 100 ºC annealing.





• Decrease in current and frequency of ring oscillator (left);
• Variation in supply current of other blocks (right).

Padova 2015

- Consumo: **8 keuro**

  Bisello, Candelori

- Paccagnella, Deng: **1.4 FTE**

  Neviani, Vogrig:

- Servizi: **4 m/u LOE**