ALICE-PADOVA Group Meeting

Friday June 6th 2014

09:30 - 11:20	Alice: Analisi dati, SPD, Computing, situazione amministrativa... *1h50'*
11:20 - 11:30	caffe'
11:30 - 13:20	ITS-Upgrade: Physics, Electronics, Mechanics, Cooling,... *1h50'*

People 2014/2015

Ricercatori

Nome	%	M&OA	AFF.		*Note*	Responsabilita' ALICE
RICERCATORI						
F. Antinori	100	1	INFN	Sez. PD	*P. Ric. (al CERN come PjAss)*	Physics Coordinator, MB, EB, PB, CB
D. Caffarri					*CERN da Marzo 2014*	
A. Dainese	80	1	INFN	Sez. PD	*Ric.*	PB, Convener WP1 ITS-Upgrade
D. Fabris	50	1	INFN	Sez. PD	*P. Ric.*	
A. Festanti	100		UniPD	Dott. Fis.	*Dottorando – ultimo anno*	
P. Giubilato	70	1	UniPD	Dip. Fis.	*Ric. Univ.*	Convener WP10 ITS-Upgrade
C. Jena	100	1	UniPD	Dip. Fis.	*Post. Doc. – rinnovo fino a 5/2015*	
M. Lunardon	100	1	UniPD	Dip. Fis.	*Ric. Univ.*	CB (alternate), ITS-IB
S. Mattiazzo			UniPD	Dip. Fis.	*Ass. Senjor - no ass. INFN*	
M. Morando	50	1	UniPD	Dip. Fis.	*P. O.*	
S. Moretto	100	1	UniPD	Dip. Fis.	*Ric. Univ.*	
F. Scarlassara	50	1	UniPD	Dip. Fis.	*Ric. Univ.*	
G. Segato	100		UniPD	Dip. Fis.	*Ric. Univ.*	
F. Soramel	50	1	UniPD	Dip. Fis.	*P.O.*	
C Terrevoli	100	1	UniPD	Dip. Fis.	Assegno biennale da 15/7/2014	
R. Turrisi	100	1	INFN	Sez. PD	*Ric.*	Cooling SPD
G. Viesti	100	1	UniPD	Dip. Fis.	*P.O.*	

Totale: 15 ricercatori (INFN), 12.5 FTE, 13 M&O-A

People 2014/2015

Tecnologi e Tecnici

TECNOLOGI				
D. Del Col	100	UniPD	Dip. Ing. Ind.	Ric. Univ.
A. Francescon	100	UniPD	Dott. Ing. Ind.	Dottorando – ultimo anno
A. Pepato	70	INFN	Sez. PD	D. Tecn.
L. Rossetto	100	UniPD	Dott. Ing. Ind.	P.O.
M. Sgaravatto	20	INFN	Sez. PD	Teconologo
M. Benettoni	40	INFN	Sez. PD	Primo Tecn.
TECNICI				
M. Caldogno	20	UniPD		
D. Pantano	30	UniPD		
S. Martini	100	INFN		

Totale: 6 tecnologi, 4.3 FTE – 3 Tecnici

Financial status 2014

- Account balance at 6/14 (in k€):

Capitolo	assegnato 2014	impegnati 5/6/14	disponibilità
Missioni (ME+MI)	**73.5**	**27.5**	**46** (63%)
Consumo & Trasporti	**27.0**	**2.5***	**24.5** (91%)
TOTALE:	**100.5**	**30**	**70.5**

(*) CERN Team Account: ~ 3k

Budget and Services request for 2015

Budget request

- Richieste **MISSIONI (Estero+Interno)** secondo **schema generale ALICE-Italia** che tiene conto del **numero di FTE ricercatori+tecnologi** (**...**) per physics meetings, partecipazione a turni misura, manutenzione, etc... e responsabilità nella collaborazione (Physics/Technical/Editorial/ Computing/Collaboration Boards, PAGs), riunioni collaborazione italiana, partecipazione Convegno Nazionale Fisica di ALICE) e riunioni TIER2 **+ ITS-Upgrade**
- Richieste **CONSUMO** secondo schema generale ALICE-Italia **+ ITS-Upgrade**

- Request for **ITS-UPGRADE**:
  - Electronics (NI DAQ boards for trasmission tests) **8k**
  - Mechanics (integration tooling production/procurement) **20k**

Budget and Services request for 2015

Services request:

– Ufficio tecnico: ? mesi-uomo per prog. mecc. ITS-Upgrade

– Officina meccanica: 1? mese-uomo per manutenzione impianto raffreddamento SPD e ? m.u. per ITS-Upgrade

– Servizio Calcolo: 1? mese-uomo per manutenzione/upgrade farm ALICE (non-GRID)

– Officina Elettronica: ? mesi-uomo per ITS-Upgrade ????

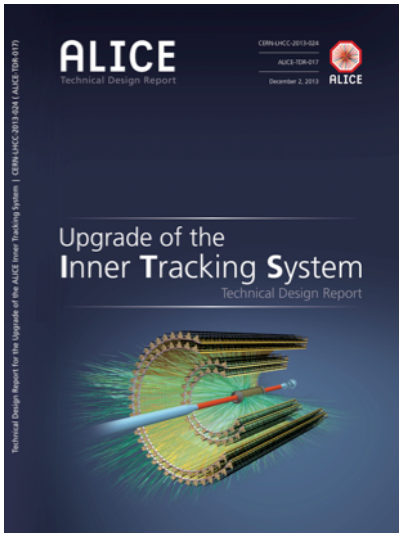
AOB

- bando assegno 2014
- Workshop/Conferenze con partecipazione PD

ITS-UPGRADE STATUS

SLIDES DI VITO MANZARI AL MEETING CON I REFEREE DEL 30/5

Status of the ITS Upgrade Project



LHCC Upgrade Cost Group review → 3 March 2014

Research Board approval → 12 March 2014

Memorandum of Understanding due to the RRB → Ott '14

ITS Upgrade Collaboration

Institute = participated in current ITS

- CERN
- France (Grenoble, Strasbourg)
- Italy (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino)
- Netherlands (Nikhef, Utrecht)
- UK (Daresbury, Liverpool, RAL)
- USA (Austin, Berkeley, Chicago, West Lafayette)

Requests to FAs ~ 97% of total cost

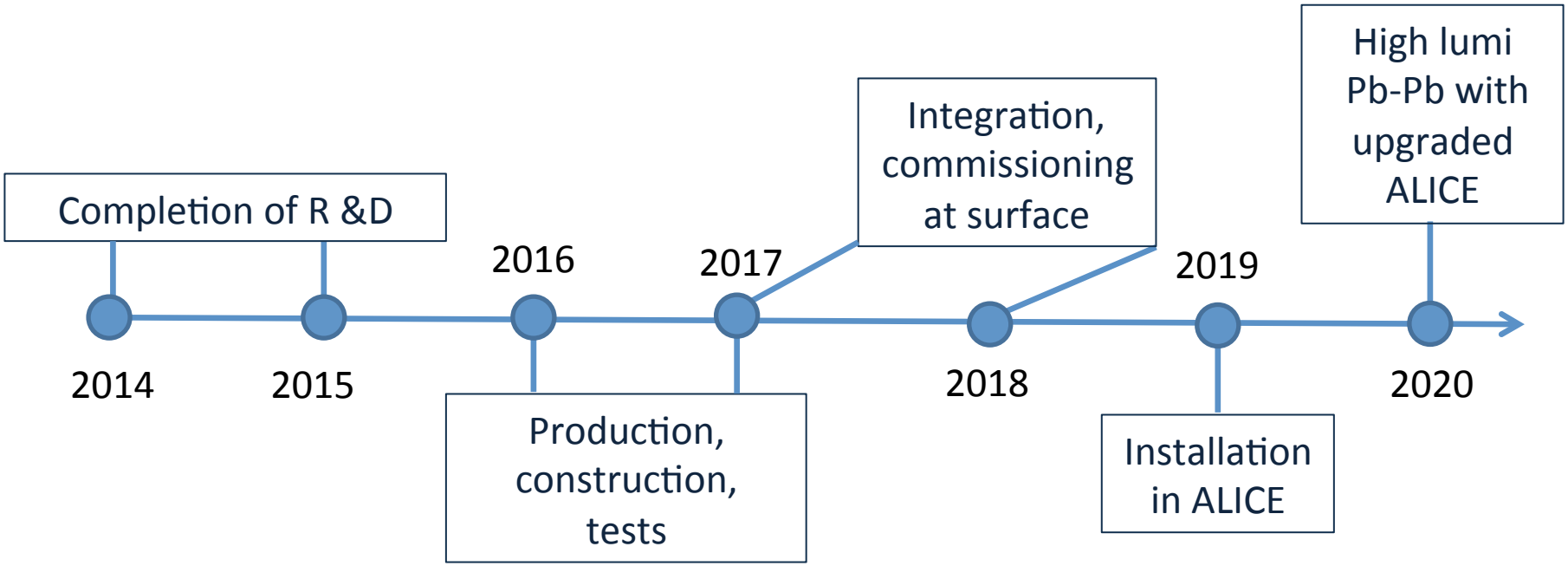
- China (Wuhan): HIC assembly, electronics
- Korea (Pusan, Inha, Yonsei): Pixel chip mass test, HIC assembly
- Thailand (Suranaree, SLRI, TMEC): silicon wafer survey, thinning & dicing
- Pakistan (CIIT-Islamabad): electronics

Requests to FAs ~ 13% of total cost

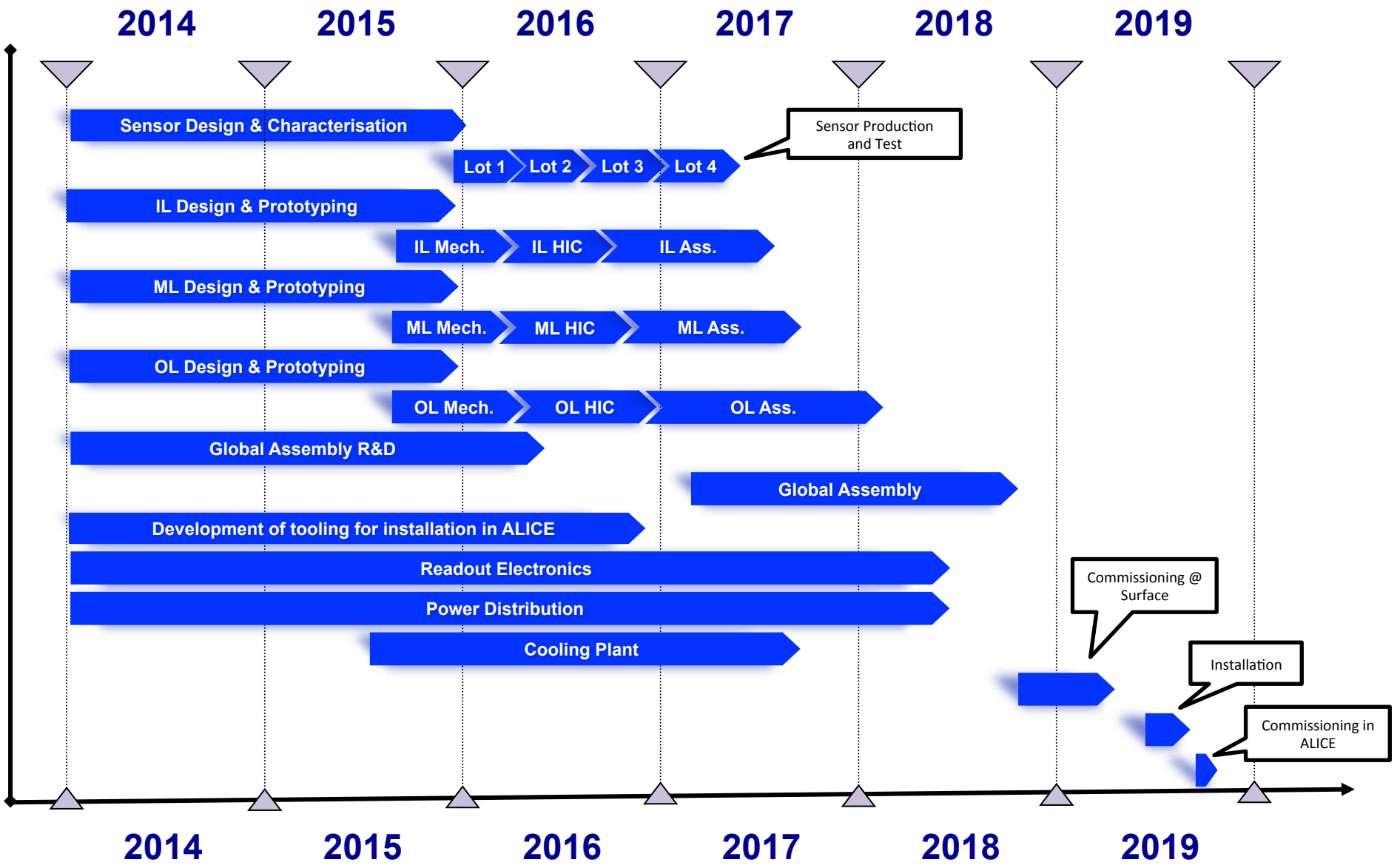
- Russia (St. Petersburg):mechanics (space-frame cold plates)
- Slovakia (Kosice): DCS
- Check Republic (Prague): data transmission, pixel chip mass test
- Ukraine (Kharkov): FPC fabrication (?)

Request to FAs 6% of total cost

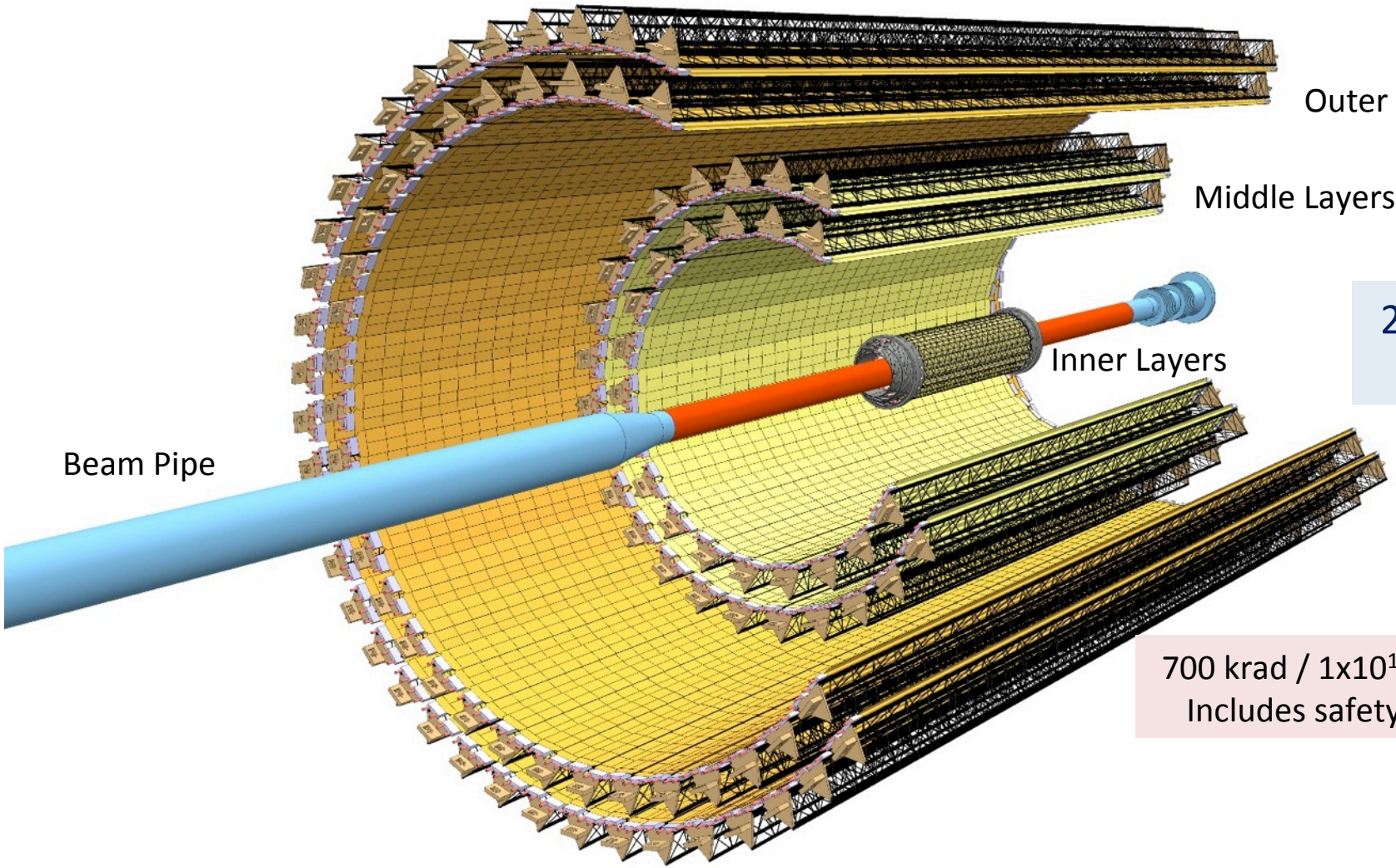
Timeline


Completion of R &D
2014
2015
2016
Production, construction, tests
2017
Integration, commissioning at surface
2018
2019
Installation in ALICE
High lumi Pb-Pb with upgraded ALICE
2020

Schedule


2014
2015
2016
2017
2018
2019
Sensor Design & Characterisation
Lot 1
Lot 2
Lot 3
Lot 4
Sensor Production and Test
IL Design & Prototyping
IL Mech.
IL HIC
IL Ass.
ML Design & Prototyping
ML Mech.
ML HIC
ML Ass.
OL Design & Prototyping
OL Mech.
OL HIC
OL Ass.
Global Assembly R&D
Global Assembly
Development of tooling for installation in ALICE
Readout Electronics
Power Distribution
Cooling Plant
Commissioning @ Surface
Installation
Commissioning in ALICE
2014
2015
2016
2017
2018
2019

The New Inner Tracking System



25G pixels
~10 m^2

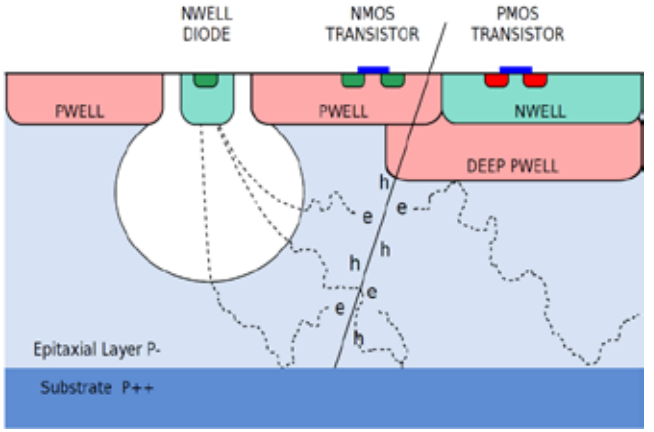
700 krad / $1x10^{13}$ 1 MeV n_{eq}
Includes safety factor 10

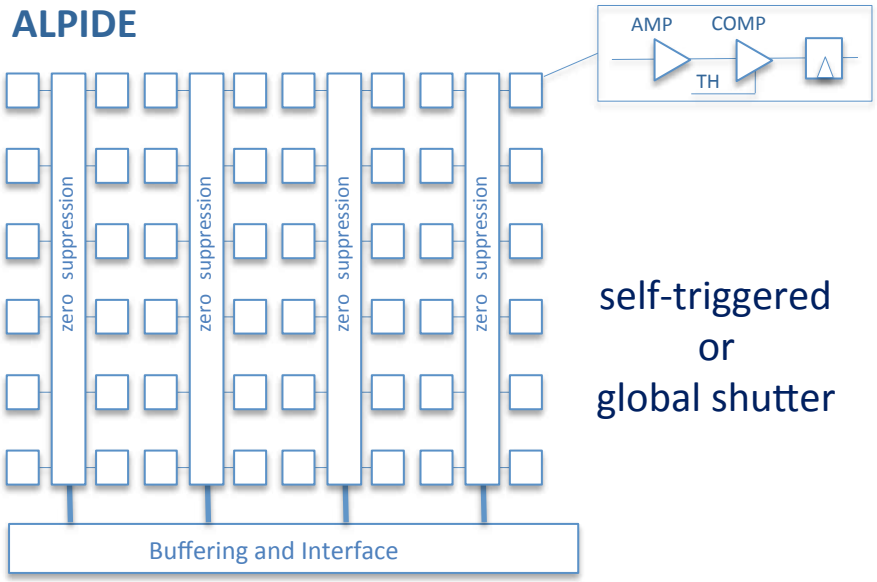
7 layers of Monolithic Active Pixel Sensors

Pixel Chip Features and Architectures

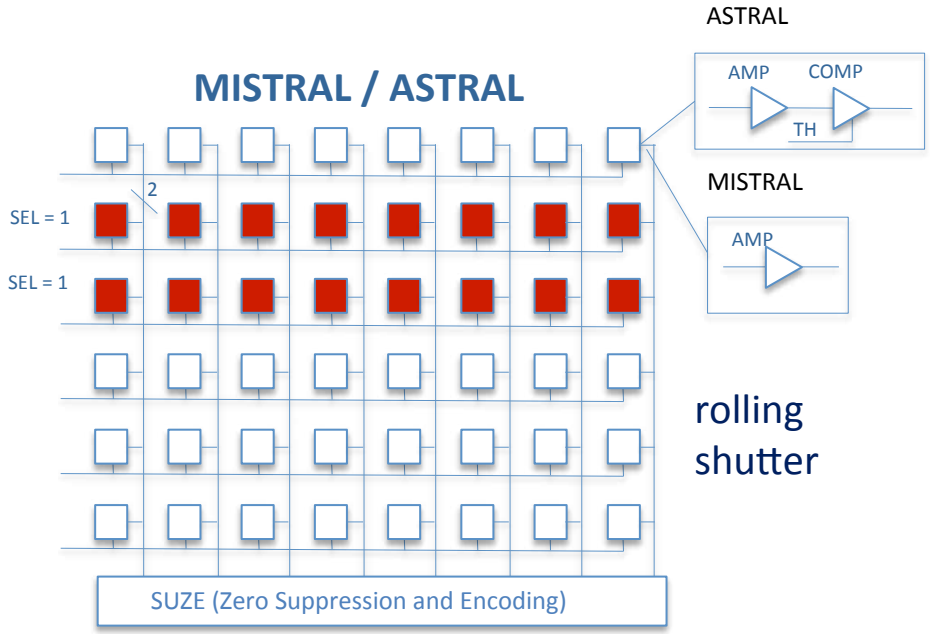
Monolithic Active Pixel Sensors (MAPS) using Tower/Jazz 0.18 µm technology

- Chip size: 15 mm x 30 mm
- Pixel pitch ~ 30 µm
- Si thickness: 50 µm
- Spatial resolution ~ 5 µm
- Power density < 100 mW/cm^2
- Integration time < 30 µs





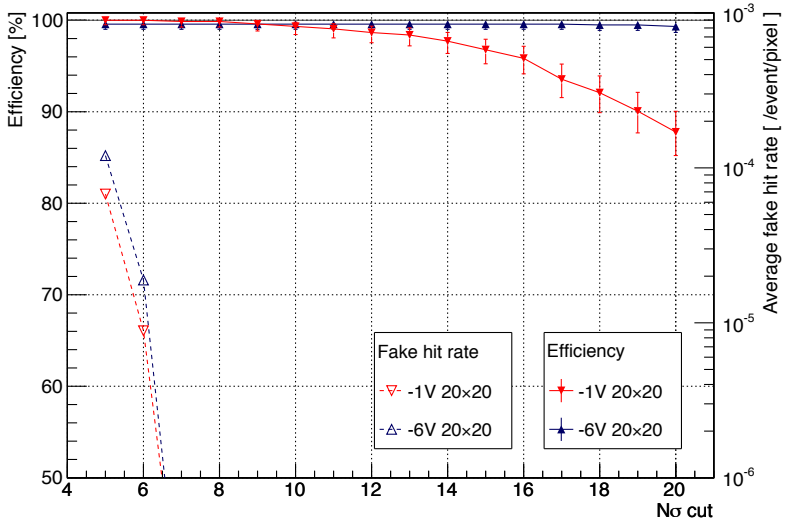
self-triggered
or
global shutter



rolling
shutter

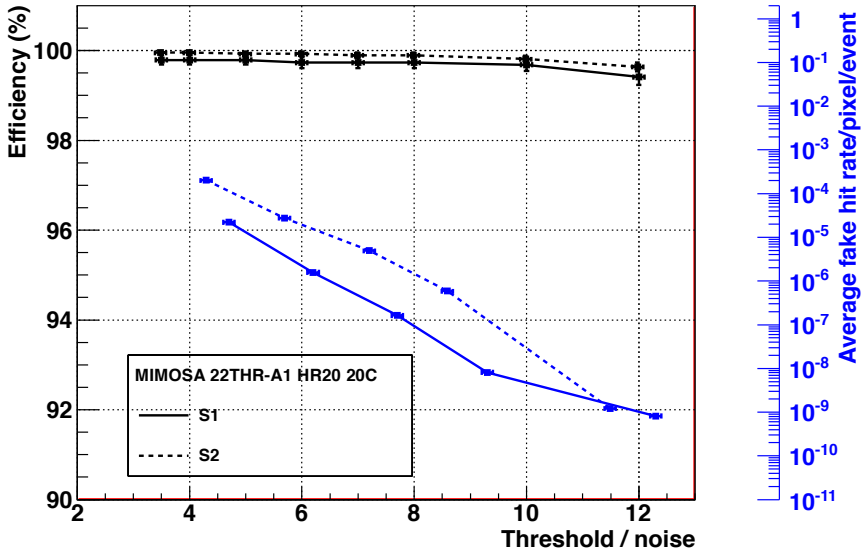
Pixel Chip Prototypes: Experimental Results

ALPIDE



Explorer: prototype with analogue output
pALPIDE: sizeable prototype of final chip (digital output) , pixel size: 22 x 22 μm^2

MISTRAL/ ASTRAL



MIMOSA-22-THR-A1 performance from digital output pixel size (22 x 33 μm^2) for two design options

At Threshold / Noise: 20
Detection efficiency: 99.7 %
Fake hit rate < 10^{-8} hits/event
Spatial resolution ~ 5 μm

Measurements at DESY with 3-6 Gev/c electron and positron beam

Pixel Chip Development and Production

- R&D started in 2011 and will continue till end 2015

- Established so far
  - Adequate radiation hardness
  - Excellent charge collection efficiency for pixel 20 – 66 μm
  - Excellent detection efficiency
  - Sizeable prototypes of different readout architectures → built and being characterized
  - Full scale prototypes, pALPIDE_FS and FSBB (MISTRAL/ASTRAL), produced with the engineering run submitted in Feb '14 and currently being tested

- Next steps
  - Next Engineering run → July 2014
  - Internal review → 16-17 July 2014
  - Final decision (external review) → Dec 2014

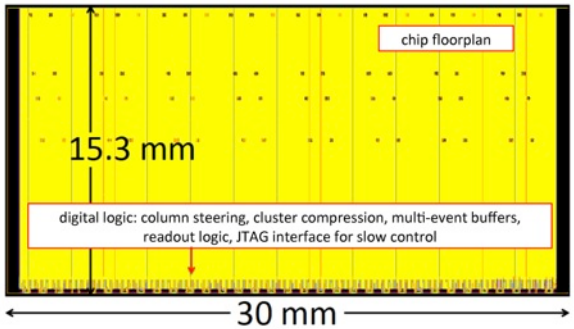
N.B.:

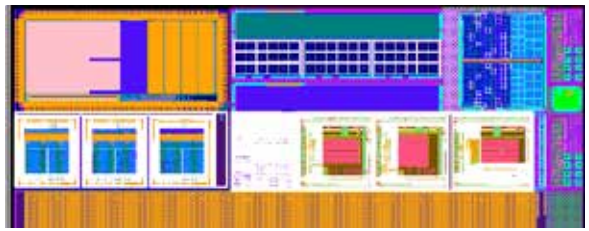
1) Physical layout and electrical interface of the two proposed circuits are identical
2) The cost of for the completion of the R&D and the cost of the mass production do not depend on the circuit selection;
3) The development of the other detector components does not depend on the choice of the circuit design

Contributi INFN a Design e Caratterizzazione dei Pixel Chip

- **ALPIDE & MISTRAL/ASTRAL**
  - Prototipo Serializzatore → **Torino**
  - PLL & Driver → **Torino**
  - Protocollo di trasmissione dati → **Padova, Torino**

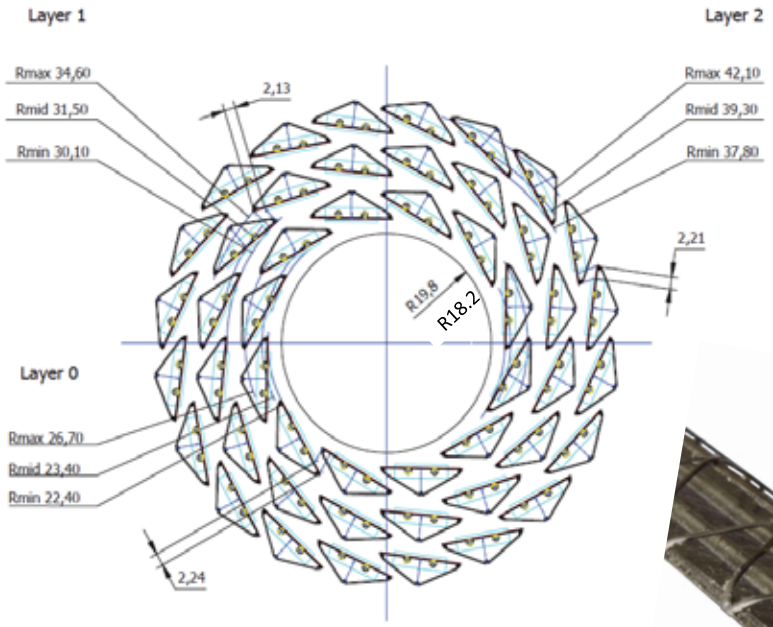
- **pALPIDE_FS**
  - Collaborazione CCNU(China), CERN, INFN, Yonsey (South Korea)
  - Matrice 1024x512 pixels con discriminatori in-pixel
  - front-end digitale:
    priority-encoder readout, formattazione dati, gestione del Multi-Event-Buffer, trasmissione dati su porta parallela da 8 bit a 40 MHz (bandwidth 320 MB/s) → **Cagliari**
  - slow control basato su interfaccia JTAG → **Cagliari**

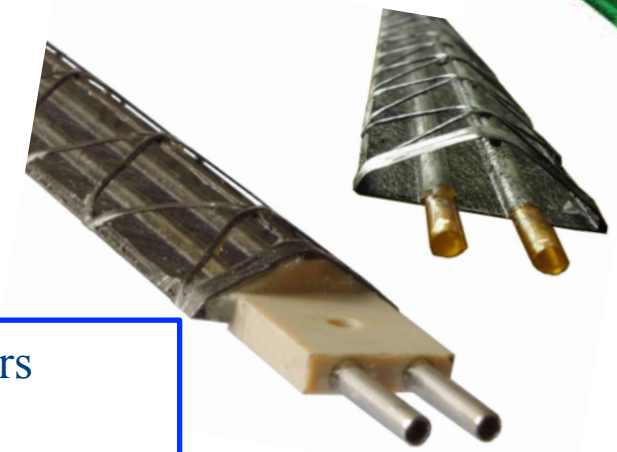


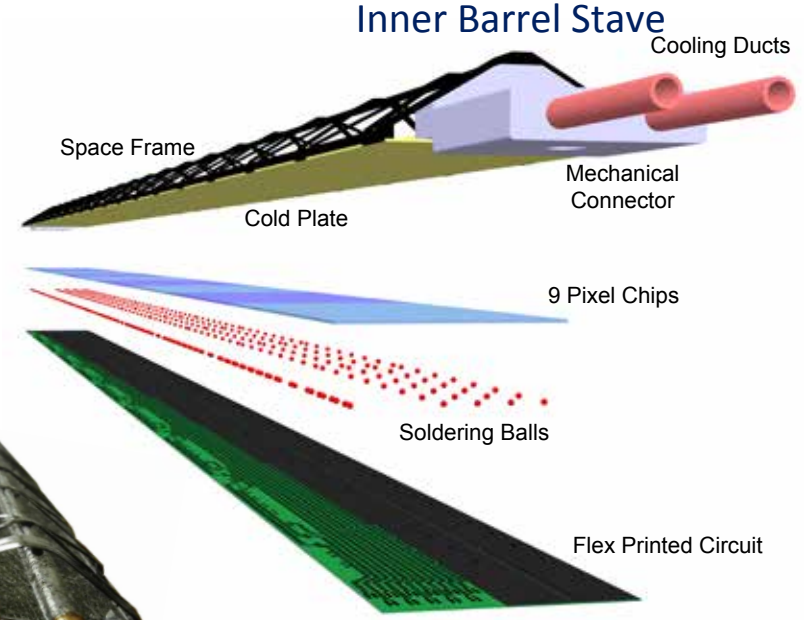


- Contributi determinanti ai test in laboratorio e su fascio a DESY (2013), LNF (2014) e CERN PS/SPS (seconda metà 2014) → **tutte le Sezioni**

Inner Barrel







Inner Barrel (IB): 3 Inner Layers

Radial position (mm): 22, 30, 38

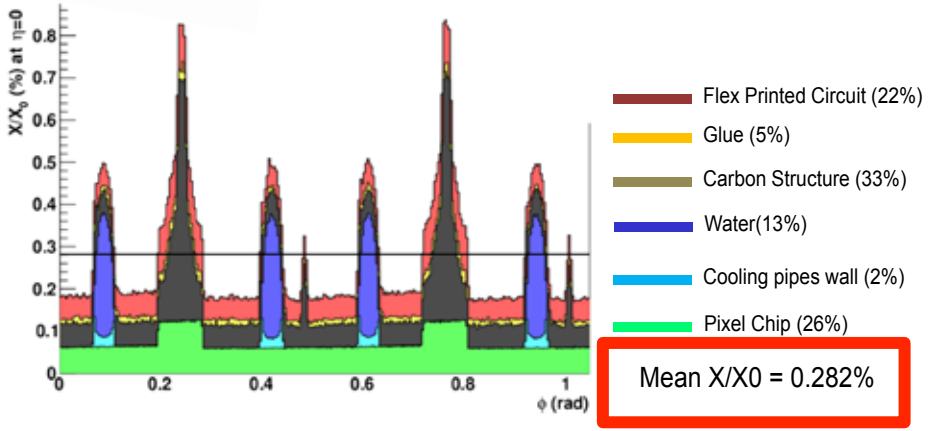
Length in z (mm): 271

Nr. of staves: 12, 16, 20

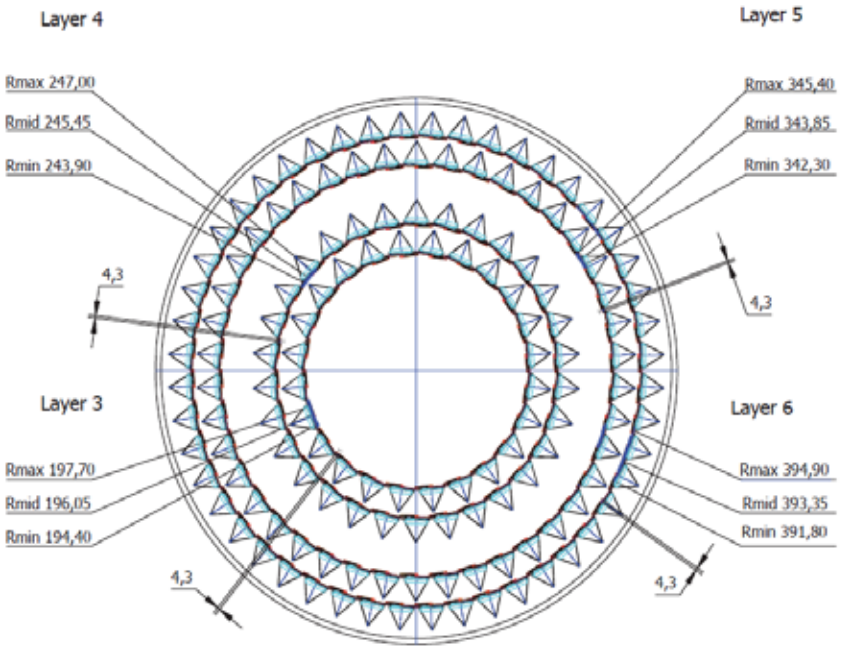
Nr. of chips/stave: 9

Nr. of chips/layer: 108, 144, 180

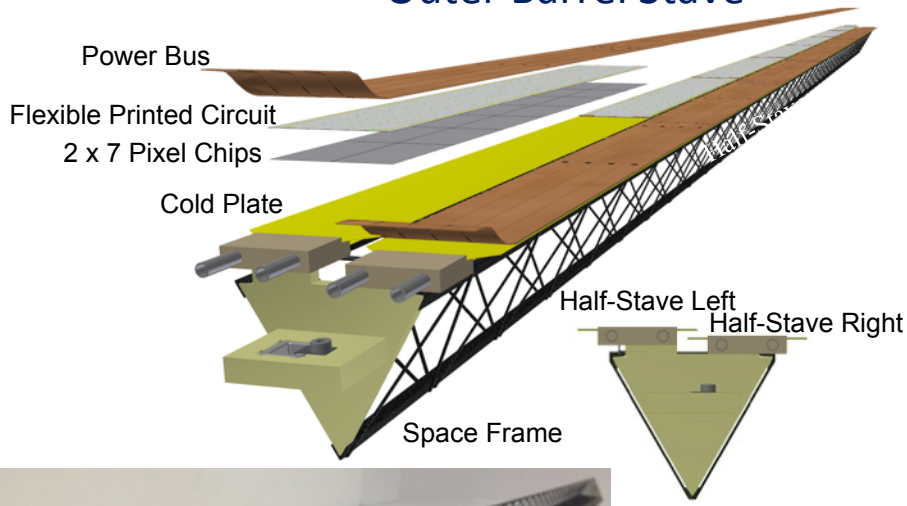
Material thickness: $\leq 0.3\%$ X_0 per layer



Outer Barrel



Outer Barrel Stave



Outer Barrel (OB): 2 Middle + 2 Outer Layers

Radial position (mm): 194, 244, **342, 392**

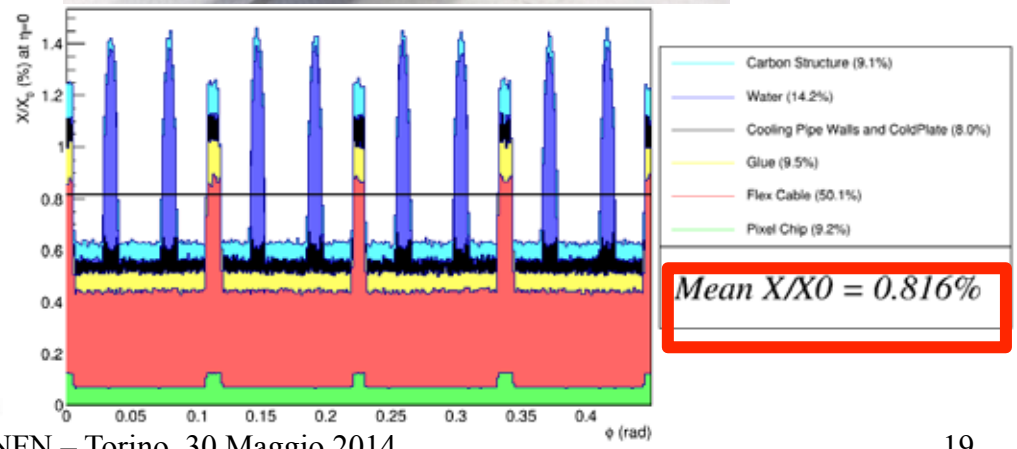
Length in z (mm): 843, **1475**

Nr. of staves: 24, 30, **42, 48**

Nr. of chips/stave: 112, 112, **196, 196**

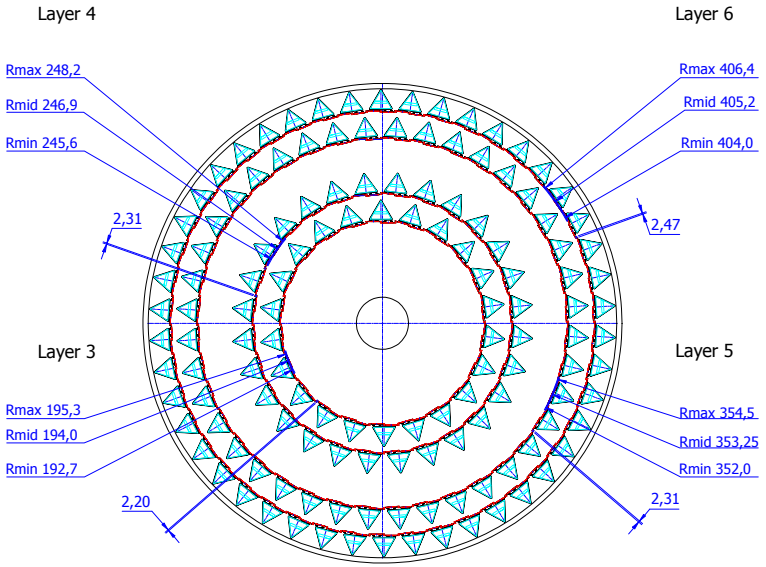
Nr. of chips/layer: 2688, 3360, **8232, 9408**

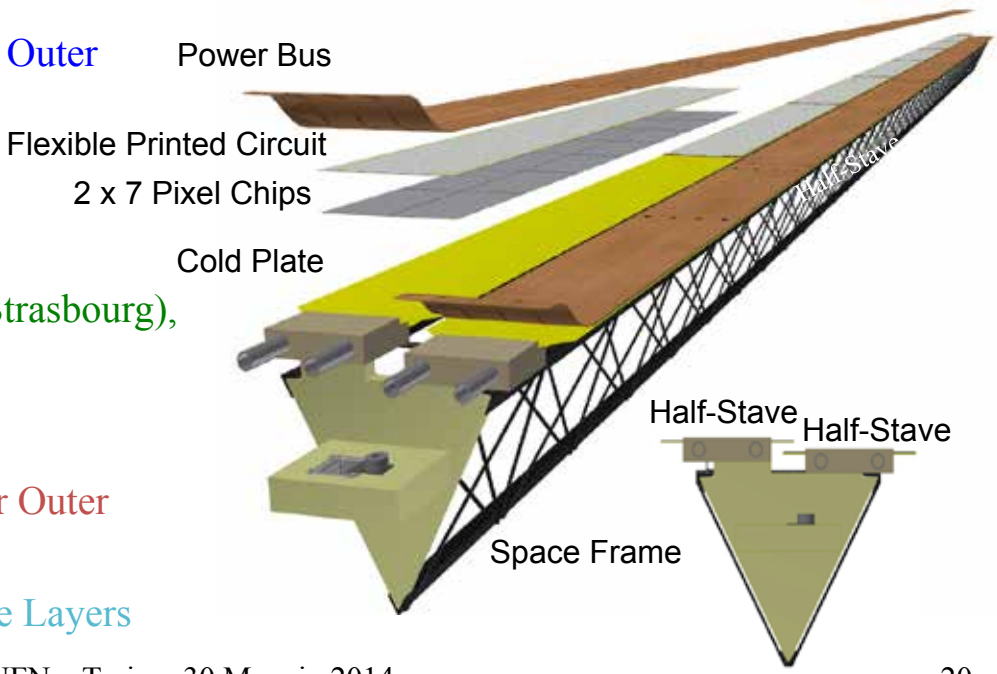
Material thickness: ~ 0.8% X_0 per layer



Construction of Outer Barrel Staves

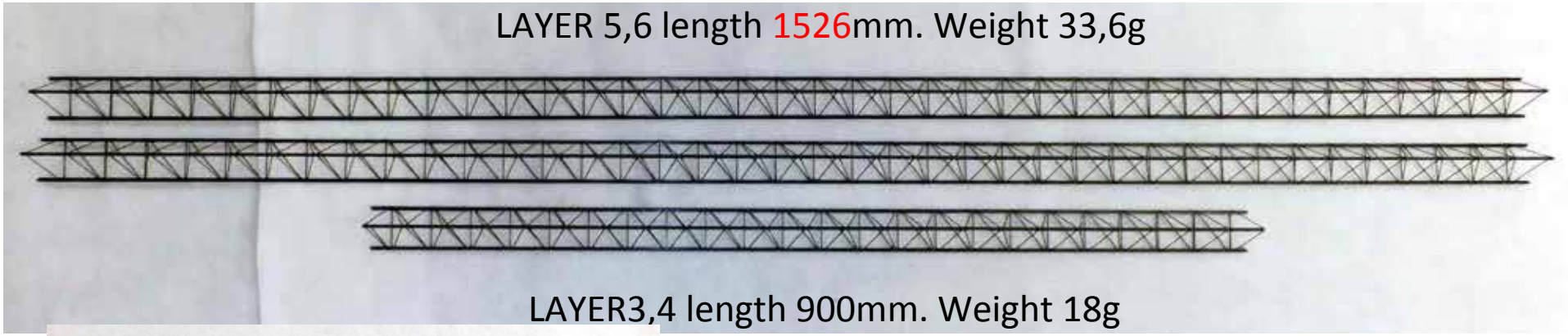
- Staves for the Outer Barrel
  - Middle Layers: 24 (L3) +30 (L4), 843 mm
  - Outer Layers: 42 (L5) + 48 (L6), 1475 mm
- Stave main components
  - Space Frame & Cold Plate (different length for Middle and Outer Layers)
  - Module (identical for Middle and Outer Layers)
    - Module Carbon Plate
    - Flexible Printed Circuit (FPC)
    - 2 x 7 Pixel Chips
  - Power Bus (different Length for Middle and Outer Layers)
- Work organization
  - Module construction (7 centers):
    - CCNU (China), INFN (Bari), IPHC (Strasbourg), LBNL, Liverpool, NIKHEF, Pusan
  - Stave assembly and test (4 centers):
    - INFN (LNF), Daresbury, NIKHEF for Outer Layers
    - Berkeley (+ CERN backup) for Middle Layers





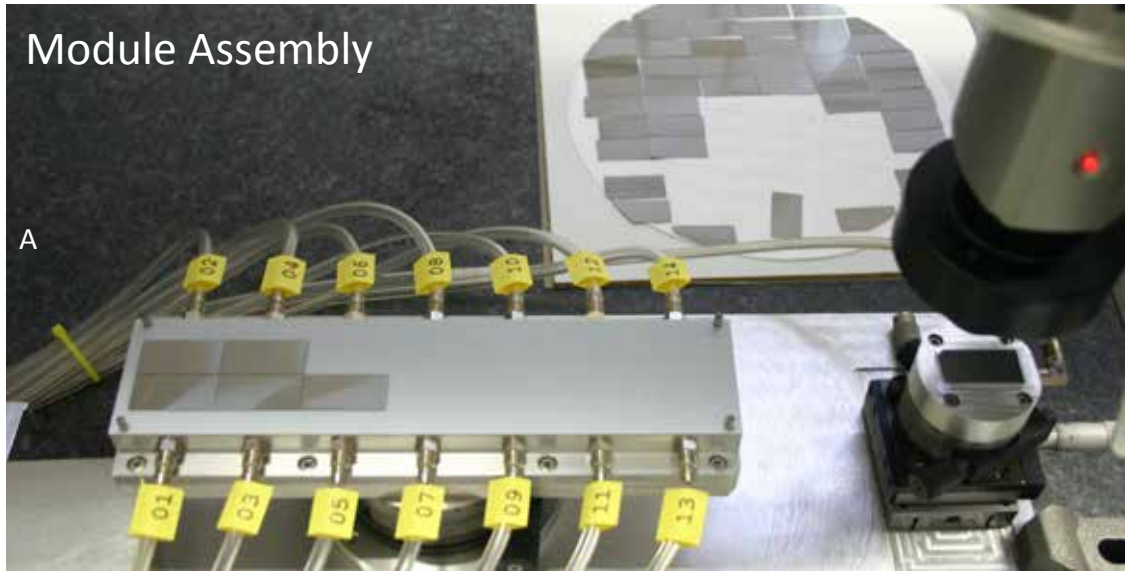
Outer Barrel Stave

Prototypes

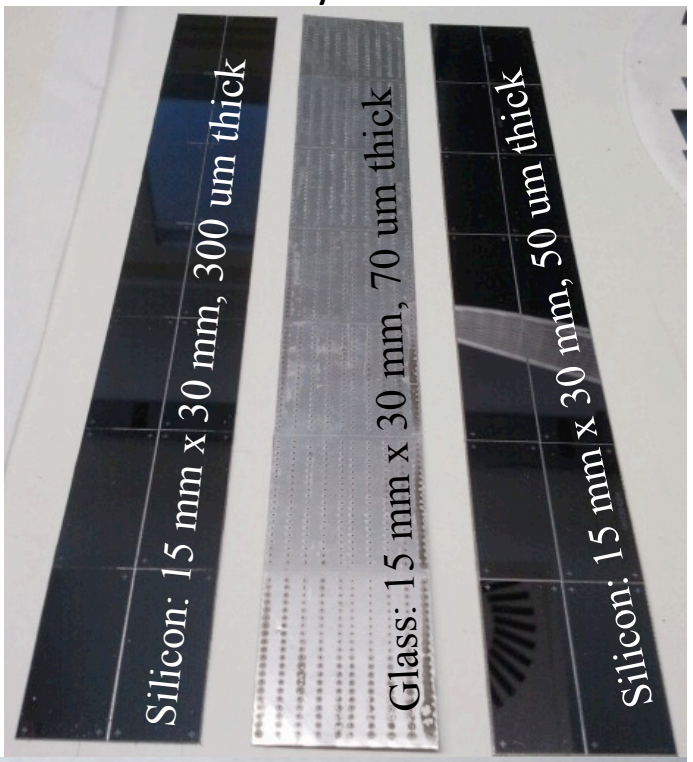


LAYER3,4 length 900mm. Weight 18g

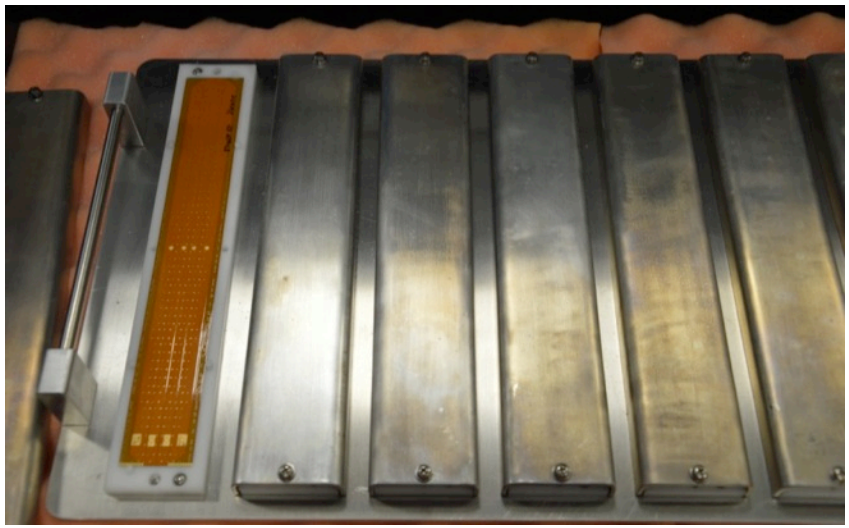
OB Module Assembly and Laser Soldering

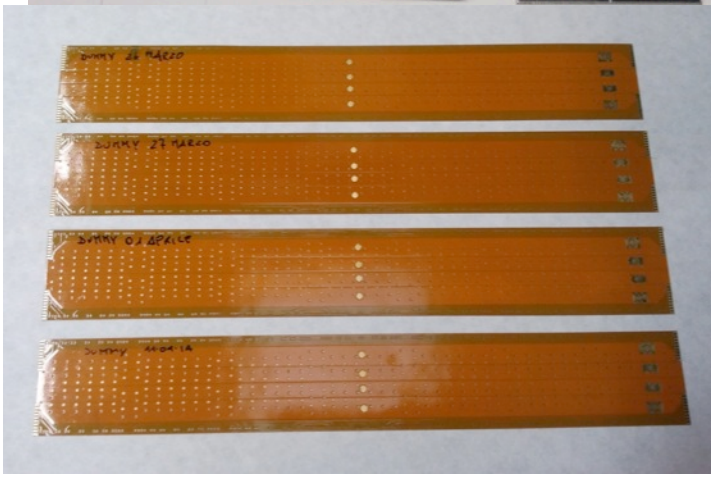


Dummy Modules



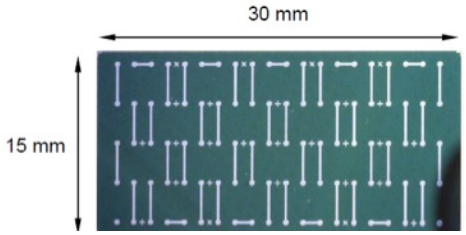
Module Shipping



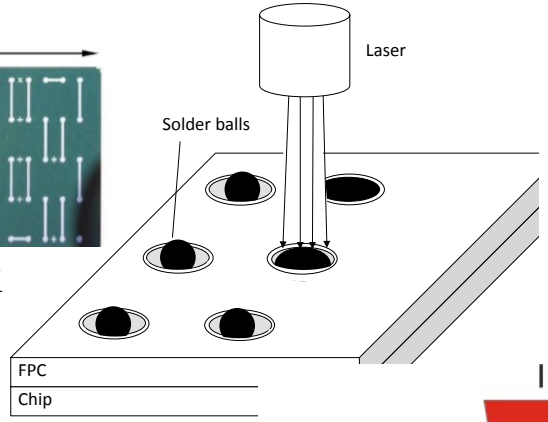


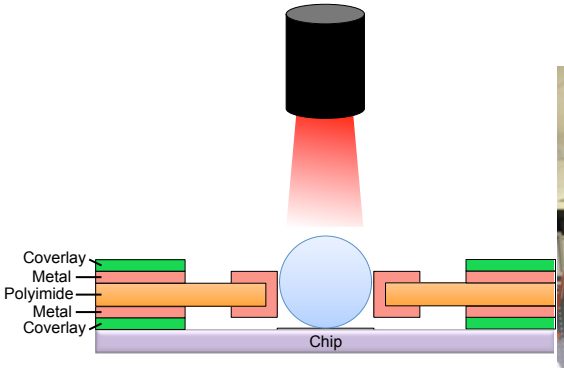
Chip to FPC interconnection – laser soldering

Interconnection of Pixel chip on flexible printed circuit by Laser soldering



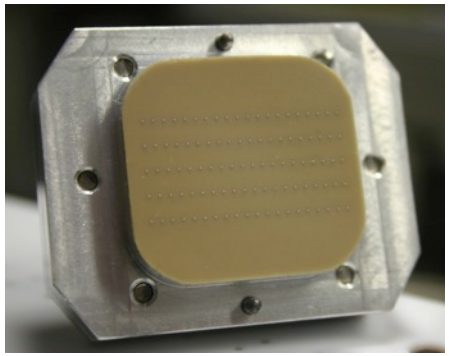
Pads over matrix

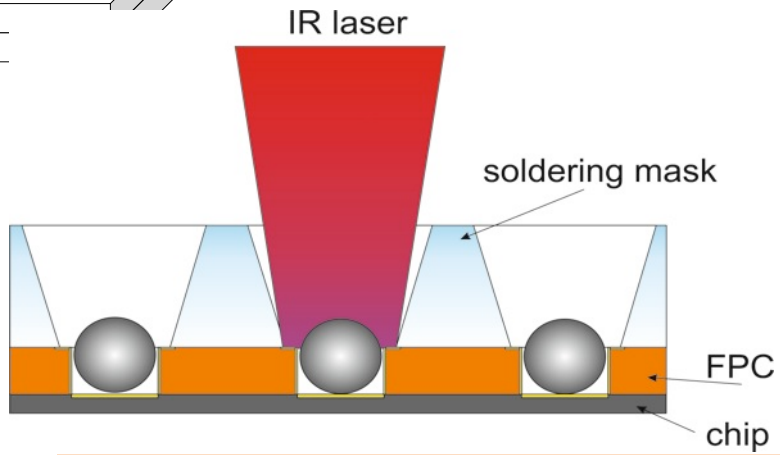




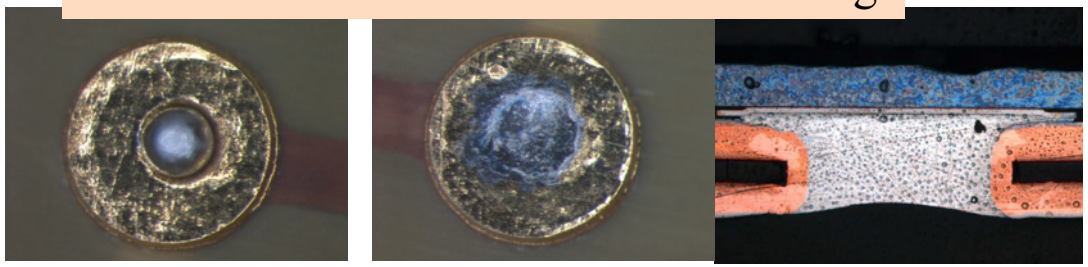
Laser system

Soldering balls pick-up tool





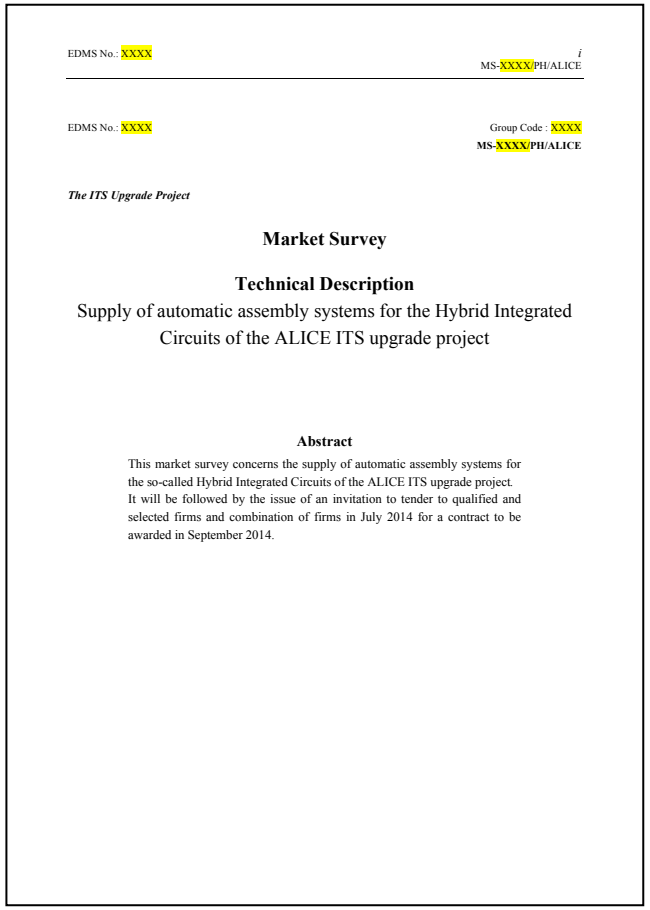
Before and after laser shooting



Module Assembly and Laser soldering

L'uniformità dei moduli la cui produzione è distribuita in diversi centri, può essere garantita solo automatizzando le procedure di assemblaggio e saldatura

- Sistema automatico per
  - Ispezione ottica
  - Allineamento e posizionamento dei chip
  - Posizionamento delle sferette di saldatura
  - Saldatura mediante laser
- Market Survey seguito da una Gara, gestiti attraverso il CERN, per la fornitura di:
  - una macchina prototipo
  - 4-7 macchina per la produzione
- Timeline
  - Market Survey → settimana prossima
  - Tender → metà Luglio '14
  - Aggiudicazione contratto → Settembre '14
  - Fornitura prototipo → dopo 6 mesi



EDMS No.: XXXX *i*
MS-XXXX/PH/ALICE

EDMS No.: XXXX Group Code : XXXX
MS-XXXX/PH/ALICE

The ITS Upgrade Project

Market Survey

Technical Description

Supply of automatic assembly systems for the Hybrid Integrated Circuits of the ALICE ITS upgrade project

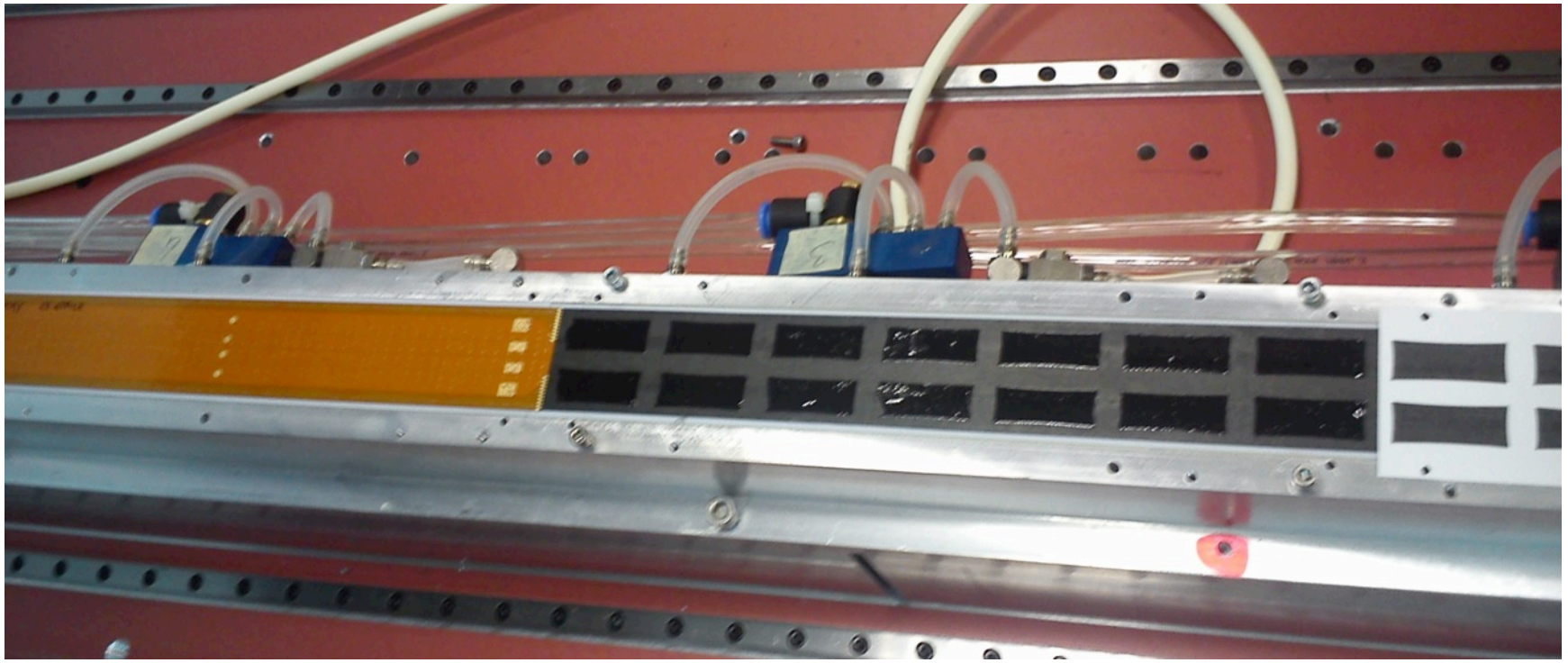
Abstract

This market survey concerns the supply of automatic assembly systems for the so-called Hybrid Integrated Circuits of the ALICE ITS upgrade project. It will be followed by the issue of an invitation to tender to qualified and selected firms and combination of firms in July 2014 for a contract to be awarded in September 2014.

- Costo per la produzione delle macchine incluso nel costo CORE del progetto

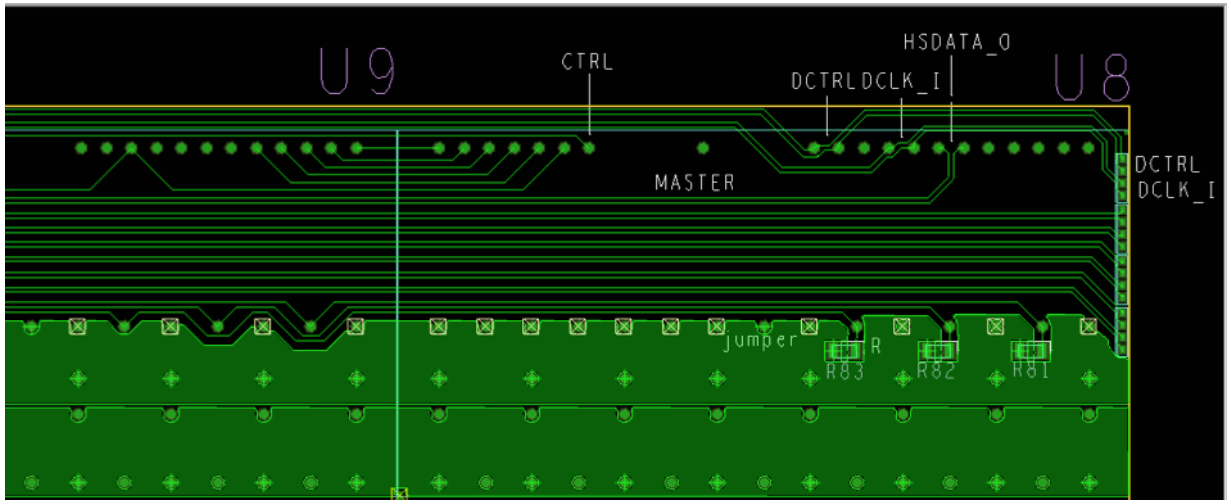
OB Stave assembly

- Riqualificazione clean rooms in atto
- Jig per half-stave assembly: versione 0 finita
- Assembly procedure: in fase di validazione
- Primo dummy half-stave (deadline July 2014):
  - 5/7 moduli incollati
  - Dummy PB in produzione
  - saldature module-to-module in fase di studio

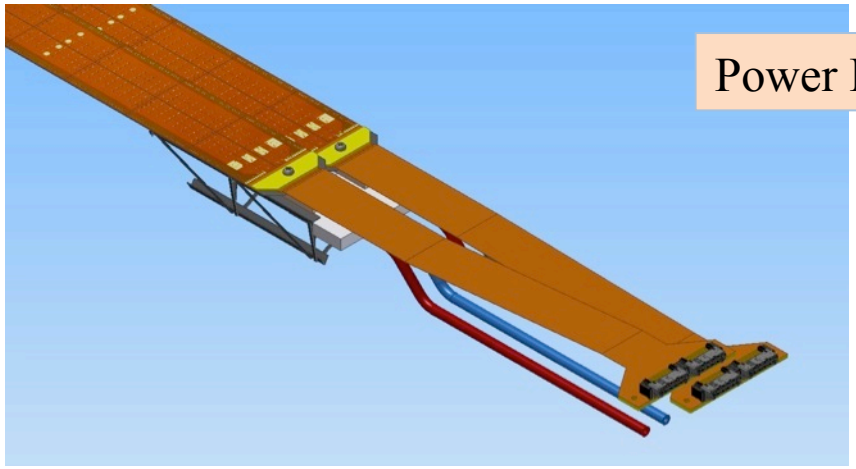


FPC and Power Bus

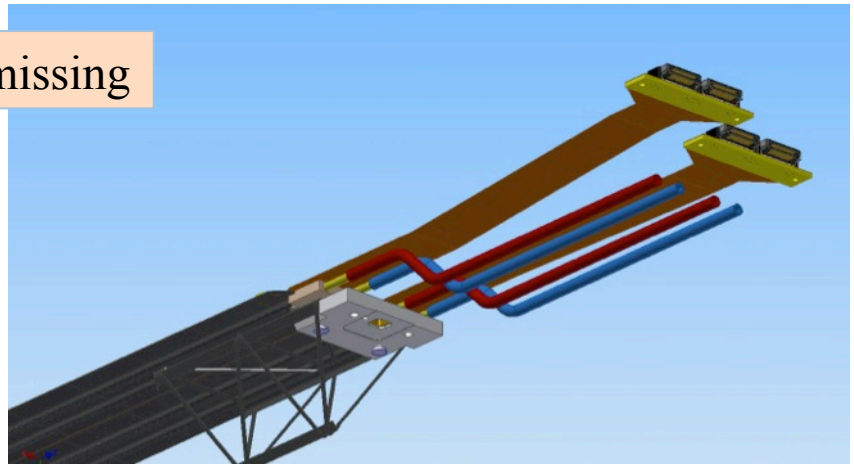
- FPC-Prototypes per moduli dummy e test di saldatura → prodotti
- FPC-v0 per studi di sistema e interconnessione fra i moduli → in produzione
- FPC-v1 modificato in accordo ai requisiti del protocollo di comunicazione fra i pixel chip e il mondo esterno → disegno in corso
- PB-v0:
  - layout minimale per prove di saldatura su dummy half-stave
  - studi di fattibilità presso laboratorio di Rui de Oliveira: chemical etching + Cu vacuum deposition and electroplating + Ni-Au deposition

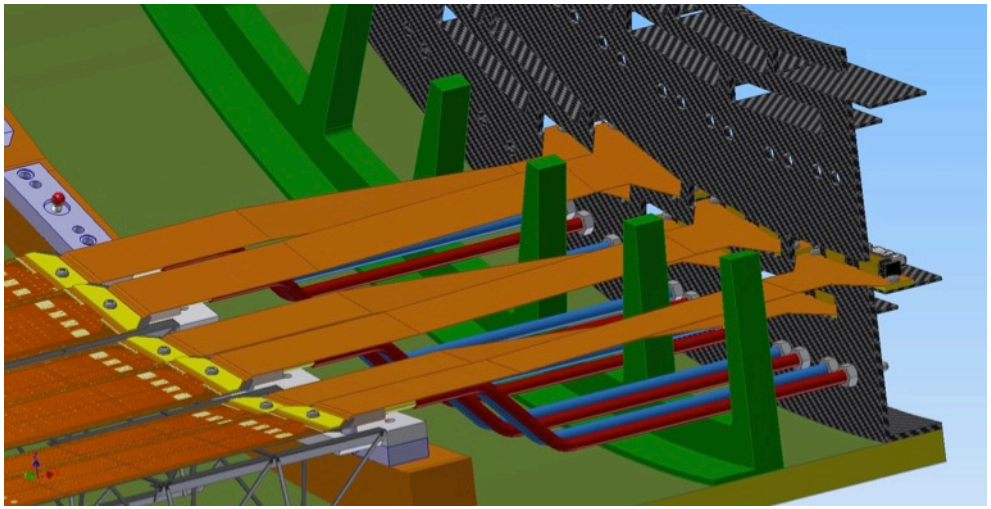


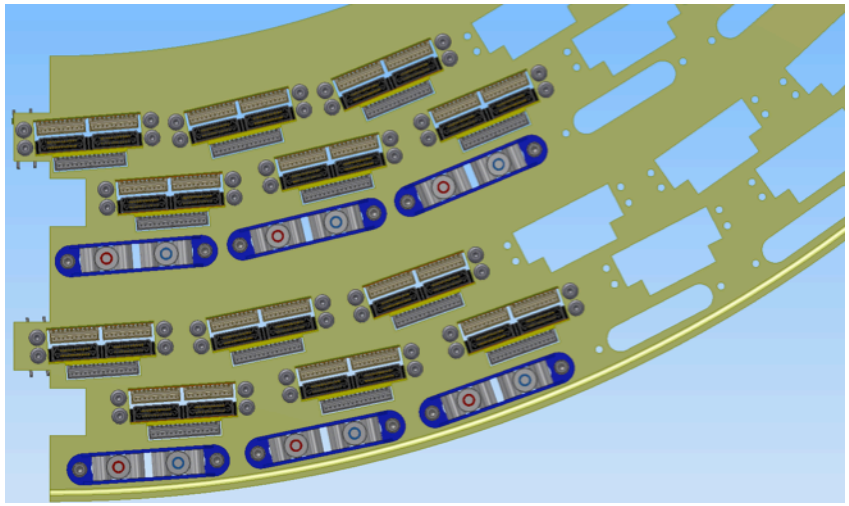
End-of-Stave, End-Wheels and Integration



Power Bus missing

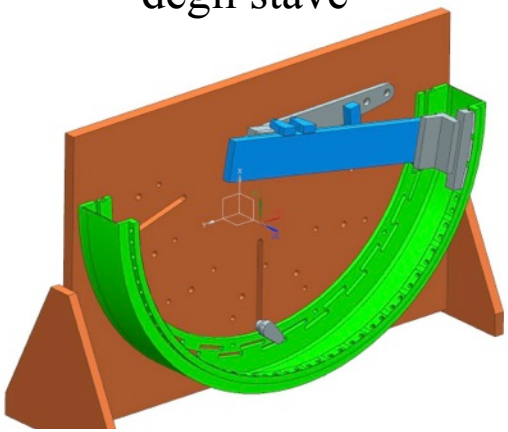


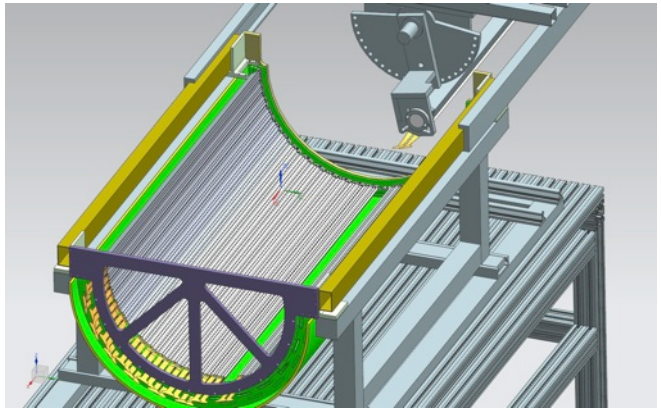


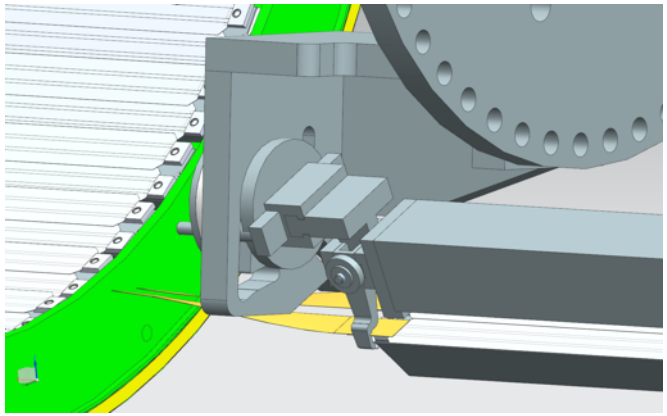


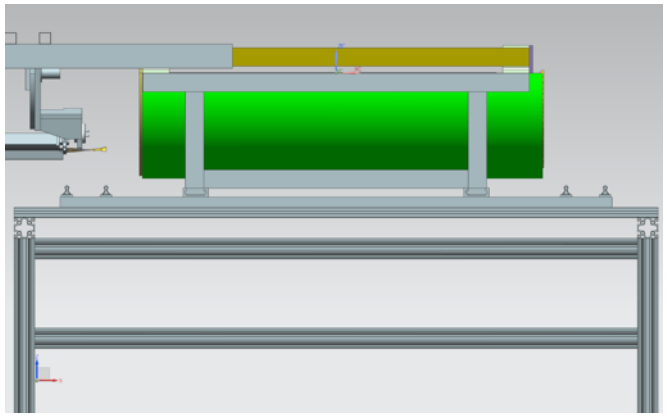
End-of-Stave, End-Wheels and Integration

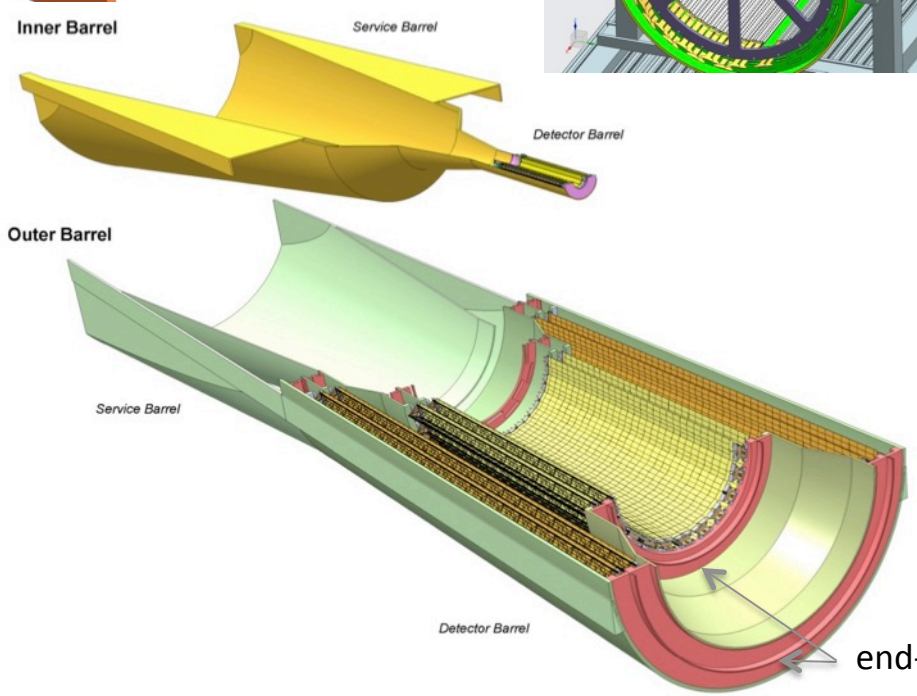
- Integrazione degli Stave in Half-Layer
  - Le end-wheels permettono un accurato posizionamento degli stave











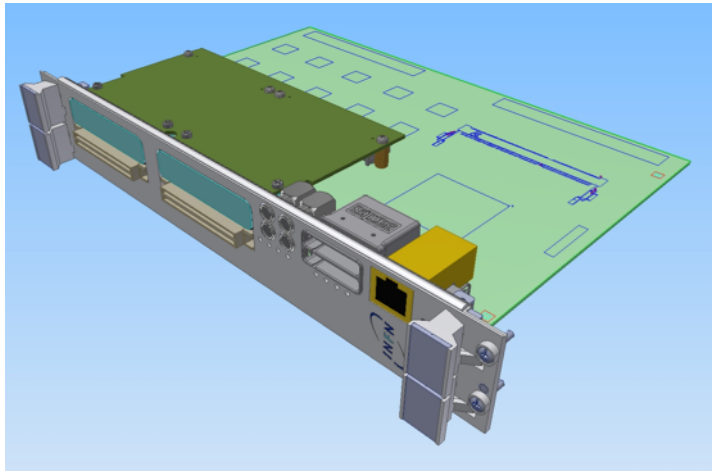
- Detector e Service barrel
  - Services from one side only

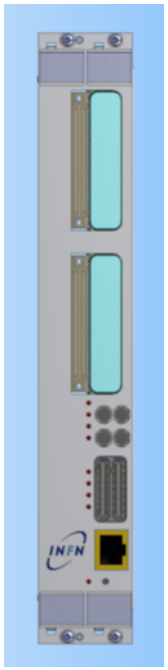
Chip, Module and Stave Test System

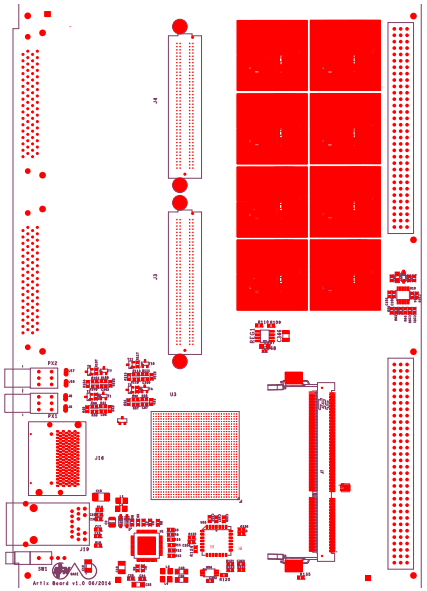
- Sistema di test per Chip, Moduli e Stave durante la produzione → **Bari, LNF**
  - Requirements
    - 9 input seriali ad alta velocità > 1Gb/s
    - 1 output per clock @ 40 MHz
    - 1 linea di controllo @ 40 Mb/s
    - Memoria adeguatamente dimensionata per acquisire gli eventi
    - Interfaccia veloce con il PC
    - Flessibilità per sviluppo versioni successive e applicazioni diverse
  - Specifiche implementate
    - VME board (only for power supply)
    - 12 Hi speed Input + 12 Hi speed output Up to 6.6 Gb/s
    - 24 Low speed serial I/O - Up to 1 Gb/s
    - 64 general purpose LVDS I/O
    - Gigabit Ethernet interface + Protocollo software "Logical Link Control"/IEEE 802.2
    - 3 NIM configurable I/O
    - 2 expansion slots – Mezzanine boards (standard FMC)
    - 1.5 MB internal memory (inside FPGA)
    - 1 GB memoria on-board (modulo SODIMM DD3)
- Dettagli in corso di definizione parallelamente alle specifiche dell'interfaccia dei pixel chip

Chip, Module and Stave Test System

- Disegno PCB è in corso (16 layer)
- Acquistate evaluation board Xilinx (stesso tipo di FPGA) per Bari e LNF per lo sviluppo e il test del firmware (Bari) e del software (LNF)
- Data prevista per avvio produzione prototipi PCB → Luglio '14
- Data prevista consegna schede prototipo assemblate → Settembre '14







Test System per Prototipi Pixel Chip Full-Scale

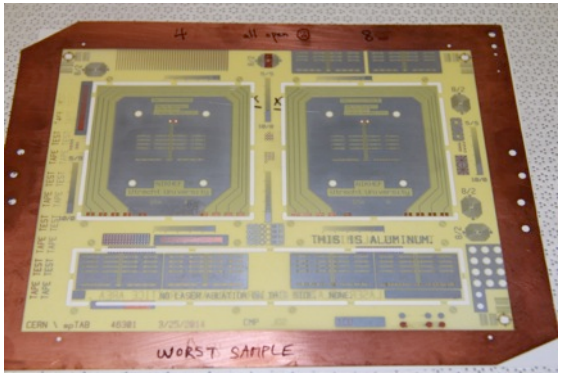
- Caratterizzazione prototipi pixel chip full-scale → **Cagliari**
  - Sistema descritto in precedenza non adeguato per
    - caratteristica dei segnali di uscita
    - complessità
    - scala temporale
- Sistema di test compatto con interfaccia USB3
  - Progettazione, produzione prototipi e commissioning
  - Test di lab e su fascio di pALPIDE_FS
  - Adattamento per FSBB in corso
- Test dei pALPIDE_FS
  - Pixel chip functionalities
  - Digital periphery slow control and readout logic
  - DACs
  - Pixel matrix
  - Tests con Fe-55
  - Hit maps e Cluster size

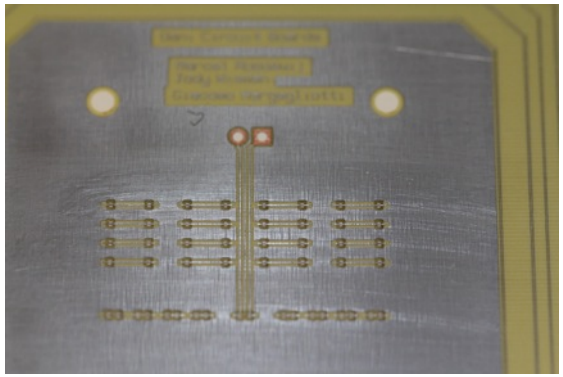
Responsabilità

Institute	Responsibilities
Bari	• OB Module • Development, Module 0, Production • Design of the End of Stave services • Module and Stave test system (*) • Power distribution and supply system (pro-tempore)
Cagliari	• Chip design and characterization • Chip characterization system (*)
LNF	• LNF Beam Test Facility • OB Stave Production
Padua	• Outer Layers End-wheels and Half-layer Integration
Turin/Alessandria	• Chip design and characterization • OB FPC and PB • OB Stave • Development, Stave 0

Altri contributi

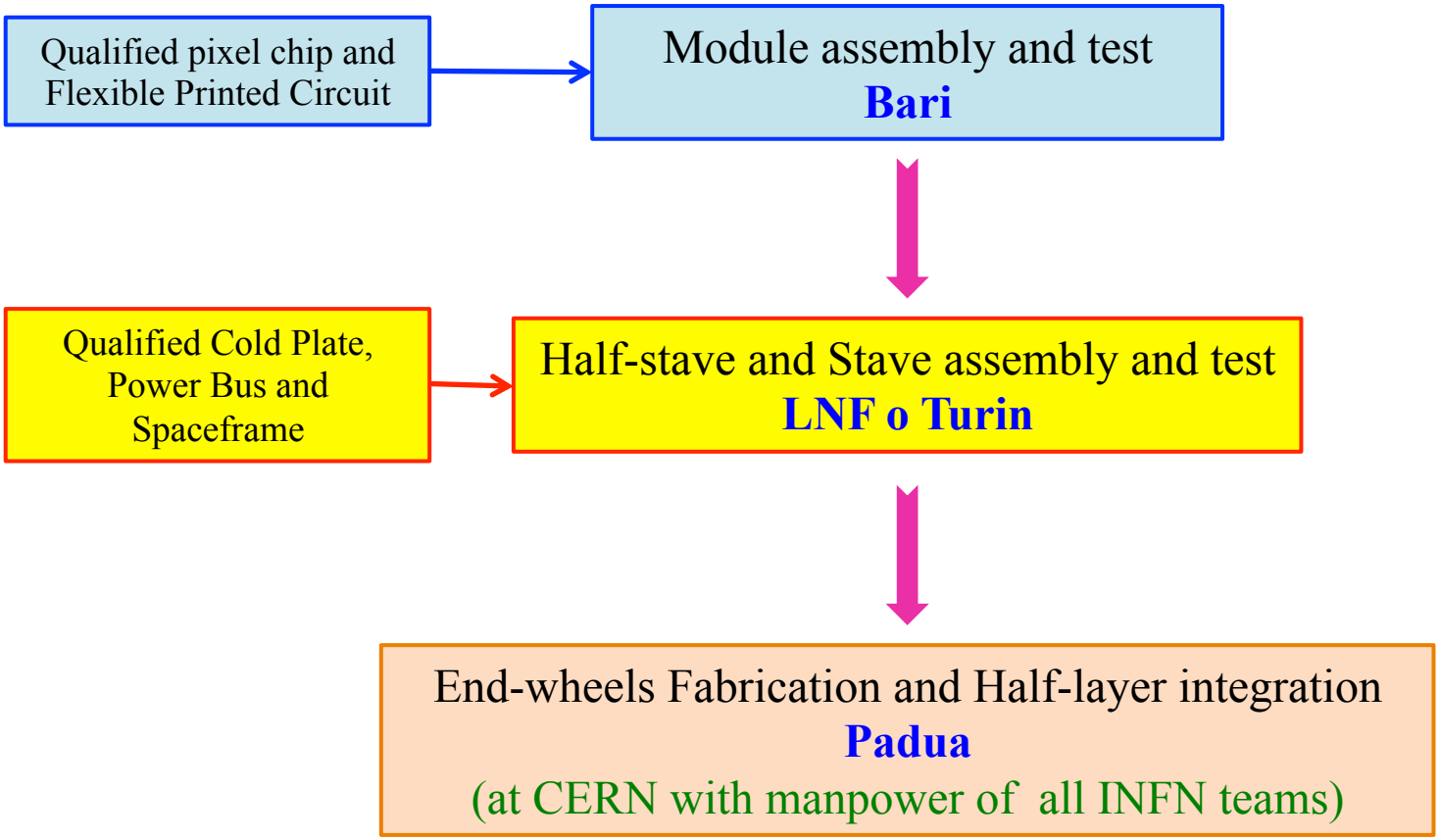
Activity	Contributing INFN teams
Chip test and characterization	Bari, Cagliari, Catania, LNF, Padova, Roma, Alessandria/Torino, Trieste
Mechanics for the Stave assembly	Cagliari
Pixel chip, FPC and PB qualification and selection	Catania, Trieste
Module and Stave test system	LNF
SpTAB (interconnect technique backup wrt laser soldering)	Trieste





- Circuiti stampati flessibili FR4-Al e Tab-bonding → **Trieste**
  - Ditta: OMNI CIRCUIT BOARDS
  - Sezione: 30 μm Al e 50 μm FR4
  - Prossima produzione: migliore qualità alluminio per ottimizzare l'aderenza del bonding
  - Tab-bonding realizzato dalla ditta MIPOT
  - Spesa stimata per il completamento dell'R&D: 5 k€ per flex + 7 k€ per tab-bonding

Construction Flow-Diagram



Funding and Spending Profile (kEUR)

Overall INFN funding for the ITS Upgrade:

- **2013-2015**: R&D – Modulo/Stave 0 → **1000 kEUR**
- **2015-2018**: Construction → **2900 kEUR**

Totale 3900 kEUR

New Spending Profile

	2013	2014	2015	2016	2017	2018	2019	Total
R&D (kEUR)	258	337+136	228					959
CORE (kEUR)			445	1040	935	400	80	2900

FINE