LAr upgrade for Phase II

V0.1 (May 2014) - F. Tartarelli

As explained in the "Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment" [1], to meet the challenges and take advantage of the operation of the ATLAS detector at High-Luminosity LHC (HL-LHC), an upgrade of the Liquid Argon Calorimeter readout system is required. The main factors driving this decision are the following:

- *Radiation resistance: replace components with versions more rad-tol (when required) to sustain 3000 fb^{-1}*
- *Ageing: some components would have ~15-20 yrs of operation at the beginning of RUN 4. They are also difficult to maintain and repair.*
- *Provide highest granularity information and resolution: efficient and selective triggers at high luminosity ($L=5x10^{34}$ cm^{-2} s^{-1}/μ=140); Making extensive use of detailed topology of clusters and events; Providing improved Calorimeter Trigger primitives for e/γ/τ/jets, matching with Track Trigger, isolation, etc*

The proposed new electronics will maintain the analog performance of the existing one: 16-bit dynamic range and low coherent noise (less than 5% of the incoherent noise). Moreover the upgrade will be used to overcome some of the limitation of the current design.

As it is proposed for other detectors, the general trend for LHC calorimeter read-out architecture is the following:

- Remove all on-detector sums
- the data are not buffered in the front-end, but rather streamed off-detector at LHC bunch-crossing frequency of 40 MHz
- fast pre-processors convert raw-data into calibrated information that feed the trigger system where improved and more complex algorithms are applied

Off-detector buffers allow for much higher trigger latency or purely software-based triggers.

The main functional blocks of the new architecture are shown in Figure 1. The new Front End Boards (FEB2) will provide analog preamplification and shaping, production of (summed) analog signals for the LTDB, analog-to-digital conversion of all signals at a rate of 40 MHz, multiplexing and serialization of digital data, and transmission over high-speed optical links. Since there will be no Level-1 pipeline, the control logic will be limited to clock distribution and slow controls for configuration and calibration. After digitization, the raw data produced on a FEB2 represents 128 (channels) x 14 bits (incl. two gain scale bits) x approximately 40 MHz, or about 72 Gbps. Conservatively assuming 25% overhead for control words and encoding, each board needs to multiplex, serialize and transmit 90 Gbps of data, leading to a total data transmission rate of 140 Tbps. A radiation-tolerant serializer in 250 nm silicon-on-saphire technology able to run at 5 Gbps has already been developed. With a newer process, speeds of

10 Gbps should be achievable. Moreover, the CERN GBTX/Versatile Link solutions are also possible if the needed speeds will be achieved.

The LTDB, introduced in Phase-I, can be kept to provide signals to the Level-0 and/or Level-1 trigger stages. At this time, no control board is foreseen for Phase-II. Both clock and control directives are expected to be sent over a dedicated optical link to each individual FEB2 as well as the calibration board. This approach, somewhat more complex off-detector, removes the need for a separate slow bus and dedicated ASIC. The main tasks of the back-end electronics of the LAr Calorimeters are the reception of digitized data from the FEB2 boards, data filtering and processing, as well as data transmission to the trigger and DAQ system. As already mentioned, the expected raw data rate from each 128-channel FEB is 90 Gbps. The total input data rate to the LAr back-end amounts therefore to about 140 Tbps.

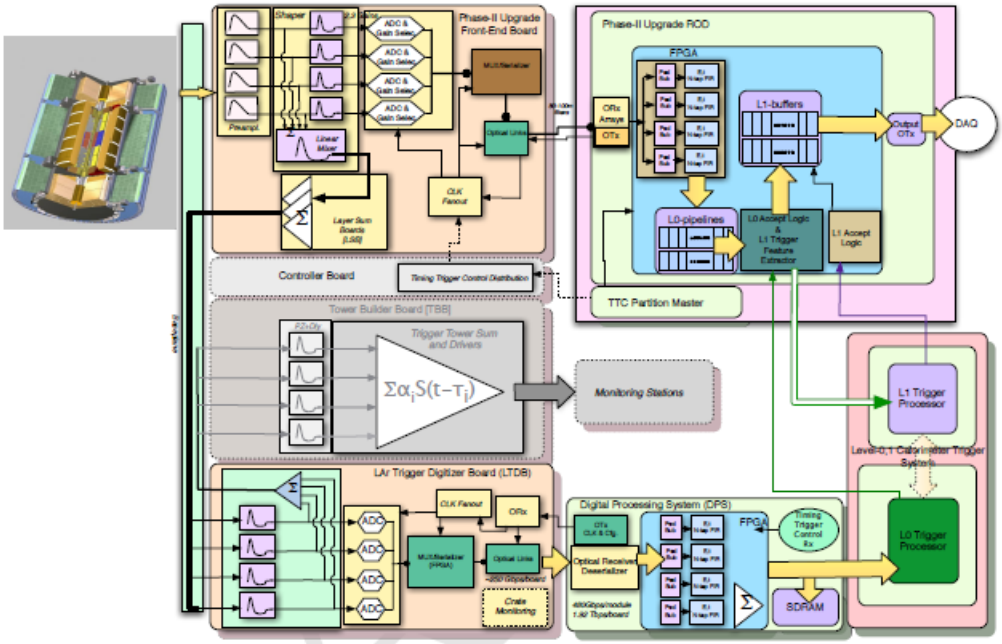

Figure 1: New proposed architecture for LAr calorimeter readout in Phase II

Possible Milano contributions to the Phase II upgrade

Our planned contributions to Phase II upgrades are further developments of our contributions to the Phase I upgrade.

DC powering

For Phase I upgrade we are designing the power distribution for the 124 new trigger boards (LTDB), including the choice and qualification of the POL (Point-Of-Load) that will be mounted on the boards. However, the low-voltage power supplies (LVPS) will remain the same. These are water-cooled 3 kW DC/DC converters located on detector (in the Tile Calorimeter finger gaps). The units operate in an external magnetic field up to 300 Gauss and 20 krad. For Phase I the seven existing voltages provided by

the LVPS will be used as input to the POLs to produce the (lower) voltages needed by the LTDB electronics.

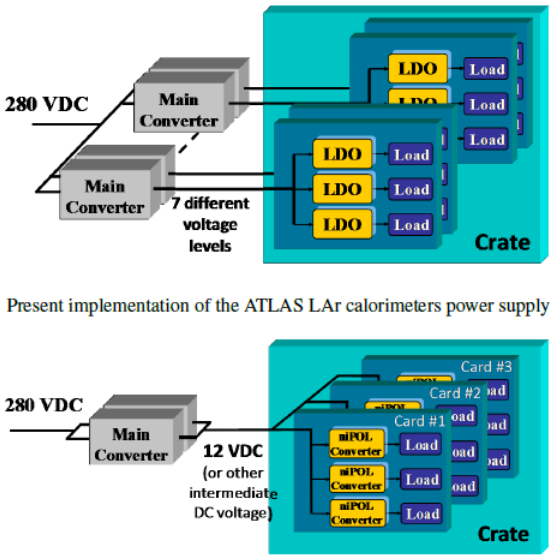

Figure 2. Present implementation of the ATLAS LAr calorimeters power supply network.

Figure 3. Proposed power supply distribution system (niPOL = non-isolated Point of Load).

Figure 2: Old (top) and new (bottom) power distribution scheme for the front-end of the LAr calorimeter

For the Phase II upgrade, exploiting the experience and knowledge gained in Phase I we would like to design the power distribution scheme for the 1534 new Front-End Boards (FEB2) that will replace the existing FEBs (Figure 2). There is no power distribution scheme design yet, however, we expect that the POLs selected for Phase I would meet the requirements for Phase II. They could be the same or a slight variant of them; their integration in the FEB2 needs to be studied.

The 58 LVPS will be exchanged with new units. The new units will still accept 280V as input as today (provided by AC/DC converters located in USA15) but they will deliver just one intermediate voltage (probably 24V) instead of the 7 voltages produced today (see Figure 2, bottom). The 24V will be used as input to the POLs to generate the voltages needed by the new FEB2s (around 1V).

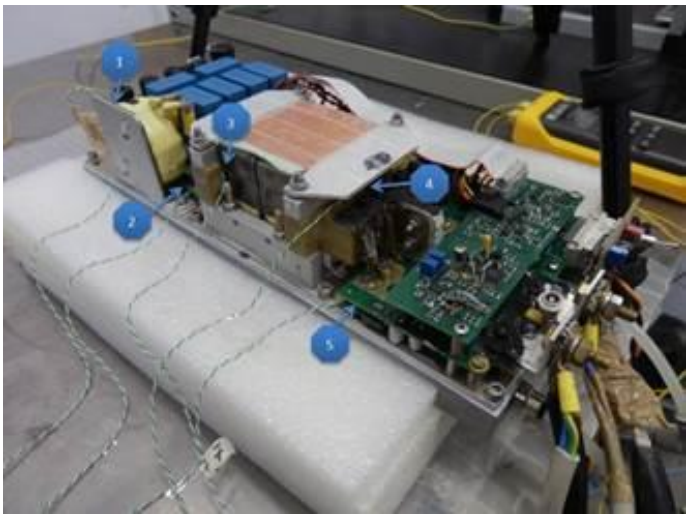

Figure 3: First LVPS prototype built in the framework of the APOLLO project

A full scheme of the power distribution was studied in the framework of the Gruppo V project "APOLLO" [2] [3] which ended in 2013. A new LVPS prototype with characteristics compatible with the LAr requirements, was designed, build and tested (Figure 3). Successively, based on the results of these tests, a new prototype unit was designed. The new prototype is under construction at CAEN (will be available in a few months). Three units (that operated in parallel to provide the total power needed by LAr) will be tested electrically and in presence of a magnetic field. To save time and money the present prototype will mount commercial non-rad tolerant power MOSFETs. The power MOSFETs will be replaced with rad-tol components at a later stage.

The APOLLO project started a few years ago when the Phase II ATLAS upgrade was on a shorter timescale. It is now necessary to revisit the project in light of the progress in power component technologies and in light of the new Phase II schedule.

For example, in the last years the industrial technology has evolved from Si MOSFET based power devices to GaN-based devices. These devices operate at higher frequency than Si-based devices and so have lower power dissipation. Moreover new commercial power architectures are becoming available. Developments in the field can be followed in two ways: continuing to explore the possibility to pursue a custom development or evaluating available commercial products. In more detail:

- In the first case we want to modify the design of the units produced by CAEN. Search and select GaN MOSFETs on the market and test them. Then replace the Si MOSFETs with GaN MOSFETs in the CAEN units, and redo all the tests and qualification.
- In the second case we want to explore solutions already available on the market. For example there are already interesting solutions produced by Vicor, like the power systems of the ComPAC series. We would like to acquire these or similar modules and study their characteristics and compatibility with LAr application (including operation in magnetic field and rad tolerance). If these "bare" modules are found suitable for our purposes, next step would be to integrate these modules (one or more, depending on the available power) into a single LVPS

unit. The units will have to match the mechanical constraints of LAr as, like the existing units, they will have to fit in the limited space between the Tile calorimeter fingers. Cooling solutions and full logic and control need also to be designed and then implemented.

We believe this is an important item to be studied that would give us good exposure inside the Collaboration. Given the time it was necessary to design, produce and commission the LVPS presently installed in the detector, we believe it is about time to start this R&D finalized to design LVPS for LAr. Moreover it is important not to lose the expertise we have gained during the years of the APOLLO project. Former members of APOLLO (PV, PD, ENEA-Casaccia, …) have express interest to pursue these studies. Other Institutes in the LAr collaboration might be interested and collaborate on this topic: BNL (which followed the production of the LVPS by MDI, used during Run 1) and CERN (which is following the commissioning of the new LVPS by Wiener to be used during Run 2). Developments in this field might also be useful for other ATLAS sub-systems. In the context of the IFD2014 Workshop it was investigated if possible synergies with CMS-Italia could be established but none were found.

Lar trigger

We have always been and still are involved in studies of the performance of the LAr calorimeter: energy calibration of electrons and photons, photon/jet separation,… During Phase II it is planned to read all calorimeter channels at full granularity and send the data off detector at the LHC bunch crossing frequency of 40 MHz. This opens the door to the possibility of implementing more complex selection algorithms, similar to those now implemented in the offline or high-level trigger, already at lower trigger levels, possibly Level 1. We would like to pursue these goals both studying new trigger algorithms and contributing to the design of the new trigger architecture.

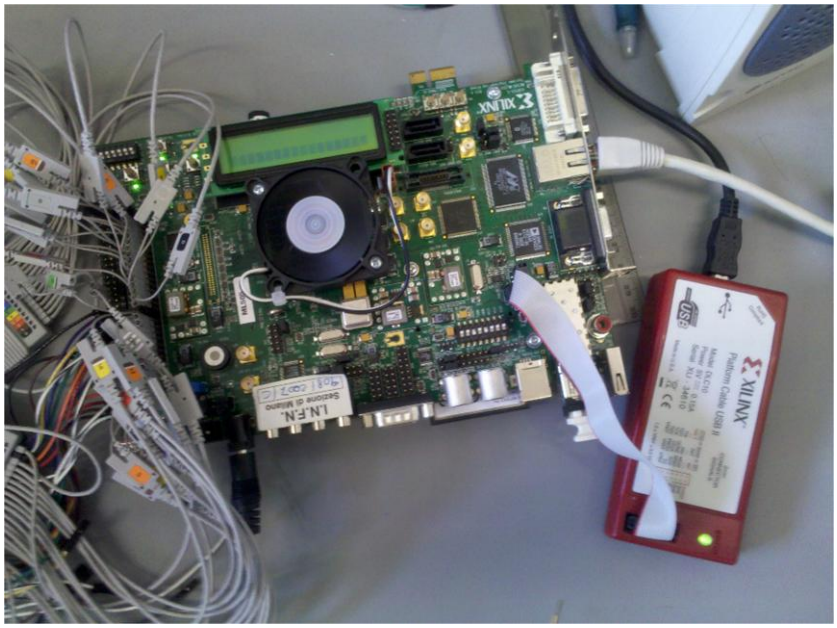

Figure 4: FPGA evaluation board to perform LAr trigger studies

Until now we have performed some LAr trigger studies using a FPGA demonstrator board and implementing algorithms in it (Figure 4). To do more accurate studies (eg, timing) we would like to assemble a more complex set-up. We would like to buy an ATCA crate and build a dedicated board to host the FPGA (eventually using an AMC mezzanine for more flexibility). The board includes also an ATCA interface and a GbE Ethernet connection. The board should be able to host various FPGA types. We plan to acquire few FPGA and select the one more suitable for our implementation (based on number of gates, I/O and clock speed). We also need to build a board (ROD injector) that will simulate the input data flow.

We want to study how to handle the expected data flow from the calorimeter, how to arrange and partition the data and algorithms to select EM clusters (or other objects). Detailed simulations to study the impact on selected physics channels will be performed.

The hardware set-up will be used as a demonstrator to study efficiency, latency,… and identify possible bottlenecks of a given configuration.

Other Institutes in the LAr collaboration might be interested in collaborate on this topic: BNL, LAPP, San Paolo, Dresden and the Institutes in the L1CALO group (RAL, Cambridge, Michigan,…). Developments in this field might also have synergies with other ATLAS sub-systems and other Institutions working on ATLAS trigger. In the context of the IFD2014 Workshop it was investigated if possible synergies with CMS-Italia could be established but none were found. Some of us participate with this activity to the PRIN 2013 HTEAM which will provide funds to hire an AR for 2 years.

Financial requests

DC powering

2015: We estimate: 10 keuro to acquire new components and modify the CAEN prototype with new GaN MOSFETs; 10 keuro to acquire commercially available power modules;

2016: 5 keuro to prepare a test set-up (test load,...); 15 keuro beam time to perform radiation tests of components and modules.

2017: based on the study of the first two years, we have selected the design and the components needed and we are ready to lunch the production of a full prototype: 20 keuro.

LAr trigger

2015: 20 keuro for the test set-up (ATCA crate, components of the board)

2016: 15 keuro to produce the test board for the FPGA

2017: 8 keuro to complete the set-up with a ROD injector board

In summary:

	2015	2016	2017	Total:
DC powering	20	20	20	60
LAr trigger	20	15	8	43
				103

Milestones

DC powering

2015: Validation of GaN devices and commercial power bricks

2016: Test of custom and commercial solution and choice of which of the two to pursue

2017: finished design of full prototype with LAr specs and ready for production of prototype

LAr trigger

2015: Start assembly of the test set-up with the acquisition of the ATCA crate and design of the board ready; simulation started: selection of physics channels and needed samples.

2016: production of the board; set-up ready to do study and optimization of trigger algorithm

2017: more complete test of the performance of the test stand with the addition of the ROD injector; finalization of simulation studies.

Manpower

The consistency of the group as of today:

Name		% LAr
L. Carminati	RU	50
M. Citterio	DT	20
M. Fanti	RU	50
M. Lazzaroni	PA	70
S. Mazza	Ph.D. student	60
C. Pizio	AR	50
S. Resconi	Ric	50
F. Tartarelli	PR	100
R. Turra	AR	50
1 AR PRIN (to be hired)	AR	100
		10 persons/6 FTE

M. Lazzaroni and M. Citterio will follow the DC powering activity. M. Lazzaroni was the Milano responsible for APOLLO during third and last year of this project; M. Citterio was one of the main promoter of this R&D. M. Lazzaroni will continue to be the responsible of this activity with the support of Mauro and of two technicians. Both M. Lazzaroni and M. Citterio are involved in the same activity for the Phase I upgrade. We don't think this is a problem as these are exactly the same problematic and the Phase II activity is a natural evolution of the Phase I studies. Knowing exactly what are the problems and features of setting up the DC powering for Phase I will help in selecting the new LVPS for Phase II and in design the power section of the more complex FEB2 boards. We think both activities can be carried on in parallel without any negative side effect on the Phase I activity.

L. Carminati, F. Tartarelli, S. Mazza and the AR hired with PRIN funds will work on the LAr triggering: assembly of the set-up and development of the algorithms. M. Citterio and the electronics service will help with the set-up of the test stand and the design of the board. R. Turra, C. Pizio, S. Resconi will perform simulation of the performance of the full trigger chain.

Bibliography

[1] The ATLAS Collaboration, "Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment," *CERN-2012-022, LHCC-I-023,* 2012.

[2] P. Tenti, G. Spiazzi, S. Buso, M. Riva, P. Maranesi, F. Belloni, P. Cova, R. Menozzi, N. Delmonte, M. Bernardoni, F. Iannuzzo, G. Busatto, A. Porzio, F. Velardi, A. Lanza, M. Citterio and C. Meroni, "Power supply distribution system for calorimeters at the LHC beyond the nominal luminosit," *JINST,* vol. 6, p. P06005, 2011.

[3] M. Alderighi, M. Citterio, M. Riva, S. Latorre, A. Costabeber, A. Paccagnella, F. Sichirollo, G. Spiazzi, M. Stellini, P. Tenti, P. Cova, N. Delmonte, A. Lanza, M. Bernardoni, R. Menozzi, S. Baccaro, F. Iannuzzo, A. Sanseverino, G. Busatto, V. De Luca and F. Velardi, "Power converters for future LHC experiments," *JINST,* vol. 7, p. C03012, 2012.