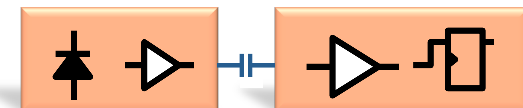
HV-CMOS at Genova

G. Darbo – INFN / Genova

HV-CMOS at Genova

Genova, 3 April 2014



HV/HR - CMOS

Indico agenda:

https://agenda.infn.it/conferenceDisplay.py?confId=7882

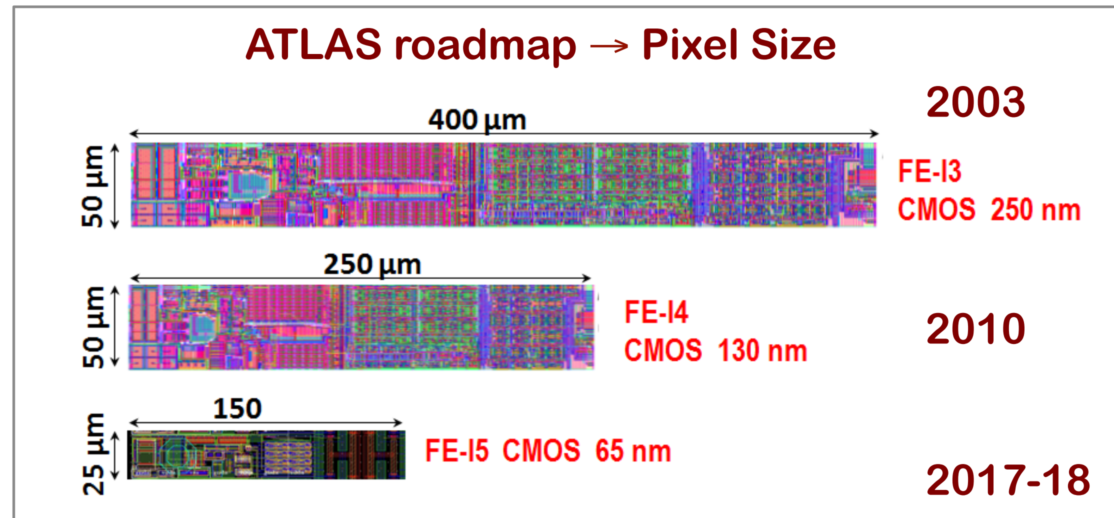
ATLAS Pixel Module R&D Roadmap

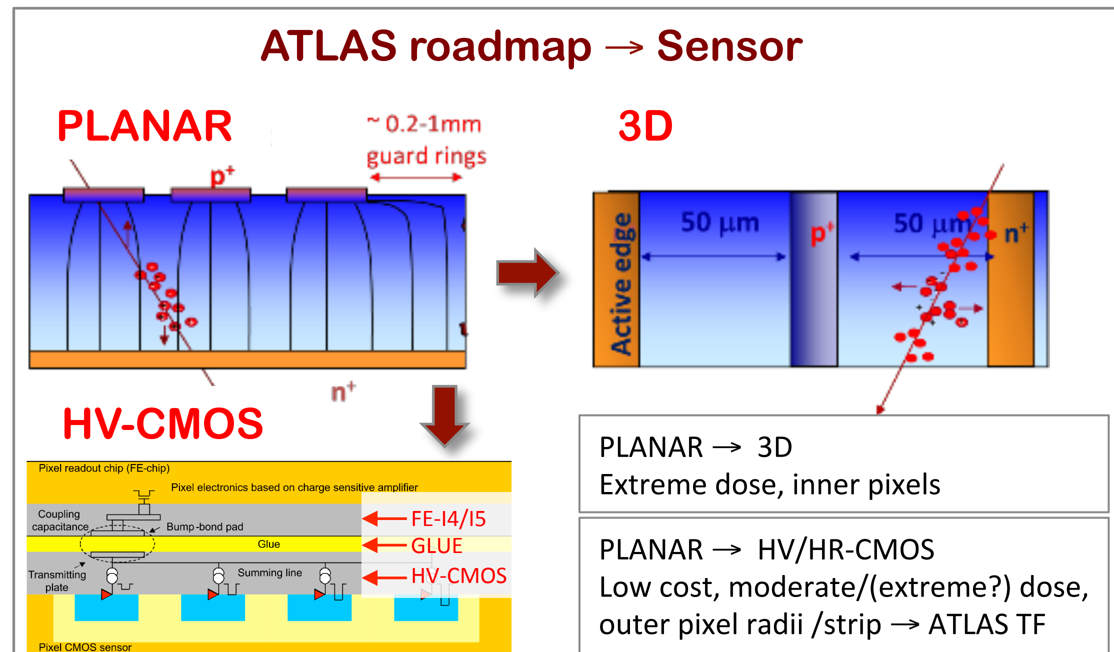
HL-LHC Tracker (2025)

- 638 MCh – area: 8.2 m^2
- 10÷20x TID/NIEL dose as today
- 6x event pile-up as today: 140 ev/BC

Enabling technologies

- *65 nm CMOS front-end* → hi-dose, small pixel size (25x100μm^2) → RD53
- 3D Sensor → low bias w.r.t. planar (<250 V from 1.5kV), larger collected charge per unit thickness
- HV-CMOS → use chip technology (8”÷12 cheaper wafer), glue vs. bump-bonding for modules. Challenging, but very promising → ATLAS Task Force *(TF)*



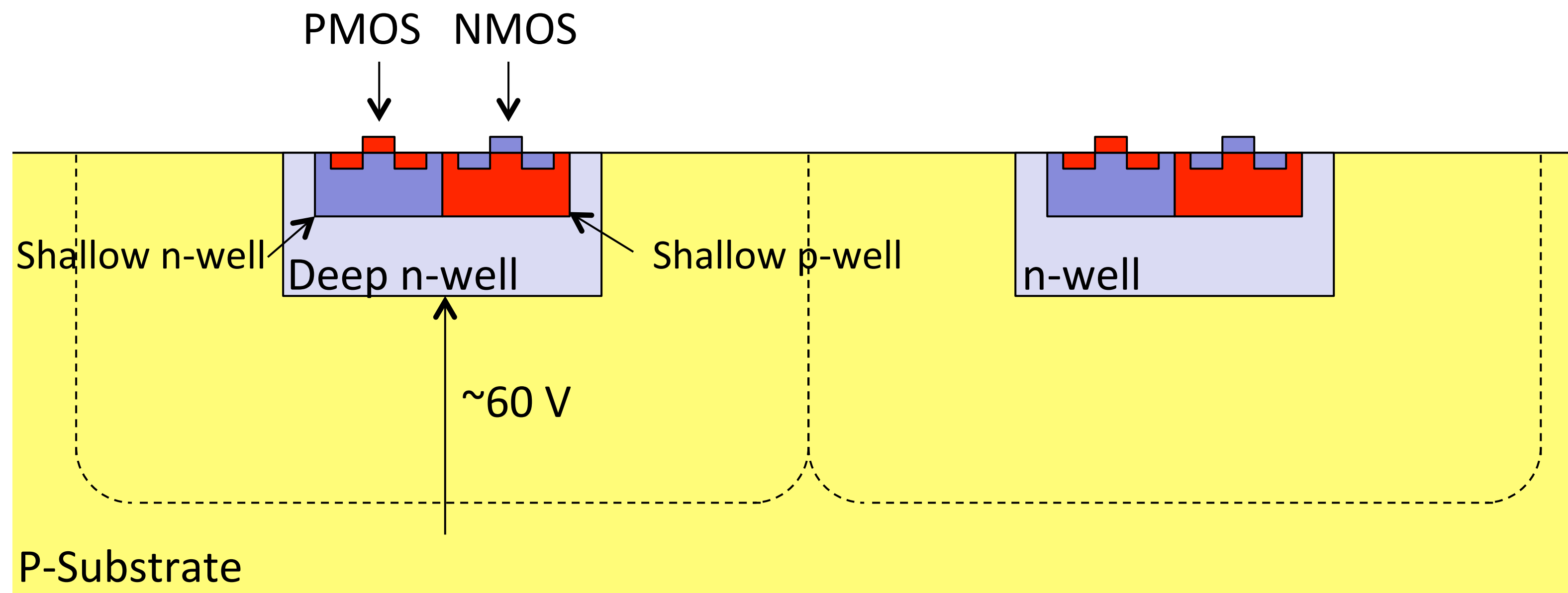


HV-CMOS – How they work

Idea:

- *Use the standard (HV-)CMOS technologies to implement particle detectors*
- *Use a high voltage to deplete the sensor volume – charge collection by drift*
- *Original Implementation: CMOS electronics inside the deep n-well-collecting electrode*
- *"Smart diode"*

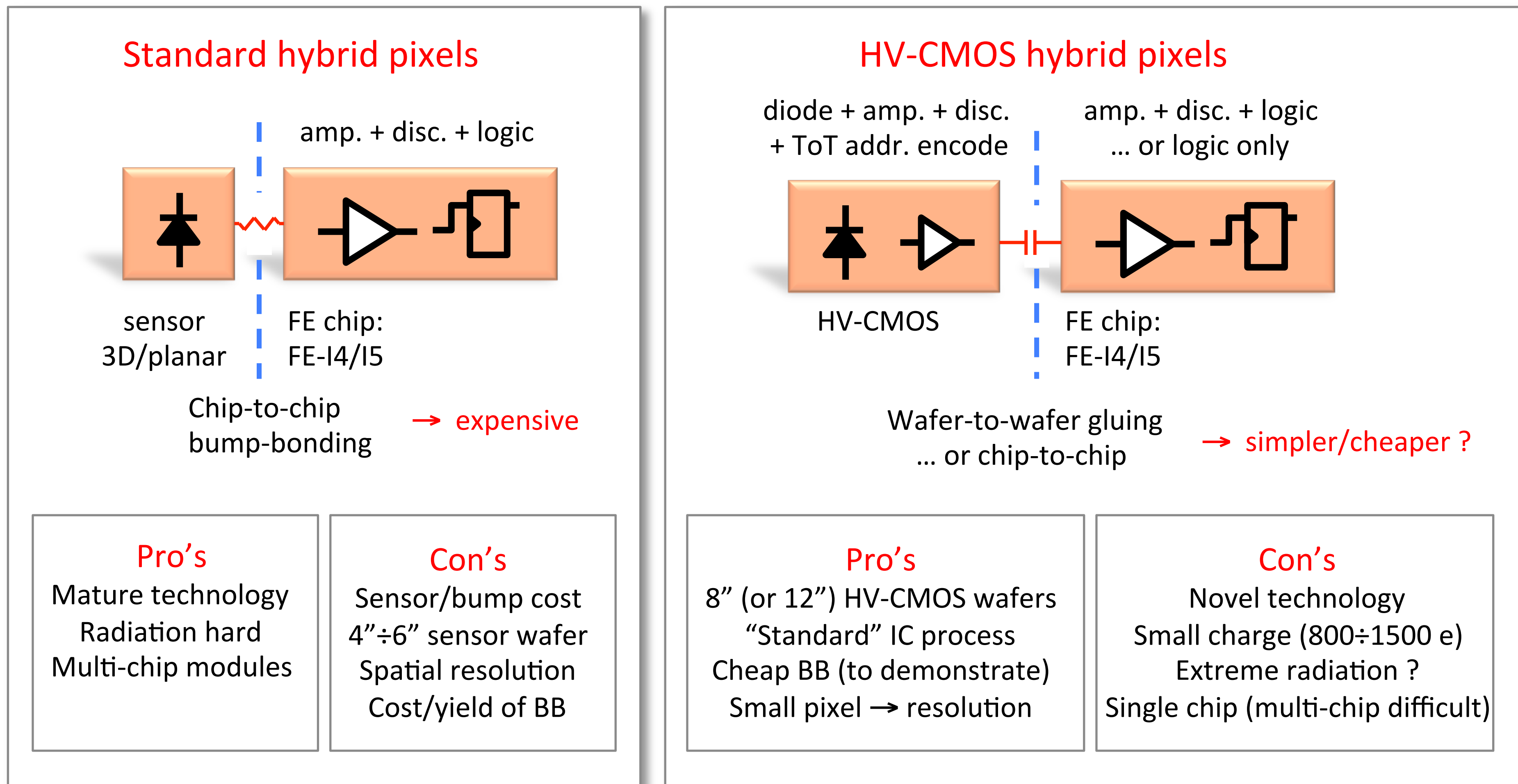
Ref.: I. Peric, Nucl. Instr. And Meth. A 582 (2007) 876–885



Hybrid Pixels: HV-CMOS

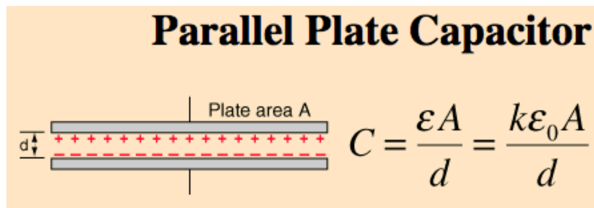
HV-CMOS as evolution of MAPS → Charge collected by drift vs. diffusion

Hybrid HV-CMOS → collection layer (high-voltage CMOS) separated by R/O layer

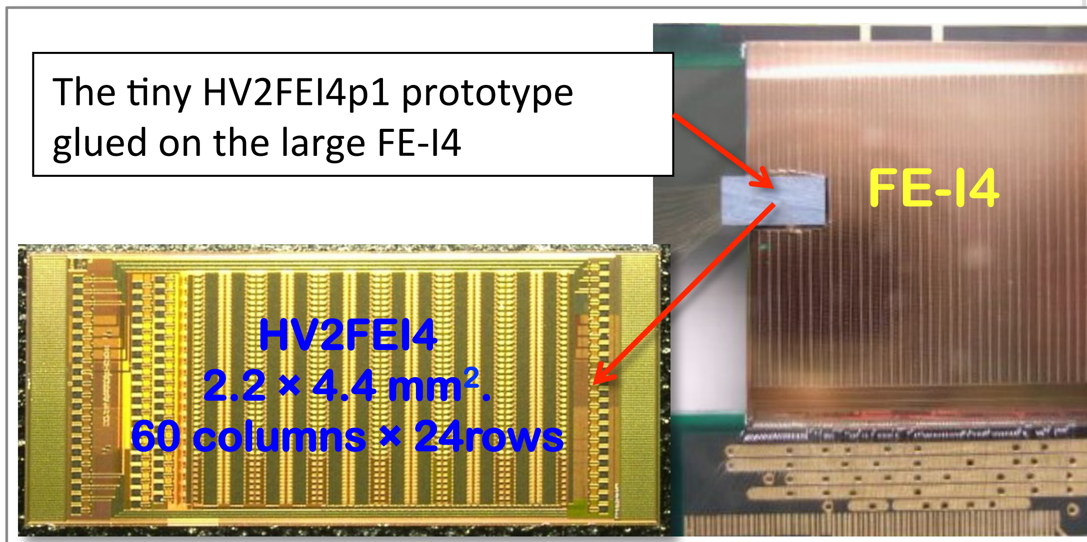


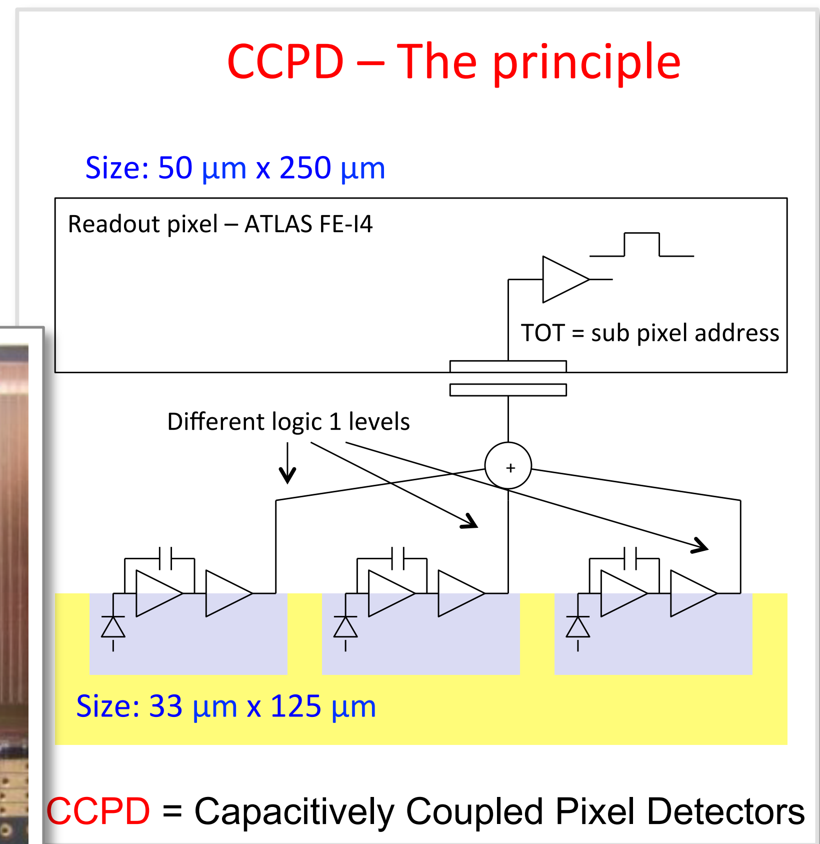
CCPD using HV-CMOS

- *The CCPD (Capacitively Coupled Pixel Detectors) are an hybrid detector using the HV-CMOS as preamplifier/discriminator and the FE-I4 as R/O chip*
- *The coupling is done using the FE-I4 bump-pads:*
  - Metal pad diameter = 18μm
  - 26800 pads/chip 50μm minimum pitch



  - For d = 5 μm and Ɛr = 2.2, C = 1fF





CCPD = Capacitively Coupled Pixel Detectors

Digression: Collaboration with STM

STMicrolectronics – Visit to Agrate

- *Nanni, Leo + Attilio Andreazza, Clara Troncon, Mauro Citterio, Valentino Liberali visit/contact with R&D group of STM in Agrate (4/3/2014).*
- *Design of a chip in collaboration with Ivan Peric + Eng. From MI, …*

Why STM could be interesting:

- *BCD8 Process Platform*
- *3-well process – better suitable for design (isolation between substrate and transistors)*
- *180 nm & 3.5 gate oxide (expected rad-hard)*
- *Up to 70 V process*
- *Replace epi-wafers with moderately resistive substrates (60-100 Ωcm – HR: high resistivity) – STM to decide soon, but looks (very) promising*

HV-CMOS → HV/HR-CMOS best of both worlds.

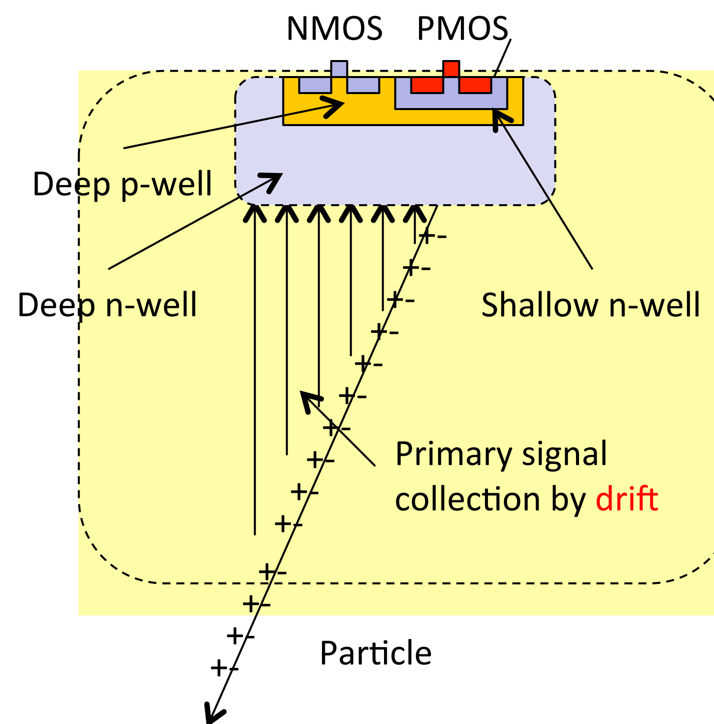
Direct collaboration with STM "insiders" is an advantage!

High (moderate) resistive substrates:

- around 80 Ωcm looks optimal:

$$V_{dep} \propto \sqrt{\rho * V_{bias}}$$

Uniformly doped substrate 80 Ω cm
Signal: ~ 2700e-4500e (estimation)



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COSA FARE A GENOVA

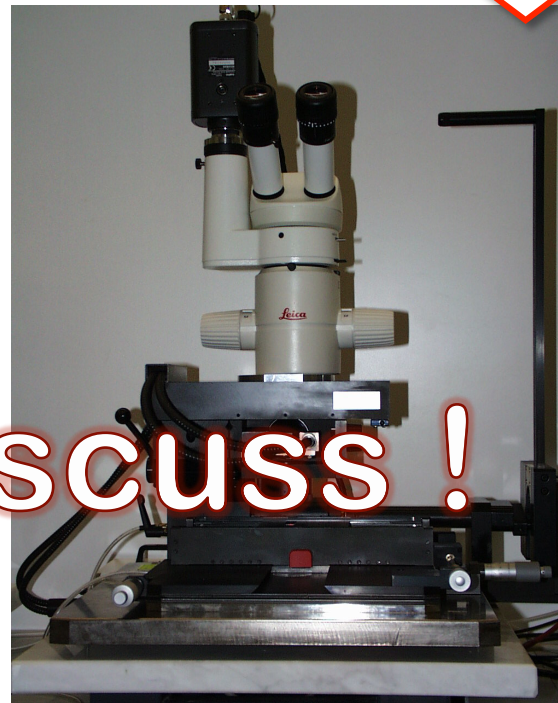
ASSEMBLY

Assembly of HV-CMOS/FE-I4

Procedure (idea to fully workout)

- Deposit US-8 photoresist by spinning → ~5 µm thick
- Use mask to pattern the photoresist → make spacer columns
- Deposit glue amongst columns
- Align FE-I4 to HV-CMOS → with old flip-chip machine?
- Apply pressure until columns are in contact

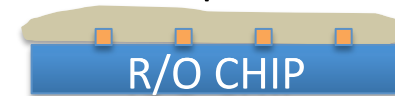
- Is feasible?



Let's discuss !

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition



Align & pressure

2x2 pillar height test:
- distance 4 mm
- height in µm

Pillar 1	5.92
Pillar 2	6.07
Pillar 3	5.92
Pillar 4	5.92

Low Temperature Detector facility – LTD Genova
Ref.: M. Biasotti et al., 9th "Trento" Workshop – Genova 26-28/2/2014

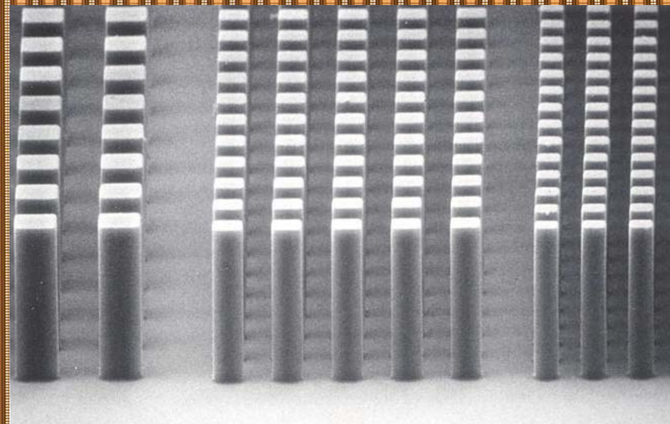
SU-8 2000

Permanent Epoxy Negative Photoresist

PROCESSING GUIDELINES FOR:

SU-8 2000.5, SU-8 2002, SU-8 2005, SU-8 2007, SU-8 2010 and SU-8 2015

SU-8 2000 is a high contrast, epoxy based photoresist designed for micromachining and other microelectronic applications, where a thick, chemically and thermally stable image is desired. SU-8 2000 is an improved formulation of SU-8, which has been widely used by MEMS producers for many years. The use of a faster drying, more polar solvent system results in improved coating quality and increases process throughput. SU-8 2000 is available in twelve standard viscosities. Film thicknesses of 0.5 to >200 microns can be achieved with a single coat process. The exposed and subsequently thermally cross-linked portions of the film are rendered insoluble to liquid developers. SU-8 2000 has excellent imaging characteristics and is capable of producing very high aspect ratio structures. SU-8 2000 has very high optical transmission above 360 nm, which makes it ideally suited for imaging near vertical sidewalls in very thick films. SU-8 2000 is best suited for permanent applications where it is imaged, cured and left on the device.



10 um features, 50 um SU-8 2000 coating

SU-8 2000 Features

- High aspect ratio imaging
- 0.5 to > 200 μm film thickness in a single coat
- Improved coating properties
- Faster drying for increased throughput
- Near UV (350-400 nm) processing
- Vertical sidewalls

Questions

- *Deposizione/spinning di SU-8*
  - Dove facciamo le prime prove di deposizione: vetrino? Chip FE-I3 (11x8 mm^2)? FE-I4?
  - Come misuriamo lo spessore? Usando il profilometro (installato dopo Pasqua)?
  - Abbiamo lo SU-8 che ci serve? Vogliamo procurarne altri? Quali?
- *Maschere*
  - Disegno delle maschere, che pattern, software, chi se ne occupa?
  - Quanti pattern disegnamo?
  - Che distanza tra le colonne? La stessa dei bonding pad? O a qualche mm di pitch?
- *Colla*
  - Come depositiamo la colla? Che colla usiamo? SU-8 come colla?
  - È possibile per spinning avendo già le colonne? O lo facciamo sul secondo chip?
  - Con dispenser? Ma con colonne spaziate di ~mm (tra le colonne)?
  - Cosa succede se ci sono delle bolle (mancanza di dielettrico → variazione della capacità)

Questions 2

Allineamento

- Come allineamo (un chip piccolo per iniziare)?
- La macchina del flip-chip è usabile? Il campo di vista è piccolo, come ci assicuriamo che ci sia un allineamento globale?
- Facciamo una prova con vetrino? Ma come verifichiamo che avremmo fatto un buon allineamento? Colonne e colla sono trasparenti. Un avolta incollato non abbiamo riferimenti.

Misure meccaniche

- Come misuriamo l'uniformità dell'altezza delle colonne?
- Come verifichiamo, anche in modo distruttivo, che abbiamo assemblato correttamente un FE-I4/HV-CMOS? Ossia allineamenti e spessore?

Misure elettriche

- Possiamo fare misure di capacità? Va realizzato un chip con pattern di metallizzazioni che permetta di misurare la capacità tra chip sotto e quello sopra. Ad esempio microstrips.

BACKUP SLIDES

HV-CMOS: Achievements

Irradiated to 1x10^{15}, 1x10^{16} n_{eq}/cm^2

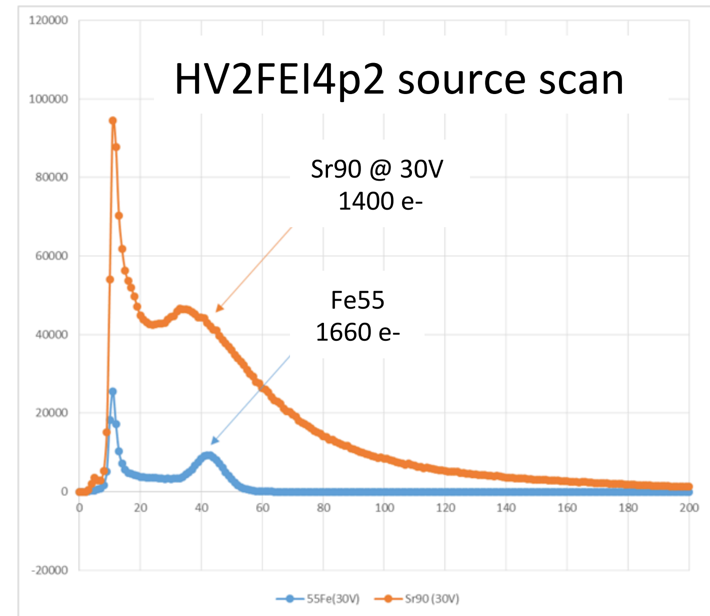
- source scan with ~25 V_{bias}
- still alive, noise occupancy ~10^{-10}

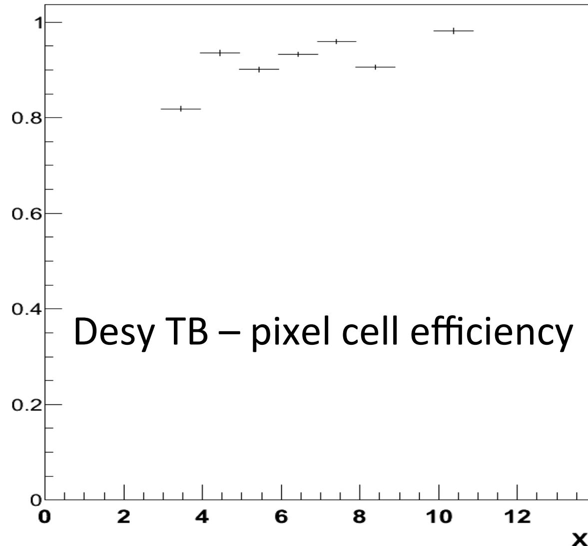
… and 862 Mrad.

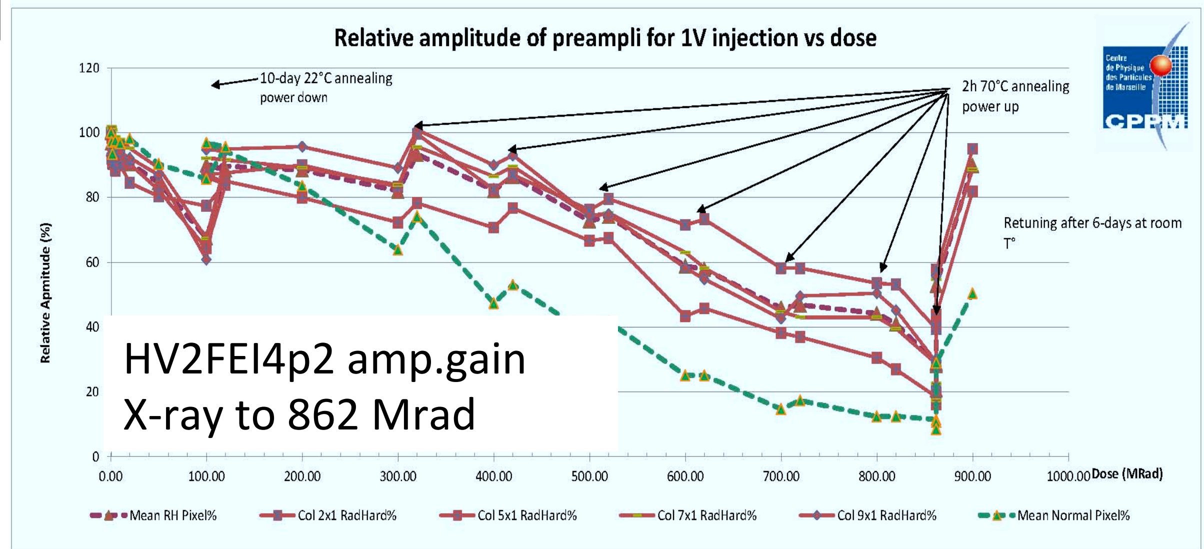
- Amplifier recovers at 90% of original value after annealing

Test beam (preliminary – need understanding)

- Efficiency: 90÷95% → calibration or E_{field} border effect?
- Time resolution: ~60% in time → time slewing?







ATLAS Technology Inventory

AMS H35

- Early prototypes done in this process. High breakdown voltages (> 100V) – somewhat elevated power consumption

AMS H18/IBM 7HV

- Currently the main development process: HV2FEI4 and other chips

GF 130nm HV

- HV process by GlobalFoundries in even smaller feature size, used to implement the HV2FEI4_GF. Actual experimental breakdown voltage is ~30 V before irradiation.

TowerJazz 180 nm High Resistivity Process

- Bonn testing. Possibly a process for monolithic detectors

IBM 130 nm with Triple Well (T3) Process

- attractive as it is the process of the FE-I4 readout chip, it is not an HV/HR process and therefore does not allow high bias voltages leading to rather low signal-to-noise values.

TSMC 65 nm process

- Process selected for future FE-I5 chip. Probably not for CCPD

Documentations

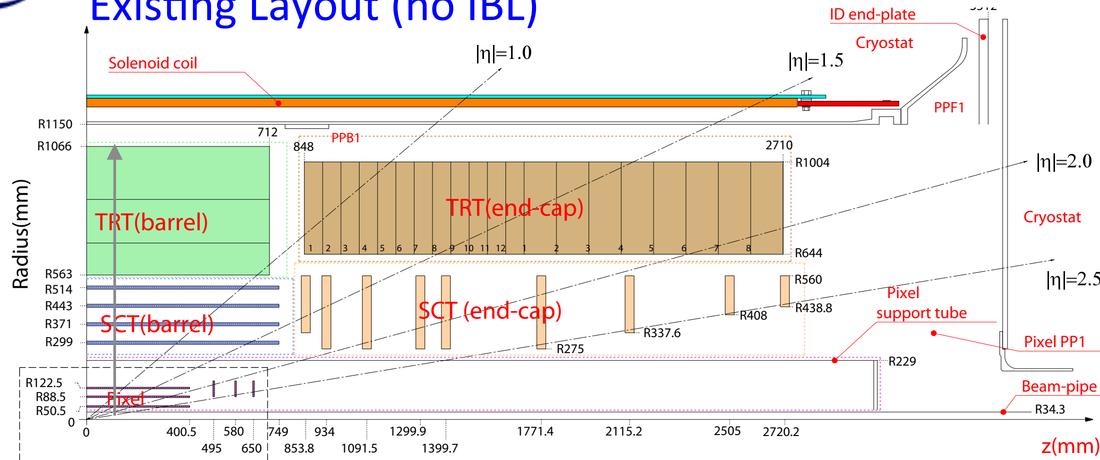
Talks:

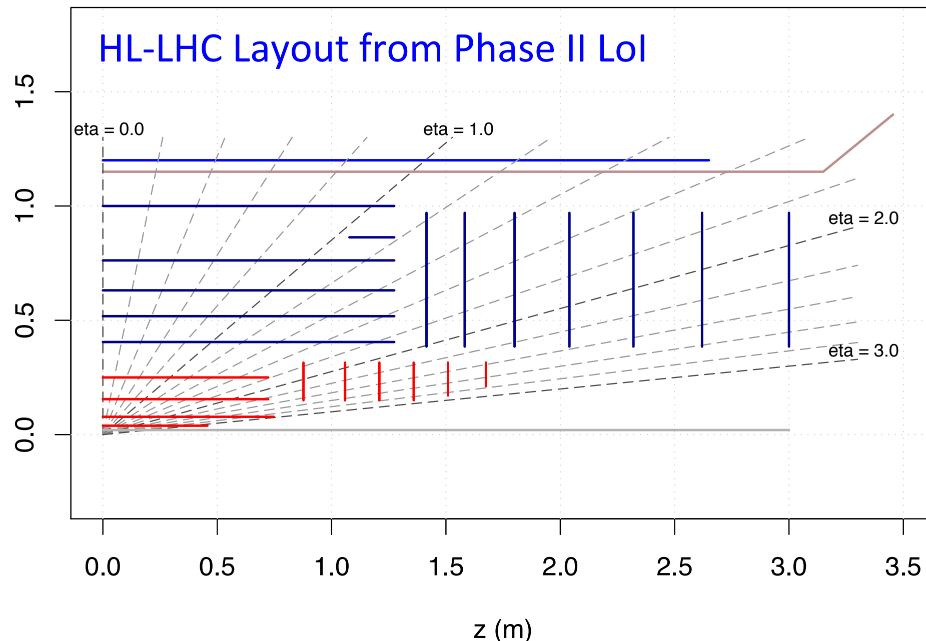
- Ivan Peric, HV-CMOS Overview, at 9th Trento Workshop, Genova 26-28/02/2014 http://indico.cern.ch/event/273880/session/5/contribution/64/material/slides/1.pdf
- Malte Backhaus, Radiation-hard Active Pixel Sensors for HL-LHC Detector Upgrades based on HV-CMOS Technology, at 9th Trento Workshop, Genova 26-28/02/2014: http://indico.cern.ch/event/273880/session/5/contribution/65/material/slides/0.pdf

Papers

- I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage cmos technology, Nucl. Instr. and Meth. in Phy. Res. A 582(2007)876-885.
- I. Peric, C. Kreidl, and P. Fischer. Hybrid pixel detector based on capacitive chip to chip signal- transmission. Nucl. Instr. and Meth. in Phy. Res. A 617(2010)576-581.
- I. Peric. Active pixel sensors in high-voltage CMOS technologies for ATLAS. JINST 7(08):C08002, 2012.

HL-LHC Tracker Layout





LHC Tracker (2012)

- *Pixel*
  - 80.3 + 11.4 (IBL) Mch – area: 1.7 m^2
- *Strip*
  - 6 Mch – area: 63 m^2
- *Dose (Pixel/IBL):*
  - 1.0 x 10^{15} n_{eq}/cm^2 (B-Layer)
  - 5.0 x 10^{15} n_{eq}/cm^2 (IBL)
- *Ev. pileup: 24 (design), 37 in 2013*

Pixel, Silicon strips, TRT

HL-LHC Tracker (2025)

- *Pixel*
  - 638 MCh – area: 8.2 m^2
- *Strips*
  - 74 Mch – area: 193 m^2
- *Dose:*
  - 2.0 x 10^{16} n_{eq}/cm^2
- *Ev. pileup: 140÷200 (design)*

All silicon, longer barrel: pixel up 2.7 in |η|
(A TF is studying extension to |η|=5)