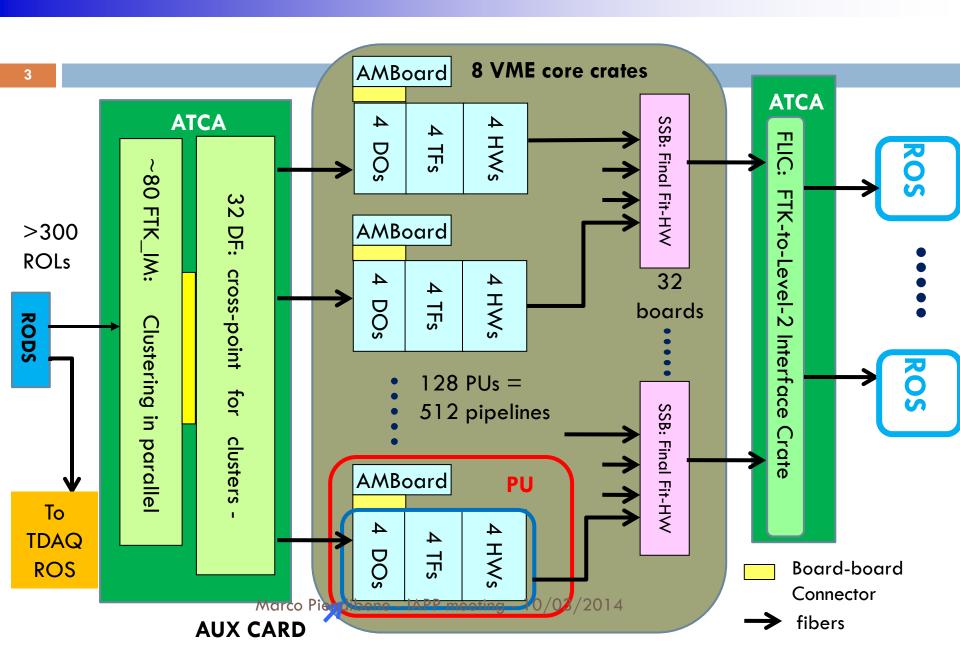
# AUXBOARD AND AMBOARD INTEGRATION @ CAEN

Piendibene & Magalotti for the IAPP collaboration

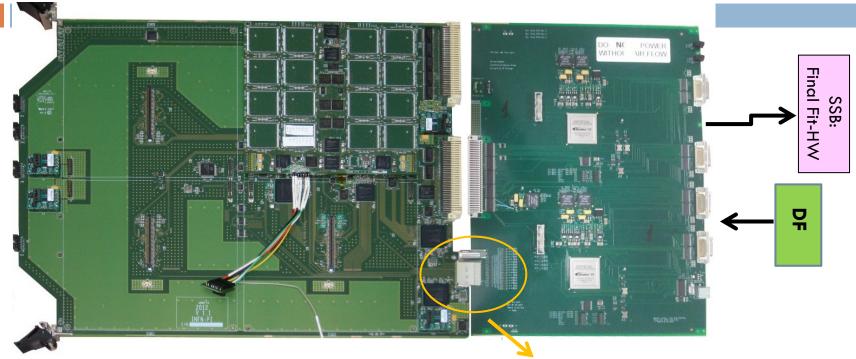
#### Outline

- Processing Unit (PU)
- Amboard (AMBFTK)
- AUXboard (protoAUX)
- Integration @ CAEN
- Integration @ University of Chicago
- Next steps

#### FTK global view (just to remember)



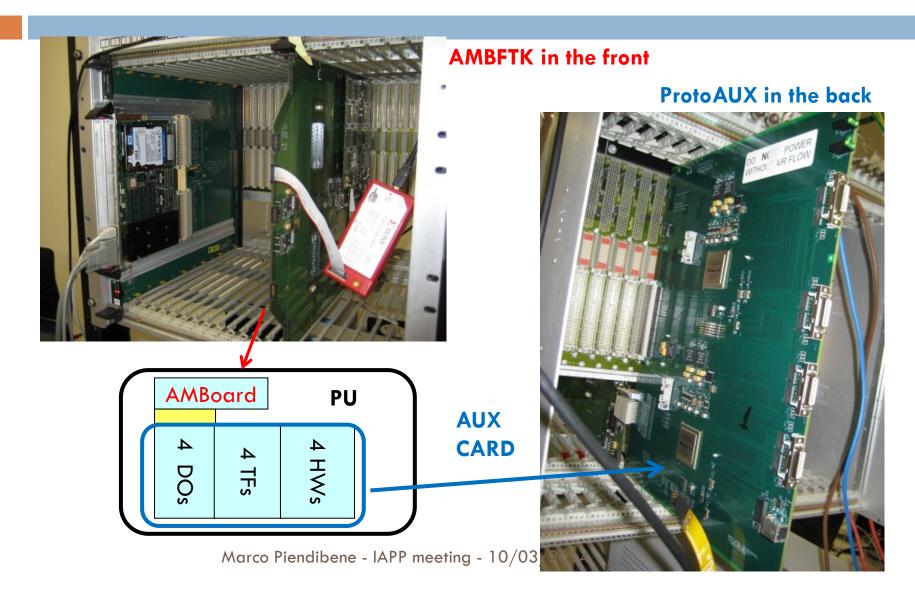
### Processing Unit (PU)



12+16 = 28 serial link @ 2GHz!

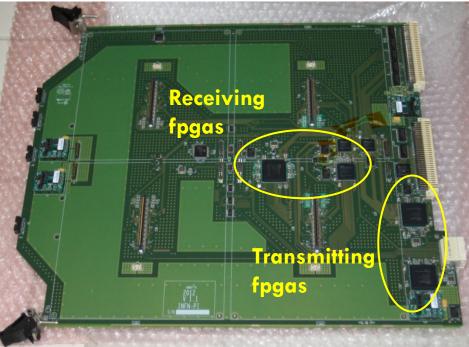
- 128 PUs do pattern matching and the 1<sup>st</sup> stage track fitting.
- A PU consists of an Associative Memory board (AMBFTK on the left) and a large Auxiliary Card (protoAUX on the right)

#### ...in the crate



### Amboard (AMBFTK)





- AMBFTK: prototype of the final board (AMBSLP)
- Connection with the LAMBs (mezzanines which host AMchip) partially serial and partially parallel
- Communication with ProtoAUX totally serial, like the final version



To/from AMBoard

### AUXboard (protoAUX)



- protoAUX: prototype of the final board (AUXboard)
- Communication with AMBFTK totally serial, like the final version

### Integration

- Firmware for both AMBFTK board and AUX board has been developed
- to test the pattern matching function (AMBFTK)
- to test the VME access to both AMBFTK board and AUXboard
- to test the exchange of data between the two boards through the high speed dedicated connector (P3): 28 links @ 2Ghz!

### Integration and test @ CAEN

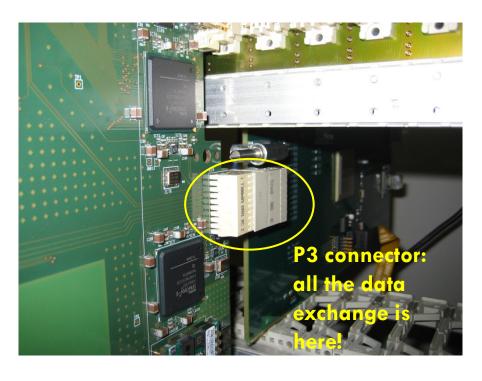




- VME access: after some patches (there was problems on the cpld that distribute VME address and data to the protoAUX) → OK
- Transmission on the high speed connector: after a lot of work to understand correct configurations of the trasceiver and terminations of the PCB traces →OK (28 serial link @2 Ghz) ☺

### P3 communication tests @CAEN

Transmission between Altera (protoAUX) and Xilinx (AMBFTK) transceivers (28 links @ 2GHz)



- Lock of the internal PLL of each transceiver: OK
- Alignment of the transceivers: OK
- Transmission of a known sequence (counter): OK in both directions
- Data integrity has been verified using spybuffers and fpga internal logic analyzers (chipscope and signal tap)
- Needs intensive tests

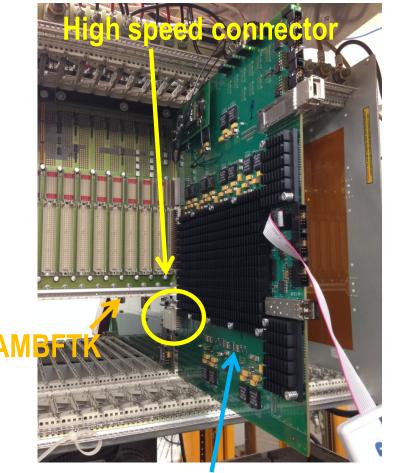
## Integration and test @ UOC

#### Not so warm in Chicago!



- The AMBFTK board has been sent to University of Chicago
- Daniel has been sent too ©
- Transmission test between AMBFTK board and the final AUXBOARD has been performed

### P3 communication tests @UOC



- Daniel @ UOC
- Final AUXboard with AMBFTK
- Transmission in both directions
  → OK
- 16 + 12 = 28 links @ 2Ghz are working perfectly! ©
- Needs intensive tests, but we are in good shape! ©

### Next steps

- test with
  - AMBSLP (final AMboard) with protoAUX
- and then...
  - AMBSLP (final AMboard) with AUXBOARD (final)!
- We need also to understand how to use the new crate CPU (VP717) with the version 4 of the TDAQ software – work in progress.

#### conclusions

- The most challenging thing, the high speed communication through the high speed P3 connector, seems to be OK! (but needs intensive tests)
- We need to perform the same test with the final version of the boards
- □ The processing unit (PU) integration has started. Up to now all is OK! ⓒ