Deleverable 8.2 – AUTH Training 2014 – Thessaloniki

Author: Calliope-Louisa Sotiropoulou (AUTH)

On Wednesday 12th of March and Thursday the 13th of March Aristotle University offered the third FTK IAPP Training. The training was offered in the Computer Laboratory of the Computational Physics Post-graduate program in the Department of Physics where 12 computer workstations were available with fully installed software to the participants of the training. Also 10 FPGA Development boards by Xilinx were available to the participants for use during the laboratory exercises.

The instructor of the training was Calliope-Louisa Sotiropoulou (PhD candidate and researcher in Aristotle University of Thessaloniki), assisted by Panos Neroutsos and Savvas Varsamopoulos (post-graduate students). Christos Gentsos (PhD candidate and researcher in Aristotle University of Thessaloniki) assisted in preparing the laboratory exercises offered. Dimitrios Porlidas (Post-graduate student) made a presentation of an FPGA implementation of a waveform generator.

The program of the training was the following:

Wednesday the 12th of March

- 10.00: Introduction to FPGAs
- 10.45: Introduction to VHDL
- 11.30: Break
- 12.00: Waveform generator (by Dimitrios Porlidas)
- 12.45: Break
- 14.00: Embedded Systems Lab Training (Xilinx EDK/SDK with Spartan 3E boards)
- 17.00: Introductory FPGA lab (for beginners)

Thursday 13th of March

- 10.00: Machine Vision for Biomedical Applications by AUTH eLab
- 11.00: Break
- 11.30: Machine Vision for Biomedical Applications by AUTH eLab

- 12.30: Break
- 14.00: Introduction to Vivado HLS Tool
- 16.00: End of Training

The program was adapted so that beginners and experienced FPGA users could gain from the training. The two first courses on Wednesday were introductory courses on FPGAs and VHDL design. The presentation of Dimitrios Porlidas was on a waveform generator implemented on a Spartan 3E FPGA device. The waveform generator prototype was also brought to the lab and a demonstration was provided by the presenter. The Embedded Systems Lab Training was on the use of the EDK tool of the Xilinx Toolchain to include a microblaze processor with peripherals on FPGA embedded systems. The laboratory included step by step instructions on the system implementation and use of the Spartan 3E development boards for practice. A processor system with use of a VGA driver for output was implemented by the participants. The second laboratory of the day was provided for the beginners in the use of FPGA devices. It was an introductory laboratory for designing, verifying, implementing and testing a simple up-down counter with led output on the Spartan 3E development board.

On the second day the previous work and experience of the AUTHeLAB team on FPGA design and participation to research projects was also presented to the collaboration. The work presented was on a Machine Vision implementation for microfluidic Lab-On-Chip devices. The project included use of common powerful image processing algorithms on FPGAs. These image processing algorithms are also used in HEP applications. The last laboratory was an introductory lab on the use of Vivado HLS (High Level Synthesis tool). This tool can accept as input a common (non HDL) programming language such as C/C++ and implement it as HDL type firmware on generation 7 FPGA device by Xilins (Artix 7, Kintex 7, Virtex 7). Such a tool is useful for people with little or no experience in HDL that want to design a hardware accelerator fast.

The slides from the training are available on the collaboration website:

http://ftk-iapp.physics.auth.gr/Collaboration/Docs/TrainingSlides/

In the training participated the following researchers and students:

Paola Giannetti (INFN)
Marco Piendibene (UniPisa)
Simone Donati (UniPisa)
Daniel Magalotti (University of Modena)
Saverio Citraro (UniPisa, INFN)
Pierluigi Luciano (INFN)
Francesco Crescioli (CNRS)
Akis Gkaitatzis (AUTH)
Despina Sampsonidou (AUTH)
Andreas Sakellariou (Prisma)
Konstantina Mermikli (Prisma)
Dimos Sampsonidis (AUTH)
Kostas Kordas (AUTH)
Student from AUTH Electronics Engineering Department

Figure 1. The presentation of Dimitrios Porlidas with the prototype demostrator waveform generator