Solid State Sensor Poster Review

27 posters in 20 minutes ➔ 44.44 secs / topic
Be prepared 😊
### Overview

| ATLAS | Alignment of the ATLAS Inner Detector Tracking System  
ATLAS Silicon Microstrip Tracker Commissioning and Silicon Sensor Performance  
Results from the Commissioning of the ATLAS Pixel Detector with Cosmics Data |
|--------|--------------------------------------------------|
| CMS | Data Quality Monitoring of the CMS Silicon Strip Tracker Detector  
CMS Silicon Strip Tracker Operation in Cosmic Run at Four Tesla |
| ALICE | The Silicon Drift Detector of the ALICE Experiment  
The ALICE Silicon Pixel Detector Read-Out Electronics |
| LHCb | First Experience and Results with the LHCb Silicon Tracker |
| CDF | Longevity Studies in the CDF Silicon Detectors  
Operational Experience with the CDF Run II Silicon Detector |
| Future detectors (e.g. B-factories) | Silicon vertex detector upgrade for SuperKEKB factory  
The SuperB Silicon Vertex Tracker |
| 3D & RD | 3D Silicon Detectors for LHC Upgrades  
Characterization and Modelling of Signal Dynamics in 3D-DDTC Detectors |
| SLIM | SLIM5 Beam Test Results for Thin Striplet Detector and Fast Readout Beam Telescope  
Investigation of an abnormal pattern of the strip leakage currents in microstrip detectors |
| "other devices" | Laser and Alpha Particle Characterization of a Floating-Base BJT Detector  
Study of Geiger Avalanche Photo Diodes (GAPD) Applications to Pixel Tracking Detectors  
Characterization of CMOS Active Pixel Sensors for Particle Detection: Beam Test of the Four Sensors RAPS03 Stacked System |
| Generic supporting studies | Development and Experimental Characterization of Prototypes for Low Material Budget Support Structure and Cooling of Silicon Pixel Detectors, Based on Microchannel Technology  
Optimising the Strip Geometry for very Fine Pitch Silicon Strip Sensors  
Lithium Diffusion into Silicon-Germanium Single Crystal |

Unfortunately not all slides nor posters are in Indico, Fortunately I have a digital camera. I tried my best.
LHC DETECTORS
Regina Moles (IFIC – Valencia)

ALIGNMENT OF THE ATLAS INNER DETECTOR TRACKING

Heinz Pernegger (CERN Physics Department)

ATLAS SILICON MICROSTRIP TRACKER COMMISSIONING AND SILICON SENSOR PERFORMANCE

Jens Weingarten (Dortmund University)

RESULTS FROM THE COMMISSIONING OF THE ATLAS PIXEL DETECTOR WITH COSMICS DATA

A summary was already given on Monday, more details on the posters. They are really worth three looks (each)!
• Assembly and **survey** measurements:
  - External measurements of the as-built detector

• **Frequency Scanning Interferometry**: SCT is equipped with a laser alignment monitoring system

• **Track based** alignment algorithms:
  - To achieve the ultimate precision (μm)

The use of real cosmic ray data has allowed us to obtain a first set of alignment constants for the real detector.

**The ATLAS ID is ready to reconstruct the first LHC collision tracks.**
Impressive results achieved during commissioning and cosmic data taking last year

- TOT threshold scan
- Lorentz angle
- Hit efficiency 99.8%

To name a few
• Heinz Pernegger (CERN Physics Department)

**ATLAS Silicon Microstrip Tracker Commissioning and Silicon Sensor Performance**

• Commissioned ATLAS Silicon Strip SCT during 2008
  – Stable readout in ATLAS with low noise
  – Test SCT tracking performance with Cosmics

• Readout in 2008 99% of Barrel and 97% of Endcap modules

• Efficiency >99%

• Noise Occupancy $\sim 2-5 \times 10^{-5}$ (specs $5 \times 10^{-4}$)

• First round of alignment with cosmics tracks (2M tracks in SCT) very successful
Leonardo Benucci (University of Antwerp)

**DATA QUALITY MONITORING OF THE CMS SILICON STRIP TRACKER DETECTOR**

Vitaliano Ciulli ((Univ. di Firenze e Sez. dell' INFN,)

**CMS SILICON STRIP TRACKER OPERATION IN COSMIC RUN AT FOUR TESLA**
Data Quality Monitoring (DQM) is being built to provide complete and coherent monitoring data (online and offline) at low latency, to ensure the optimal working of the hardware and software and to certify the quality of the data for analysis in an efficient way.

**WHAT DQM MONITORS (Monitor Elements, ME):**
- RAW data (readout and unpacking errors)
- DIGIS and Cluster (related or not to a track)
- track parameters
- Hit residuals

The data quality is assessed through histograms (about 300,000 histograms defined).

**HOW DQM MONITORS:**
- Producers (source) book and fill ME
- Consumers (client) access ME and produce
- Summaries to merge informations from each histogram of each module

**Quality tests:**
compare with reference histograms or reference values

visualize with Graphical User Interface (GUI)

→ **CMS DQM GUI is web based: it is accessible from everywhere a web browser is available**
Data Quality Monitoring of the CMS Silicon Strip Tracker Detector

Leonardo Benucci - University of Antwerp, Belgium

DQM OFFLINE
operates @ Tier 0/1 - within day/hours
- Re-assess Tracker status using full reconstruction and best calibration constant
- spot reconstruction, calibration or other
- unexpected problems

DQM ONLINE
operates @ Point5 (CMS site) during data taking
- give prompt feedback to Tracker experts about hardware status
- identify problems very efficiently during data collection to take prompt actions

Data Bookeeping System (data for Physics)

CERTIFICATION PROCEDURE
prepare Tracker flag on data quality before storage
- checks from shifters
- detect and flag new or temporary Tracker problems and classify each run according to hardware, reconstruction and calibration conditions
- → Enable any user to consult the certification results and select suitable runs for specific commissioning/physics analysis tasks
Data Quality Monitoring of the CMS Silicon Strip Tracker Detector

Leonardo Benucci - University of Antwerp, Belgium

Data Quality Monitoring (DQM) is being built to provide complete and coherent monitoring data (online and offline) at low latency, to ensure the optimal working of the hardware and software and to certify the quality of the data for analysis in an efficient way.

CMS is as everybody else, waiting for the beam.
Mario Sitta (INFN - Torino)

The Silicon Drift Detector of the ALICE Experiment

Marian Krivda (IEP - Košice)

THE ALICE SILICON PIXEL DETECTOR READ-OUT ELECTRONICS
Silicon Pixel Detector (SPD): ~10M channels

Silicon Drift Detector (SDD): ~133k channels

Silicon Strip Detector (SSD): ~2.6M channels

Mainly calibration is described, e.g. Drift velocity and compensation efforts due to (due to non-linear voltage divider or dopant concentration inhomogeneties)
The readiness of the ALICE pixel detector is shown as well as detailed description of its readout electronics is given.
FIRST EXPERIENCE AND RESULTS WITH THE LHCB SILICON TRACKER
Tracker Turicensis Status
99% of the TT is fully working
- broken bonds
- HV problems
- optical path or acquisition board not ok
- problem with the SB
- commissioned

Status of August 2008 (Time of TED data taking)
The majority of problems are fixed for the runs of 2009-2010.

TED Data
- This is the main data-set so far. The particles are produced by dumping injection test bunched in a tungsten absorber 300m 'behind' LHCb.
- TED events are high multiplicity events, with an occupancy 20 times greater than in normal physics.
- It has been used for the spatial alignment of IT and TT, beyond the survey results that is 500µm accurate for boxes and 100µm for Layers and Ladders.

99% of the TT is fully working
SN, delay scan, Track finding and alignment done
THESE LHC DETECTORS ARE PROBABLY OVERCOMMISSIONED 😊
OPERATIONAL EXPERIENCE WITH THE CDF RUN II SILICON DETECTOR

Miguel Mondragon (Fermilab)

LONGEVITY STUDIES IN THE CDF SILICON DETECTORS

Roberto Martinez-Ballarin (CIEMAT-Madrid)

* Where LHC detectors can learn from
Operational Experience with the CDF Run II Silicon Detector

THE LEARNING OF EIGHT YEARS OF OPERATIONS

- The battle against corrosion in cooling lines and a remarkable repair
- The story of wirebond resonances and a protection system

And also...
- High automation of operations
- Ongoing maintenance
- Performance

Newer and future silicon detectors can make profit from these experiences

Miguel N Mondragon (Fermilab) for the CDF Silicon Detector Group
A real life study about radiation damage in silicon
The inner layers already passed the point of space charge inversion
→ depletion voltage increases but will still stay for a while below the applicable bias voltages
Samo Stanic (University of Nova Gorica)

**SILICON VERTEX DETECTOR UPGRADE FOR SUPERKEKB FACTORY**

Giuliana Rizzo (Università di Pisa/INFN)

**THE SUPERB SILICON VERTEX TRACKER**

- Design progresses
- Both will use additionally pixel sensor
- Several technology choices under evaluation
  - Hybrid pixels, DEPFET, CMOS, SOI (SOIPix; CAP)
  - Somehow also a test bench for ILC detectors

Not yet waiting for beam
Silicon Vertex Detector Upgrade for the Belle II Experiment
S. Stanič for the Belle SVD Group

Physics at extreme luminosity SuperKEKB collider:
(8 \times 10^{35}/cm^{2}/s after upgrade, \sim 2 \times 10^{34}/cm^{2}/s presently achieved by KEKB \Rightarrow \text{Realistic!})

Precision measurements of CPV in B decays
\bullet Study of time dependence of $B^0$ - anti-$B^0$ decays
\bullet Study of rare decay modes of beauty and charm hadrons and $\tau$

Design requirements for the Silicon Tracker:
\bullet Good resolution in the beam direction
\bullet Small amount of material inside the acceptance region
\bullet Operation at high radiation background rates and high track density (40 x present)

Silicon tracker upgrade plan:
\bullet \textbf{PXD} - \textit{Pixel} Detector (2 inner layers) - high precision
\bullet \textbf{SVD} - \textit{Strip} Detector (4 outer layers) - larger acceptance

SVD Layout:
\bullet System size 3-4x of the present Belle SVD2 (4 layers)
\bullet Use of \textbf{DSSD sensors} from 6” wafer, well established technology
\bullet Additional use of alternative “chip-on-sensor” sensor types (Lower number of readout chips, less material and power dissipation in acceptance region)
\bullet Readout with \textbf{APV25} (~ 50ns shaping time, sensitive window \sim 160ns)+ FADC+COPPER (Full DAQ chain already successfully tested in a beam test at KEK)

Conceptually proven, after finalizing the geometry ready for production.
Belle II PXD Layout (based on DEPFET):

- Small radius, as close as possible to the beam pipe
- High granularity sensors, pixel size about $50\times 75\mu m^2$
- Small detector 20-24 single sensor modules in two layers
- Total of $\sim 6$M pixels, frame readout rate <10μs
- Possibility of variable pixel in z-pitch to optimize charge sharing at large z and improve resolution in the central part

PXD Sensor R&D Status - 3 variants pursued:

- **CAP, KEK SOIPIX** (promising concepts, at basic R&D)
- **DEPFET** (Most promising candidate -

Evolving from basic R&D to production for Belle II)
- Pixel is a p-channel FET on a completely depleted bulk, deep n-implant creates a potential minimum for electrons under the gate
- $50 \times (75-115) \mu m^2$ pixels
- Frame readout time <10μs, sequential readout of pixels or rows
- Low power, ASICs at the periphery

Done:
- Successful beam tests
- Rad. hardness tests (80kGy): low noise
- GEANT4 simulation started

To do:
- Solve radiation related issues (threshold voltage shift is large)
- Consider mechanics/cooling design
- Consider DAQ interface (PXD may deliver up to 70Gbit/s)
Reduced beam energy asymmetry of SuperB (7x4 GeV) requires improved vertex resolution to reach performance similar to present B-Factories.

**Layer0 options under study for TDR-2010**

- **Hybrid Pixels**: viable option → baseline for TDR
  - Front-end pitch reduced to 50x50 μm² in a first prototype chip submitted by the end of 2009.

- **CMOS MAPS**: new & challenging technology but very promising → sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on Deep N-Well devices 50x50μm² with fast readout architecture.
    - CMOS MAPS matrix (4k pixels) with in pixel sparsification and timestamp successfully tested with beams.

- **Thin pixels with Vertical Integration**: 
  - Reduction of material and improved performance achievable with VI
  - First DNW MAPS (2 tiers) submitted with Chartered/Tezzaron 130 nm

- **Striplets**: thin double sided silicon sensor with short strips
  - mature technology, less robust against background occupancy.

**Vertex detector design based on current BaBar SVT + an innermost Layer0**

- Radius~1.5 cm, pitch 50 μm, X/X₀ ~1%, backg. > 5MHz/cm², TID ~1MRad/yr

**Fast Simulation**

- $B \rightarrow \pi \pi$ decay mode, $|\gamma|=0.28$, beam pipe X/X₀=0.42%, hit resolution =10 μm

**Notes**

- Under test

- 4 options
Layer0 R&D Recent Results

SLIM 5 Testbeam @ CERN (Sept 2008)

Successfully tested two options for Layer0

CMOS MAPS matrix with fast readout architecture (4096 pixels, 50x50 μm pitch, sparsification and timestamp)
- Hit efficiency up to 92% with room for improvement
- Intrisinc resolution ~ 14 μm compatible with digital readout.

Striplet module with FSSR2 readout chips
  - S/N=25 (thickness 200μm), Efficiency > 98%
  - More details: M. Villa - talk, L. Vitale - poster

MAPS Hit Efficiency vs threshold

Cross collaborative efforts:

Light support with integrated cooling for pixel module (P=2W/cm²)

Carbon Fiber support with integrated microchannel with coolant fluid developed:
  - Total support/cooling thickness ~ 0.3 % X₀

First thermo-hydraulic measurements on prototypes in good agreement with simulation.

More details: F. Bosi’s poster

Giuliana Rizzo
11th Pisa Meeting on Advanced Detectors –
24-29 May 2009
PRODUCTION AND PERFORMANCE OF THE SILICON SENSOR AND CUSTOM READOUT ELECTRONICS FOR THE PHENIX FVTX TRACKER
RHIC Experimental program in Heavy Ions

Center of Mass Energy: $\sqrt{s} = 200\text{GeV}$

and

Polarized Protons (Spin Program) $\sqrt{s} = \text{up to } 500\text{GeV}$

Extension into the forward regions of the Phenix Detector

A custom front-end chip, the FPHX, has been designed for the FVTX by the ASIC Design Group at Fermilab. The chip combines fast trigger capability with data push architecture in a low power design. The chip was fabricated in the TSMC 0.25 micron CMOS process.

FVTX Sensor Long Wedge

- 2 columns of strips
- 1664 strips per column
- strip length - 3.4 mm to ~11.5 mm
- 75 micron spacing
- 48 wedges per disk (7.5'/sensor, 15'/wedge)
- 0.5 mm overlap with adjacent wedges

Mini-strips are oriented to approximate an arc

Wedge; short strips 3.4mm - 11.5mm
Giovanni Mazza (INFN - Torino)

THE NA62 GIGATRACKER PIXEL DETECTOR SYSTEM
GigaTracker: 3 silicon pixel sensor stations for precise measurement of particle direction and timing.

Pixel size: 300 \( \mu \text{m} \times 300 \mu \text{m} \\
Sensitive area: 27 mm \times 60 \text{mm} \\
Time resolution: \(150 \text{ ps rms (total)} \) \\
\(200 \text{ ps rms (per station)} \) \\
Data rate: 0.8\text{–}1 \text{ GHz (total)} \\
\(1.5 \text{ MHz/mm}^2 \) (max) \\
Operational environment: vacuum

Detector to be operated below 5 °C to keep the leakage current under control

Design challenge: obtain a 200 ps resolution with silicon pixel detectors at very high particle rate.
ASIC prototypes

Two readout options are under investigation:

Pixel matrix: $40 \times 45$ cells.
Time walk compensation: Constant Fraction Discriminator (CFD).
Time measurement: on pixel TAC based TDC.
Reference clock: 160 MHz.
Four event buffers for data derandomization (on pixel).
SEU protected control logic.
  + each pixel operate independently.
  + only one long distance time critical signal (clock).
  - complex pixel circuitry.
  - more control logic on the beam trajectory.

Pixel matrix: $40 \times 45$ cells.
Time walk compensation: Time over Threshold (ToT) correction.
Time measurement: DLL based TDC at the end of the pixel column.
Reference clock: 320 MHz.
Pre-emphasis for signal transmission.
  + simple and low power pixel circuitry.
  + only one DLL based TDC needed (plus column registers).
  - many time critical signals to be sent to the EoC (one per pixel).
  - hit arbitration needed (possible event loss).

Prototypes of the analog part for the two options (preamp+CFD and ToT correction) have been designed in CMOS 0.13 μm and successfully tested.

Two test chip with the full pixel and column circuits are currently in production.

Gianni Mazza

11th Pisa Meeting on Advanced Detectors – 24-30 May 2009
various
3D & RD

3D gets more and more mature!
CINZIA DAVIA (THE UNIVERSITY OF MANCHESTER)

3D SILICON DETECTORS FOR LHC UPGRADES
Micromachined electrodes
- Active edges (dead edge <4μm)
- Large area coverage
- Fast+Radiation Hard (up to $10^{16}$ n/cm$^2$)
- Atlas pixel run completed - 10 wafers test beam shows 99.0% efficiency at 15° from incoming beam

Active Edges (C. Kenney): Wall electrodes enclosing the entire detector perimeter. Measured to be ~4 microns

Oscilloscope trace of a 3D detector + 0.25μm CMOS RO (design G. Anelli et al. CERN)

From ideas to real pieces and real results
Highlights from test beams

- Radiation hard due to high field and short inter-electrode spacing
- Test beam shows 99.0% efficiency at 15° from incoming beam -

Cinzia Da Via/Manchester May 2009

Key processing steps (25-32)

1-etching the electrodes

- Step 1-3 oxidize and fusion bond wafer
- Step 4-6 pattern and etch p⁺ window contacts
- Step 7-8 etch p⁺ electrodes

2-filling them with dopants

- Step 9-13 dope and fill p⁺ electrodes
- Step 14-17 etch n⁺ window contacts and electrodes
- Step 18-23 dope and fill n⁺ electrodes
- Step 24-25 deposit and pattern Aluminum

LOW PRESSURE CHEMICAL VAPOR DEPOSITION
(Electrodes filling with conformal doped polysilicon
SiH₄ at ~620°C)
2P₂O₃ + 5 Si → 4P + 5 SiO₂
2B₂O₃ + 3Si → 4 B + 3 SiO₂

Both electrodes appear on both surfaces

METAL DEPOSITION
Shorting electrodes of the same type
with Al for strip electronics readout
or deposit metal for bump-bonding

Cinzia Da Via/Manchester May 2009
Andrea Zoboli (Università di Trento)

CHARACTERIZATION AND MODELLING OF SIGNAL DYNAMICS IN 3D-DDTC DETECTORS
MIP penetrating from (30,30,0)

- MIP penetrating the device from (30,30,0)
- Evaluation of the current signal
- Two dimensional domain
- Full depletion not reached at the bottom
- Slow tail due to diffusion

Very interesting, have a look
RECENT ADVANCES IN THE DEVELOPMENT OF SEMICONDUCTOR DETECTORS FOR VERY HIGH LUMINOSITY COLLIDERS
Recent advances in the development of semiconductor Detectors for very high luminosity colliders

Frank Hartmann on Behalf of CERN RD50 Collaboration

http://www.cern.ch/rd50

Silicon Sensors
- p-in-n (EPI), 150 μm [7,8]
- p-in-p (EPI), 75μm [6]
- n-in-p (FZ), 300μm, 500V, 23GeV p [1]
- n-in-p (FZ), 300μm, 500V, neutrons [1]
- n-in-p (FZ), 300μm, 500V, 26MeV p [1]
- n-in-p (FZ), 300μm, 800V, 23GeV p [1]
- n-in-p (FZ), 300μm, 800V, neutrons [1]
- n-in-p (FZ), 300μm, 800V, 26MeV p [1]
- p-in-n (FZ), 300μm, 500V, 23GeV p [1]
- p-in-n (FZ), 300μm, 500V, neutrons [1]
- Double-sided 3D, 250 μm, simulation! [5]

Other materials
- SiC, n-type, 55 μm, 900V, neutrons [3]
- Diamond (pCVD), 500 μm [4] (RD42)

Note: Measured partly under different conditions! Lines to guide the eye (no modeling)!

Beware:
No MCz nor Cz material displayed

Beware:
Signal shown and not S/N!

More on the poster, e.g.:
- For fluences above ~ 10^{15} neq/cm² trapping becomes the dominant problem (depletion voltage remains important but less relevant)
- n-stripe readout (n-in-n or n-in-p) looks very promising at least for outer layer, probably even for inner with higher voltage
- At high fluences p-material does not anneal with respect to CCE (maintenance periods easier to control?)
- It seems, that in MCz material charged particles introduces more donor and neutral more particle acceptor levels \( \rightarrow \) compensation
- 3D detectors are promising candidates for the very inner layers (enormous progress by several groups)
- Systematic studies of RD50 and WODEAN improves or understanding of microscopic defects to macroscopic device behaviour

References:
[3] n-SiC, 5μm, (2μs), pad (Moncetelli 2006)
[5] 3D, double sided, 250μm columns, 300μm substrate (Pennicard 2007)
[8] n-EPI, 5μm, (-30°C, 25ns), pad (M unoz 2007)
[9] Note: Fluences normalized with damage factor for Silicon (0.62)
CHARACTERIZATION OF IRRADIATED P-TYPE SILICON DETECTORS BY THE ALIBAVA SYSTEM

Mercedes Miñano (Instituto de Física Corpuscular (IFIC))

Liverpool
Barcelona
Valencia
Irradiated test sensors have been characterized in terms of their charge collection efficiency. A new acquisition system

- **The sensors:** High resistivity N-or Area 1 cm²
- **The ALIBAVA acquisition system:** a Beetle based system to read out signals produced in strip silicon detectors by illuminating them with radiation sources.

The sensors have been irradiated with neutron and proton irradiation at expected doses of the upgraded Large Hadron Collider (LHC) luminosity peak: \(10^{35} \text{ cm}^{-2} \text{ s}^{-1}\)

- **n-in-p is a viable option for SLHC**
SIMULATION OF ELECTRICAL PARAMETERS OF NEW DESIGN OF SLHC SILICON SENSORS FOR LARGE RADII

Otilia Militaru (Université Catholique de Louvain)
As a result of the high luminosity at SLHC, the CMS tracking system with high granularity will be needed and the sensors will have to withstand an extreme radiation environment.

Otilia Militaru

On this basis, a new geometry with silicon short strip sensors (stripels) is proposed. In order to understand the behaviour of such devices, test geometries are developed whose performance can be verified and optimized using simulation of semiconductor structures. used the TCAD-ISE (SYNOPSYS package) software in order to simulate the main electrical parameters of different strip geometries, for p-in-n type wafers.
To the readout electronics noise, crucial contribution is given by the backplane capacitance of the bulk and the capacitance between adjacent electrodes (strips). These factors have been studied in order to evaluate the effect of cross talk between nearby Near-Far strips.

For the avalanche breakdown process, the structure demonstrates a good resistivity, the metal routing lower the electric field at the Near Strips junction. From simulations, can be seen the clear variation of the different components of the interstrip capacitance between neighbour strips. The influence of the opposite strip to this parameter starts to be significant when the Far Strip junction is at the same level or closer to Near Strips.
Silicon detectors with Low Interactions with Material

by INFN group 5 & eight Italian Universities

Lorenzo Vitale (Università di Trieste / INFN)

SLIM5 BEAM TEST RESULTS FOR THIN STRIPLET DETECTOR AND FAST READOUT BEAM TELESCOPE

Irina Rashevskaya (INFN – Trieste)

INVESTIGATION OF AN ABNORMAL PATTERN OF THE STRIP LEAKAGE CURRENTS IN MICROSTRIP DETECTORS
A successful beam test is described in detail

**Detector options**

The collaboration identified two detector options to reach this goal:

- A new and challenging triple well CMOS Monolithic Active Pixel Sensor (MAPS) with in-pixel signal processing and sparsified capabilities.
  - Pixel cell is 50x50 µm².
  - Active area close to 90% and 100-200 µm thick.
  - For more details, talk by M. Villa.

- A more traditional, but thin high resistivity double-sided silicon detector with short strips "striplets".
  - Strips are tilted by 45°, 50 µm pitch, active area 27 x 12.9 mm² and 200 µm thick.
  - Strip cap. ~4 pF

For more details, see Poster by I. Rashevskaya

Designed and fabricated by FBK-IRST.

On some of the sensors a "strange" current pattern was observed.

The panettone effect

(2nd poster)

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**Applications**

Such detectors can be used for the layer 0 in a future high-luminosity collider, such as the Super B-factory or the International Linear Collider.
Investigation of an abnormal pattern of leakage currents in silicon microstrip detectors

Some batches of microstrip detectors fabricated by FBK-irst showed an odd and peculiar pattern of the strip leakage currents: the current of the first and the last few strips is low, whereas all the strips in between have very high current (3-5 orders of magnitude higher). This peculiar phenomenon, common to ALL six different detectors in EACH wafer of the batch, has been called “Panettone effect”.

I. Rashevskaya on behalf of the Slim5 Collaboration, Trieste Group
Role of surface generation current

Surface generation played a major role. The high current measured on strip detectors is quantitatively compatible with this surface-generated current in the interstrip gaps. It must be concluded that in the gaps between the strips of the detectors the interface has much worse characteristics than in the gated diodes.

Proposed explanation for the origin of the effect

By comparing the technologies of different detector lots fabricated by FBK-irst, we observe that the peculiar 'Panettone Effect' is correlated with the combined presence of two LPCVD-deposited dielectric layers: silicon nitride and TEOS oxide. This combination produces a high level of stress, which induces defects at the silicon/oxide interface, leading to a high rate of surface generation. These dielectric layers are interrupted in the contact areas between metal and (implanted) silicon. This locally releases the stress in a region around the contact. Since the Bias Rings of the detectors have a continuous contact opening along their length, the local release of the stress can explain the fact that the strips within a certain distance from the Rings have low leakage current. Making use of a modified technology excluding the TEOS oxide, a batch of striplet detectors has been fabricated. They showed no “panettone effect”, and have been successfully employed in the SLIM5 beam test at CERN in September 2008.

I. Rashevskaya on behalf of the Slim5 Collaboration, Trieste Group
BJT detectors are able to measure different types of ionizing radiation: \(\alpha\)-particles, \(\beta\)-particles, X- and \(\gamma\)-photons.

Low cost and simple setups (battery) e.g. alpha detectors (Radon monitoring)
High current gain ~ 600
Not so fast 50-100\(\mu\)s
The detector is a Bipolar Junction Transistor whose Collector is the fully depleted high resistivity substrate, while the Emitter and Base implants occupy a few microns under the surface. The reverse biased Base-Collector junction collects the signal charge: as soon as the holes accumulate into the base, due to the BJT effect, an amplified charge is injected from the Emitter to the Collector, generating a few µs wide current pulse. Flowing through the feedback resistor of the OPA, this current pulse is converted into a voltage signal. An Equivalent Noise Charge of 340 e⁻ has been obtained with the simple - and inexpensive - set-up depicted above [5].
Daniele Passeri (Università di Perugia)

CHARACTERIZATION OF CMOS ACTIVE PIXEL SENSORS FOR PARTICLE DETECTION: BEAM TEST OF THE FOUR SENSORS RAPS03 STACKED SYSTEM

Introduction

Following the mainstream of microelectronics CMOS bulk technology, a third generation of monolithic Active Pixel Sensors for particle detection purposes (called RAPS03) has been fabricated in 0.18µm CMOS IP6M technology and tested. Beside electrical characterization and particle detection principle validation, an extensive detector functional test has been carried out. Actually, single chips have been already characterized in terms of response to X-ray photons and β particles.

In this work, in order to check their suitability for vertexing/tracking applications, four stacked CMOS APS sensors featuring 256x256 pixels with 10µm×10µm pixel size have been tested at the INFN Beam Test Facility (BFT), Frascati (Rome), Italy. To this purpose, a dedicated mechanical and electrical set-up has been devised and implemented, allowing for the simultaneous read-out of four sensors arranged in a stacked structure. This work has been carried out within the framework of the SHARPS experiment, supported by INFN.

Experimental Results

The characterization has been carried out using the Beam Test Facilities at the INFN LNF, Frascati (Rome), Italy. An electron beam featuring energies up to 500MeV has been used. A typical response of the four sensors is illustrated in Fig. 5. The tracker system exploits a self-trigger, using layer II and layer IV as telescope.

Signal to Noise and Spatial Resolution

The signal distributions within the cluster are represented in Fig. 10. The Landau signal distributions for a 5x5 pixels cluster are reported in Figs. 11 in terms of ADC counts (1 ADC = 0.6mV). The single pixel noise is 1.67ADC (small n-well) and 1.05ADC (large n-well).

From the generalized n-function distribution [1], the deviation from the "ideal" case of charge division among adjacent pixels can be estimated (assuming that n-functions along x-axis and y-axis are uncorrelated), thus estimating a theoretical spatial resolution limit for particle trajectory of about 0.37µm (Fig. 12).

Third generation of monolithic active pixels MAPS (0.18µm CMOS) in a test beam 4 quadrants with different layouts!

Ask Daniele about plans of radiation hardness studies?
STUDY OF GEIGER AVALANCHE PHOTO DIODES (GAPD) APPLICATIONS TO PIXEL TRACKING DETECTORS

Main Goal
The use of std CMOS tech. APD's in Geiger mode (that is reverse-biased above breakdown) as sensors with integrated logic, for direct particle detection in pixel tracking detectors

Exploit PROS and improve on CONS

The study includes simulation and prototyping (to detailed to explain here)

Pros:
• Ionization production of Avalanche starting carrier → Part. Detect.
• Std CMOS tech mature and supported for custom design
  • Integrated and Active Quenching (& active circuits) to minimize avalanche charge, cross-talk and after-pulsing
  • Gate mode (bunch crossing)
• Monolithic integration → System on chip
• Moderate (low) cost
  • Very Low material budget: Depletion region ~1 μm ~80 e/h pairs!
• Very high SNR (but only binary detectors)

Cons:
• Fill factor limited to wells width
• Dark count rate (High Geiger eff. even at low excess bias V)
• Cross-talk (to handle lowering the excess bias V)
• After-pulsing (trapped carriers & delayed release; worse w/ cooling)

Proto’s in HV CMOS:
• APD’s w/ output buffer: To minimize output load (parasitic) capacitance which impacts performance: time response, after-pulsing, dark count, x-talk
• Double APD and APD array:
  • Fill factor ↑: pixel separation minimal (Min. DNTUB distance 0(10 μm)).
  • Different pixels in the same DNTUB (common cathode).
  • Minimal separation is min. ptub distance (1.7 μm).
  • Problem sharing DNTUB: Electrons diffusing in the deep ntub could reach any pixel: electrical “crosstalk”...

Collateral (std) Application: Single photon detection for (astro-)particle physics, medical devices, etc...
STUDIES SUPPORTING FUTURE DETECTOR OPERATION
OPTIMISING THE STRIP GEOMETRY FOR VERY FINE PITCH
Ingredients:

- 50 micron pitch silicon strip sensor with a varying number of intermediate strips and different strip widths

- Testbeam at CERNs SPS: 120 GeV/c pions

Outcome:

- Resolution study suggesting the best strip geometry for 50 micron pitch strip sensors

- First tentative study of dependence of the cluster width on the incident angle for a future $p_t$ trigger in the tracker

We are waiting for further results from „cluster width on the incident angle “!!!

Marko Dragicevic, HEPHY Vienna
Filippo Bosi (INFN Pisa)

DEVELOPMENT AND EXPERIMENTAL CHARACTERIZATION OF PROTOTYPES FOR LOW MATERIAL BUDGET SUPPORT STRUCTURE AND COOLING OF SILICON PIXEL DETECTORS, BASED ON MICROCHANNEL TECHNOLOGY
Development and Experimental Characterization of Prototypes for Low Material Budget Support Structure and Cooling of Silicon Pixel Detectors, Based on Microchannel Technology

Pixel detectors at future colliders will need to match very stringent requirements on position resolution. The support structure and cooling add important contributions to the total material in the active area.

Advantages of the MICROCHANNELS: due to the high surface/volume ratio, heat exchange trough forced convection of liquid coolant is taking place efficiently, obtaining high thermal conductivities without affecting the stiffness of the structure; the contiguity between the fluid and the circuit dissipating power reduces thermal resistances; uniform temperature on the surface covered by the sensors can be obtained.

Several prototypes with different geometries of micro-machined channels have been realized in ceramics (AlN) and composite materials (CFRP). FEA studies have been validated by the experimental tests performed in the thermofluidodynamics test-bench we recently assembled at the INFN-Pisa laboratory.

**General Specifications for pixel support:**

- Need to evacuate electronics power (about 20 kW/m², sensor temperature below 50 °C)
- Pixel support (w/o cables and sensors) has to remain as low as possible (below 0.30% X₀)

In a thermal convective exchange the film coefficient is:

\[ h = \frac{N_u \cdot k}{D_h} \]

Nu = Nusselt number
K = Conductive heat transfer coefficient of the liquid
Dh = Hydraulic Diameter of the cooling channel

In order to maximize the h value it is important to minimize the hydraulic diameter. This remark points us to the Microchannel technology.
Prototypes Characterization

**Single Channel AlN additive method:**
Thickness = 0.65% $X_0$

- Thickness: 910 μm
- Length: 12.8 mm

**Triple channel CFRP subtractive method:**
Thickness = 0.40% $X_0$

- Thickness: 1100 μm
- Length: 12.8 mm

**Microchannel CFRP additive method:**
Thickness = 0.28% $X_0$

- Thickness: 700 μm
- Length: 12.8 mm

**Microchannel prototype matches the requirements of $X_0$ and dissipated power.**

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**Triple Channel FEA Simulation**

<table>
<thead>
<tr>
<th>AIN single channel measurement</th>
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</thead>
<tbody>
<tr>
<td>$T_{\text{FLUID}}$</td>
</tr>
<tr>
<td>Power Density $\delta_p$</td>
</tr>
<tr>
<td>Flow Rate</td>
</tr>
<tr>
<td>$T_{\text{IN AVERAGE}}$</td>
</tr>
<tr>
<td>$T_{\text{OUT AVERAGE}}$</td>
</tr>
<tr>
<td>$P_{\text{IN}}$</td>
</tr>
</tbody>
</table>

**CFRP triple channel measurement**

| $T_{\text{FLUID}}$ | 9.5 °C |
| $\delta_p$ | 2 W/cm$^2$ |
| Flow Rate/ch | 0.24 kg/min |
| $T_{\text{IN AVERAGE}}$ | 41.1 °C |
| $T_{\text{OUT AVERAGE}}$ | 43 °C |
| $P_{\text{IN}}$ | 2.6 bar |

**CFRP Microchannel measurement**

| $T_{\text{FLUID}}$ | 9.5 °C |
| $\delta_p$ | 2 W/cm$^2$ |
| Total Flow Rate | 0.26 Kg/min |
| $T_{\text{IN AVERAGE}}$ | 45.1 °C |
| $T_{\text{OUT AVERAGE}}$ | 47.2°C |
| $P_{\text{IN}}$ | 3.6 bar |

**Thermal conductivities:**
- CFRP support: $K_x = K_y = 75$ W/mK; $K_z = 3$ W/mK
- Aluminum Tape: $K = 180$ W/mK
- Glue: $K = 0.15$ W/mK
- Heater: $K = 0.15$ W/mK

**Boundary conditions:**
- Power density: 2 W/cm$^2$
- $h = 15000$ W/m$^2$K, turbulent flow
- (total flow rate = 0.7 kg/min, fluid $H_2O +$ Glicole 50%)
- $T_{\text{fluid}} = 9.5$ °C
- Results: $T_{\text{max}} = 38.9$ °C

F. Bosi, M. Massa, 11th Pisa Meeting on Advanced Detectors, 24-30 May 2009
LITHIUM DIFFUSION INTO SILICON-GERMANIUM SINGLE CRYSTAL

Basic wafer

$\text{Si}_x\text{Ge}_{1-x}$

Smaller bandgap than Si
Higher absorption coefficient (high Z)
Ge concentration $\sim$ absorption

Li content can change resistivity even change from p- to n-bulk
This is the very last talk

I WOULD LIKE TO THANK THE ORGANIZERS FOR A TOTALLY PERFECTLY ORGANIZED CONFERENCE

THANK YOU

THE END