The NA62 Gigatracker pixel detector system

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Abstract

The silicon tracker for the NA62 experiment has to provide both a time resolution of 150 ps rms and a space resolution of about 100 μm rms. These challenging specifications require the development of a new readout electronics in order to address the problem of measuring the tracks arrival time with such a high channel density. Moreover, the high particle density (up to 1.5 MHz/mm^2 in the center and 0.8 - 1 GHz in total) requires a high speed measurement and data transmission in order to keep the dead time below 1%.

Key words: hybrid pixel detector, silicon pixel ASIC, TDC

1. Introduction

The aim of the NA62 experiment is to study the ultra rare decay of the positively charged K meson into a pion and a neutrino-antineutrino pair at the CERN SPS [1]. The beam spectrometer has to sustain high and non-uniform beam rates (up to 1.5 MHz/mm^2 in the hot center and 0.8-1 GHz in total, hence the name GigaTracker) and should preserve beam divergence and limit beam hadronic interactions. The Gigatracker has to provide precise momentum, time and angular measurements on every single track of the secondary 75 GeV/c hadron beam with a timing precision of 150 ps (rms).
To meet these requirements, three silicon pixel detector stations will be installed. The required time resolution is 200 ps per station.

2. The NA62 GigaTracker

Hybrid silicon pixels have been chosen as detector technology [2]. Silicon pixels can provide an adequate time and space resolution as well as a sufficient radiation tolerance.

A detector thickness of 200 μm has been adopted as a compromise between the need for a short charge collection time and the material budget, which must not exceed 0.5% of the radiation length per station. The pixel readout ASIC will be thinned to 100 μm.
The pixel detector will operate below $5°C$ in order to improve the radiation tolerance. An asymmetric beam profile (60×27 mm^2) has been chosen to be able to cover the geometrical beam acceptance with no dead areas. The beam area is covered by a 2×5 matrix of readout ASICs bump bonded to a single detector. Each readout chip has a sensitive area of 12×13.5 mm^2, divided into a matrix of 45×40 pixels. The pixel size is 300×300 μm^2.In order to reduce the material budget the three stations will be placed in the vacuum of the beam pipe, posing a challenge to integration, cooling and electrical signals connections.

3. ASIC prototypes

The design of the electronic readout ASIC is very challenging, owing to the requirements of both high channel density and high time resolution. In order to address these challenges two prototypes, based on two different concepts, have been designed in a CMOS 0.13 μm technology [3].
In the first option a constant fraction discriminator technique is used to compensate for the comparator time walk. The discriminator signal is then used to store the value of a time stamp bus, which is distributed to all the pixels. A coarse measurement is thus obtained. In parallel, a Time to Amplitude Converter followed by a Wilkinson ADC is used to measure the distance between the comparator output and the next clock rising edge. All these operations are performed inside the pixel cell. In this option all pixels act independently and all the time-critical signal (except the clock) are confined in the pixel area.
In the second option the time walk is corrected using the time over threshold technique. Each pixel cell drives a dedicated transmission line to send the digitized discriminator signal to the end of column. The driver signal is time critical and therefore special techniques have been adopted in order to maintain its time precision. Each pixel output line is realized as a transmission line and is driven in current mode. Pre-emphasis is implemented in the line driver in order to circumvent the problem of the line resistance. The signal from the pixels is measured using DLL based TDCs. When a hit arrives hit registers capture the state of the DLL and the state of the base frequency clock counter.

References

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