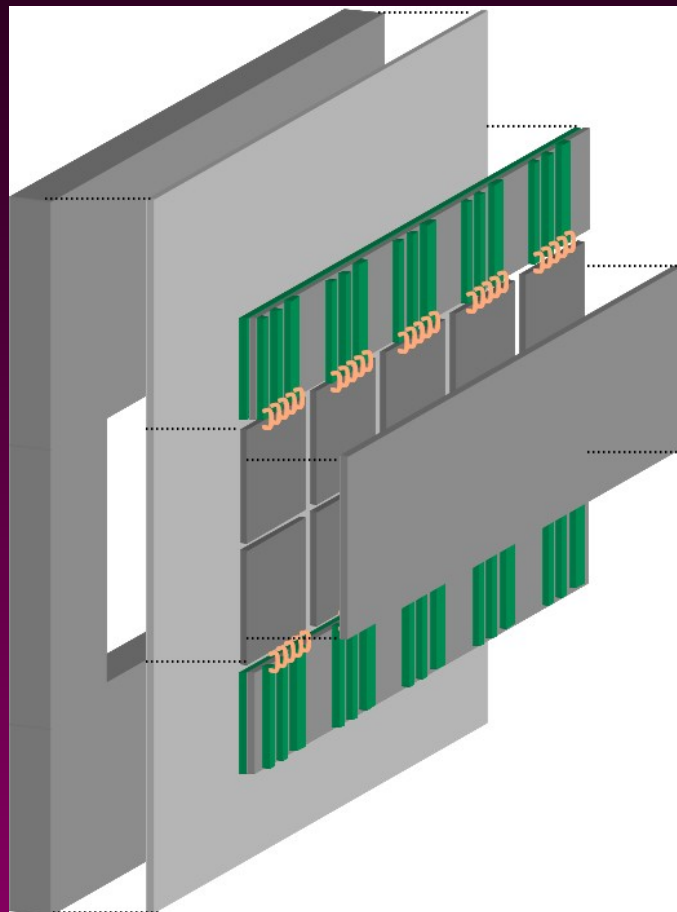




# NA62 GigaTracker



GigaTracker : 3 silicon pixel sensor stations for precise measurement of particle direction and timing.

Pixel size :  $300 \mu\text{m} \times 300 \mu\text{m}$

Sensitive area :  $27 \text{ mm} \times 60 \text{ mm}$

Time resolution : 150 ps rms (total)

200 ps rms (per station)

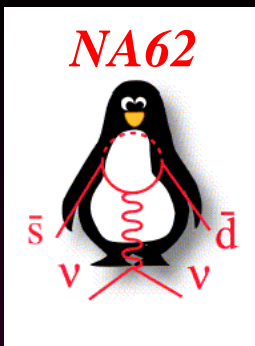
Data rate :  $0.8 \div 1 \text{ GHz}$  (total)

$1.5 \text{ MHz/mm}^2$  (max)

Operational environment : vacuum

Detector to be operated below  $5 \text{ }^\circ\text{C}$  to keep the leakage current under control

Design challenge : obtain a 200 ps resolution with silicon pixel detectors at very high particle rate.



# ASIC prototypes



Two readout options are under investigation :

Pixel matrix :  $40 \times 45$  cells.  
Time walk compensation : Constant Fraction Discriminator (CFD).  
Time measurement : on pixel TAC based TDC.  
Reference clock : 160 MHz.  
Four event buffers for data derandomization (on pixel).  
SEU protected control logic.

- + each pixel operate independently.
- + only one long distance time critical signal (clock).
- complex pixel circuitry.
- more control logic on the beam trajectory.

Pixel matrix :  $40 \times 45$  cells.  
Time walk compensation : Time over Threshold (ToT) correction.  
Time measurement : DLL based TDC at the end of the pixel column.  
Reference clock : 320 MHz.  
Pre-emphasis for signal transmission.

- + simple and low power pixel circuitry.
- + only one DLL based TDC needed ( plus column registers ).
- many time critical signals to be sent to the EoC (one per pixel).
- hit arbitration needed (possible event loss).

→ Prototypes of the analog part for the two options ( preamp+CFD and ToT correction ) have been designed in CMOS  $0.13 \mu\text{m}$  and successfully tested.

→ Two test chip with the full pixel and column circuits are currently in production