The digital read-out for the CSC system of the TOTEM experiment at LHC

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Abstract

At LHC at CERN, the TOTEM detector that will measure the inelastic rate in the pseudo-rapidity region $3.1 \leq |\eta| \leq 4.7$, named T1, is made of Cathode Strip Chambers. Signals from about 11000 anodes and 16000 cathodes must be processed and optically transmitted to the counting room. The complete electronic readout chain of the Cathode Strip Chambers is presented here. The electronics system has been developed keeping into account the hostile environment from the point of views of both radiation and magnetic field. Dedicated VLSI circuits have been extensively used in order to optimize space and power consumption.

Key words: Cathode Strip Chambers, Electronic readout, Gigabit optical link

1. The T1 detector

The T1 telescope is installed in two cone-shaped regions in the end-caps of CMS, delimeted by the beam pipe and the inner envelope of the flux return yoke of the magnet. Each telescope arm consists of five planes of CSC equally spaced in z at a distance between 7.5m and 10.5m from the interaction point. Each detector plane is composed of six trapezoidal CSC covering roughly a region of 60° in ϕ. References of TOTEM experiment can be found in [1]

2. Electronics system architecture

The electric signals generated by the ionizing particles going through the detector generate charge signals of both polarities. The CSC anode negative signals and cathode positive signals are collected by custom designed anode front-end cards (AFEC) and cathode front-end cards (CFEC), equipped with a custom front-end ASIC named VFAT, designed to perform the charge readout of the three TOTEM detectors. A basic block diagram [2] of the functional components of the system is shown in figure 1

We may define three logically and physically separated regions. VFAT front-end ASICs are located as close as physically possible to the detector (the On Detector Regions). Custom read-out boards are placed in the neighborhood of the detector (the Local Detector Region): they distribute control signals to the VFAT, collect and concentrate data from the front-end ASICs, transmit the data to read-out boards in the counting room (the Counting Room Region).

2.1. Front-End cards

The AFEC is the board that collects and groups signals from the anode wires of the CSC detector. Ten different types of

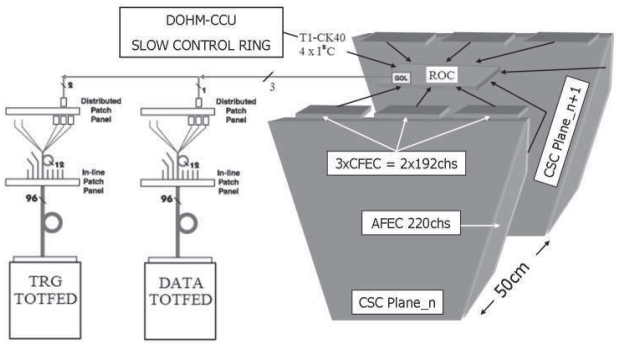

Figure 1: T1 electronics system block diagram

AFECs have been adapted to the chamber shapes, for a total of 60 boards for the whole detector. The boards are soldered directly on the edges of the chambers: their length varies between 60 cm and 100 cm. The figure 2 shows one type of AFEC.

For every channel a double-stage high-pass filter isolates the high voltage on the wire from the readout, breaking the DC ground loop and adapting impedance, capacitance and signal shape. The readout of up to 256 wires per chamber is carried out by two VFATs mounted on a VFAT hybrid each. Trigger information is generated on the VFAT by grouping signals from up to 16 contiguous anode wires.

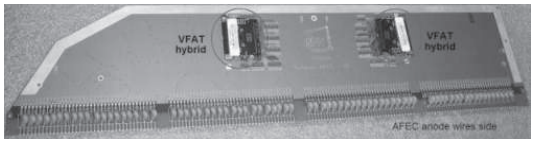

Figure 2: AFEC type 2P, adapted to the small CSC chamber installed in the 2nd layer

The CFEC is the board that collects and groups the charge pulses induced in the CSC strips by the positive ions created

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by the crossing particle and moving towards the cathode. Each board processes 128 input signals. The CFEC hosts for every channel a high-pass filter and delivers the outputs to a VFAT hybrid. Due to the different sizes of the CSC detectors, for each layer of the telescope a different number of CFEC boards is needed.

2.1.1. VFAT and VFAT hybrid

The VFAT [3] produces both Trigger and Hits information. The Trigger information, in the form of a programmable fast OR, can be used for trigger building. The Hits information is in the form of binary channel data corresponding to a given clock period selected by a first level trigger. The VFAT has 128 channel inputs. Each channel contains a low noise pre-amplifier and shaper followed by a comparator and digital circuitry. On receipt of a trigger the corresponding binary data is packaged together with time stamps and other information (i.e. ChipID, CRC) into a 192-bit data packet. The figure 3 shows the top view of the VFAT chip and its hybrid.

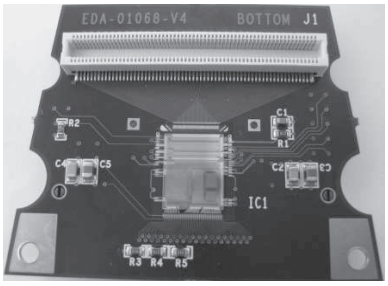

Figure 3: Top view of the VFAT hybrid

2.2. Read-Out Card

The ROC board interfaces the AFEC and CFEC cards to the DAQ system, located in the counting room. As depicted in figure 1, the ROC represents the data, trigger, slow control and low voltage junction point of two CSC detectors. The board receives the digital serial data stream from 16 VFAT hybrids hosted on the AFEC and CFEC cards, for a total of 2048 CSC signals. The serial tracking data stream received from the front-end hybrid is converted from LVDS to CMOS levels and optically transmitted, through the CMS Gigabit Optical Hybrid (GOH) mezzanine, to the TOTFED board in the counting room.

The GOH groups the 16 data inputs in two 8-bit words treated in parallel and transmitted over a fiber through a 0.8 Gbit/s Ethernet 8B/10B parallel-to-serial encoder. The trigger information can also be merged with the readout data stream using a spare Gigabit Optical Link data channel and a special VFAT Trigger Mezzanine (VTM) hybrid.

The VTM mezzanine decodes also the fast command signal and extracts the Bunch Crossing Zero (BC0) impulse that synchronize the optical trigger bit transmitters located inside the CMS cavern and the receiver modules in the Counting Room.

The figure 4 shows the ROC loaded with VTM and CCUM mezzanines.

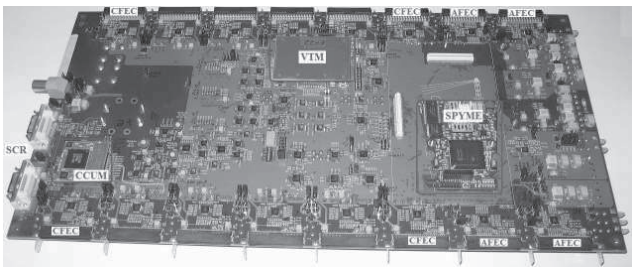

Figure 4: Top view of the ROC board

The configuration and monitoring of the system is performed using the I^2C standard protocol distributed through the optical CMS Slow Control Ring (SCR).

2.2.1. Slow Control Ring

The Slow Control Ring, adopted for all three TOTEM detectors, is based on the CMS tracker token ring system. The ROC manages the Trigger Timing and Control (TTC) signals by means of the DOHM module and communicates with the on-detector chips through the addressable CCUM mezzanine card plugged on it. The SCR can manage up to 127 CCUM nodes and also implement skip fault architecture (see figure 5) for additional redundancy based on the doubling of signal paths and bypassing of interconnection lines between CCUM.

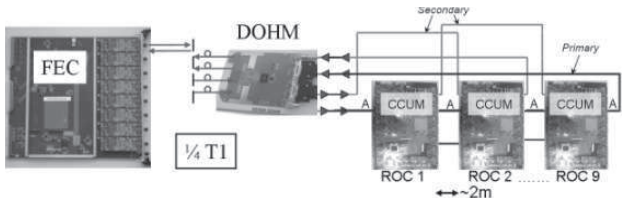

Figure 5: Slow Control Ring architecture

3. Conclusions

The TOTEM T1 detector electronics system is fully integrated within the TOTEM DAQ and also fully compatible with CMS DAQ requirements. Prototypes have proven to comply with the required functionalities and performances. The complete set of boards necessary to equipe the T1 detector have been built, tested and are ready to be mounted on the detector.

References

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