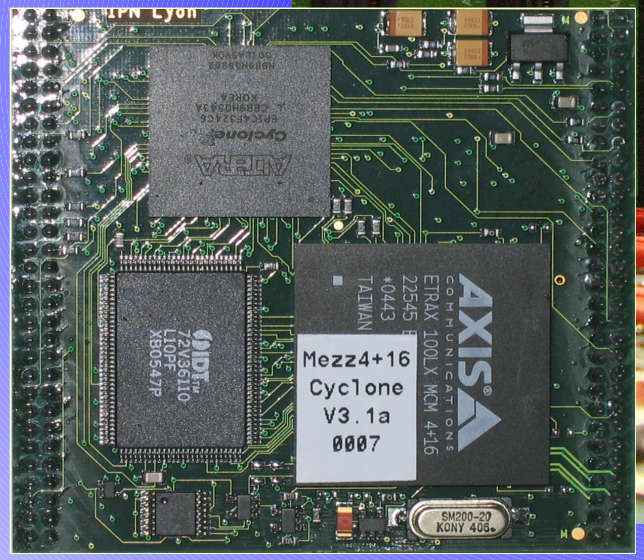
Ethernet-based DAQ systems for large neutrino experiments :



OPERA and beyond...

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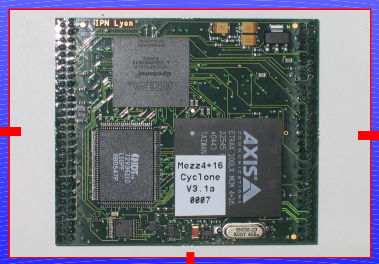
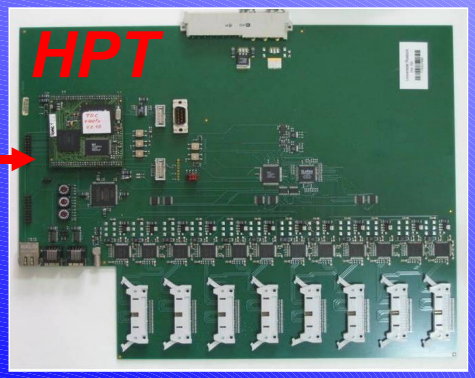
DAQ general features

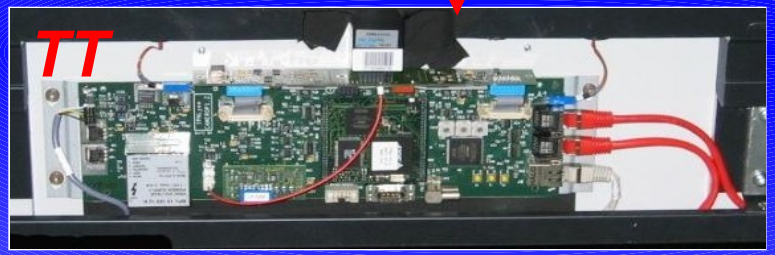
➢ The distributed DAQ is based on Ethernet. Each sensor (1200) is seen as a node in a Gigabit standard network. The basic "element" of the system is a daughter board ("mezzanine") embedding FPGA, FIFO, μ–processor (AXIS)





R/O: RPC tracker

R/O: drift tubes

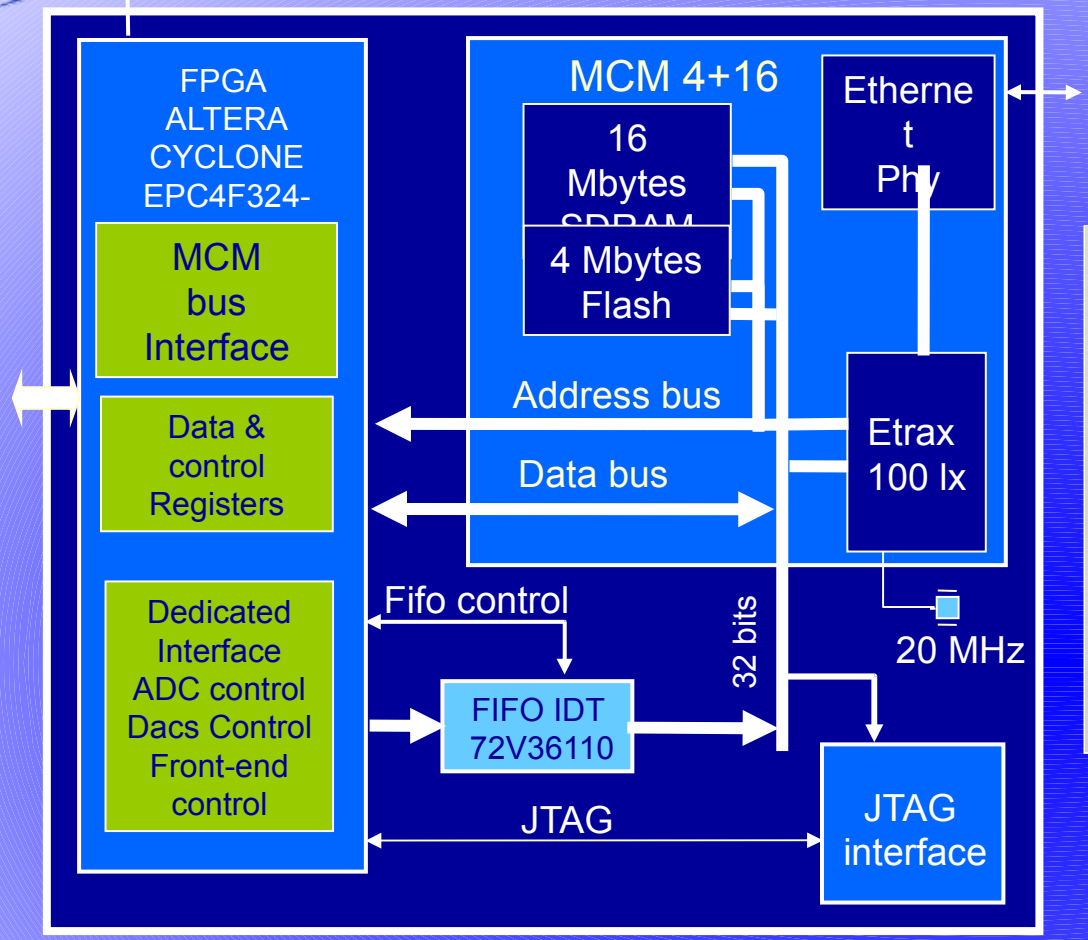


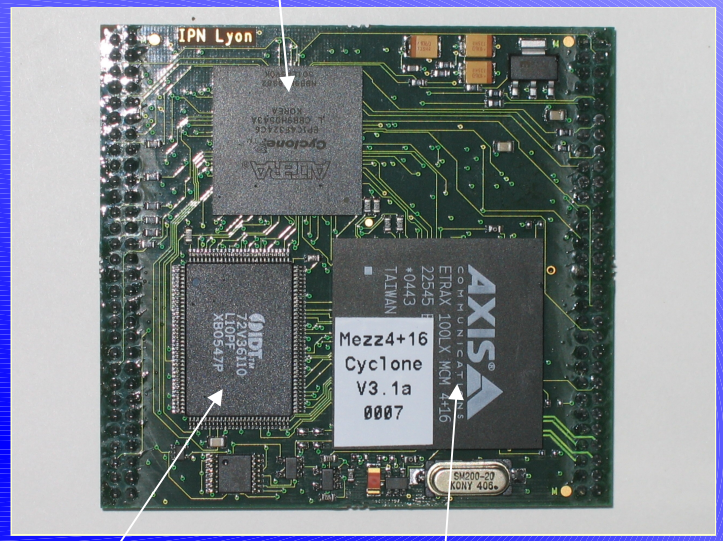
R/O: scintillator + WLS fibres + MaPMT

➢ The client/server protocol used relies on the CORBA standard implemented in C++ with interfaces into postgreSQL and Oracle database.

This software is completely object oriented and uses the Interface Description Language (IDL) to describe the distributed objects independantly of the programming language. InterORB protocols guarantee interoperability.

Embedded processor mezzanine





2*60 pins
mezzanine

FPGA (Cyclone)

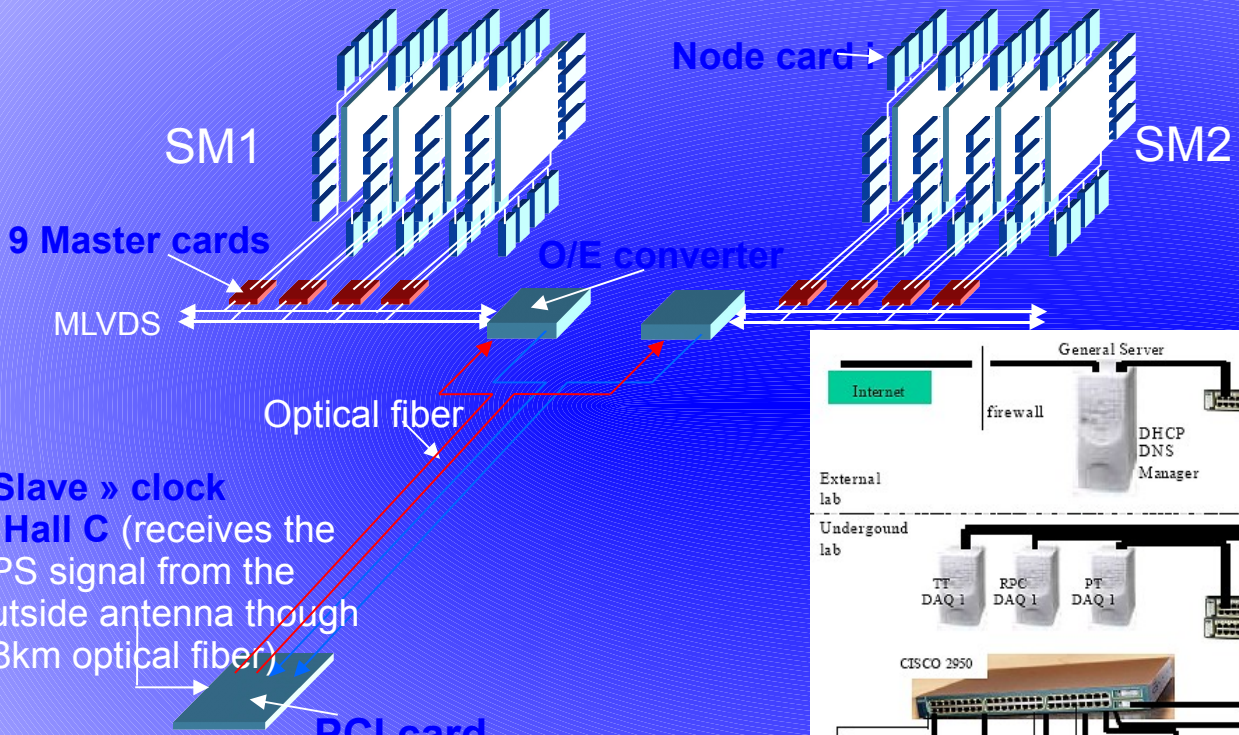
FIFO

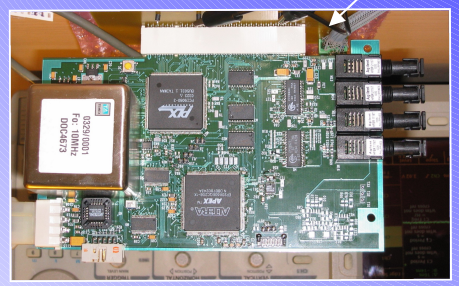
Multi Chip Module

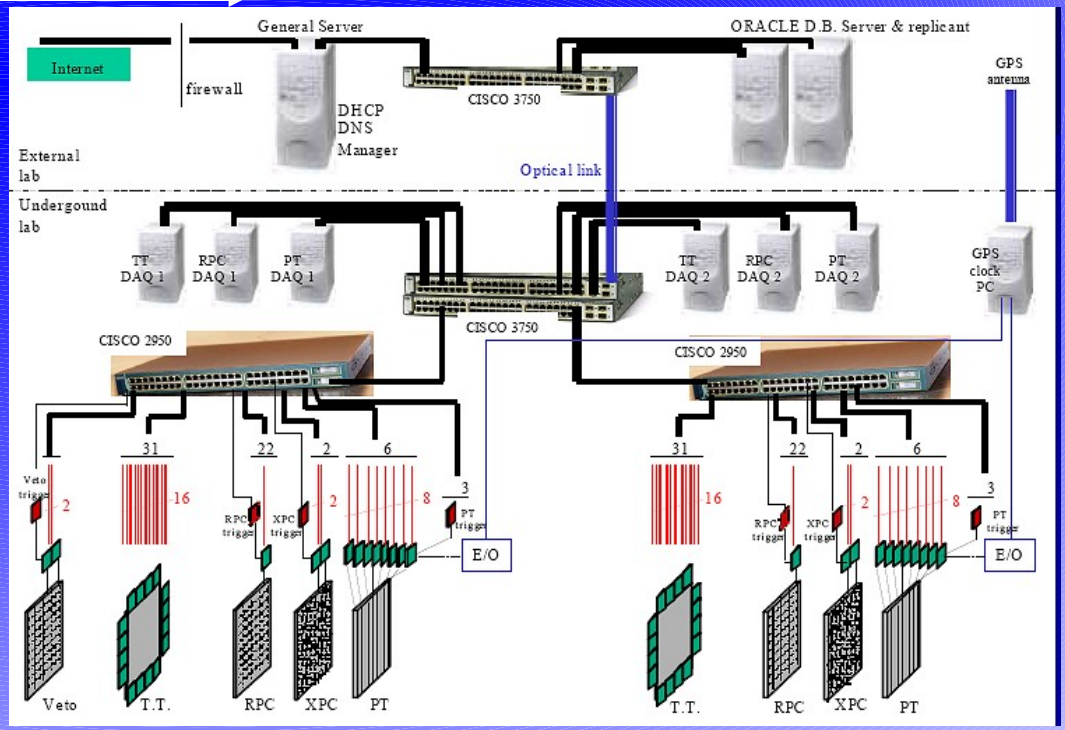
- DAQ core : microprocessor mezzanine (AXIS Etrax100lx :32 bits RISC)
- Embedded linux operating system. All distributed applications based on CORBA
- FPGA includes dedicated front-end interface for OPERA sub-systems : PMT, RPC, drift tubes
- Parallel network of synchronization clock locked on the GPS for off-line coincidence with CERN

Clock distribution & network architecture

➢ Each individual node runs a local 100MHz clock generated via a common 20MHz clock send from a precise and stable oscillator. The oscillator is plugged onto a dedicated PCI board which locks the clock signal on the GPS and encode specific commands (propagation delay meas., reset, reboot etc).

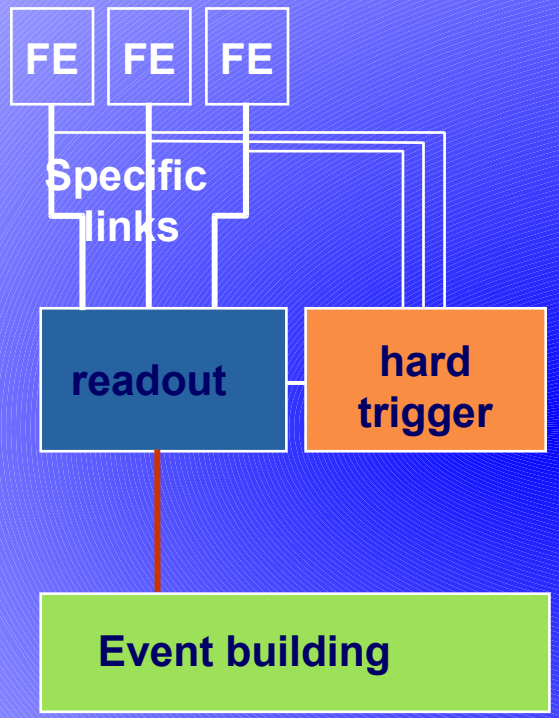




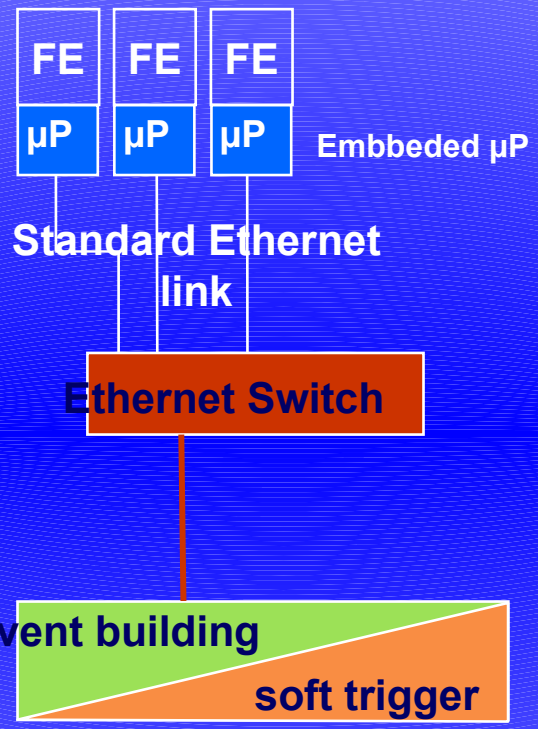


Beyond OPERA : R&D in Network based DAQ

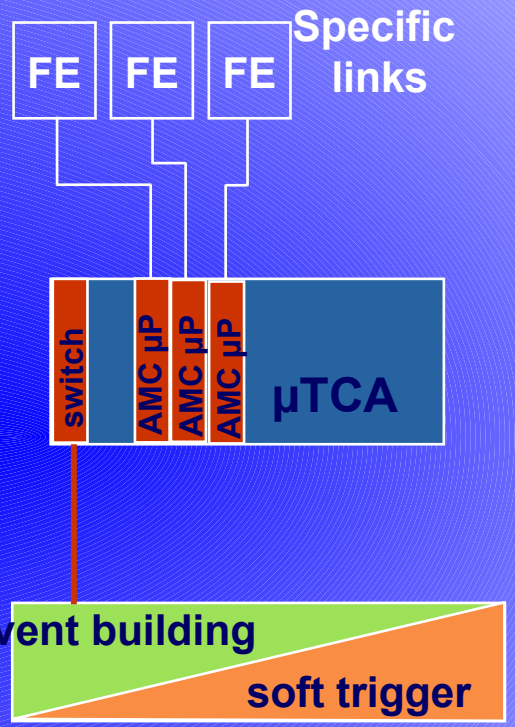
Classical architecture
(high data rate constraints)



Full distributed and network architecture
(Type OPERA 1200 sensors)



Full distributed architecture (compact detector Type TPC)

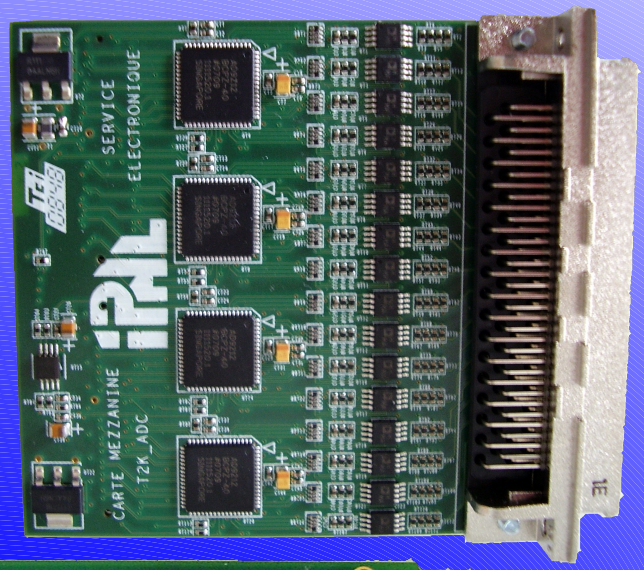


- Reduce µprocessors market dependency : softcore processors (NIOS II)
- Optimize CPU use : Network offload engine
- Gigabit Ethernet : ATCA standard
- New synchronization scheme : Synchronous PTP (IEEE 1588)

→ towards smart synchronous Ethernet networks

ARIA-GX AMC prototype

ADC
Mezzanine
With four AD9212
and 32 LVDS outputs



Under test …

ARIA-GX
EP1AGX60

DC/DC
Converter

MMC
VT026
Vadatech