The integration of the ALICE trigger system with sub-detectors

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Abstract

The ALICE Trigger electronics (TRG) has been installed in the experimental cavern and tested with each of the detectors, both individually ('standalone' mode) and in 'global' runs, i.e those involving other detectors. Global runs were performed with cosmic ray triggers, and also during the LHC startup period in September 2008. In this paper the status of the trigger system will be reviewed, in particular describing recent extensions to the system.

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1. Introduction

The ALICE trigger system operates with nucleus–nucleus, proton–nucleus and proton–proton interactions, having rates between about 8 kHz and 300 kHz [1]. The main block of the ALICE trigger electronics is the Central Trigger Processor (CTP), which is shown in Figure 1. The CTP [2] is implemented using seven different types of 6U VME board, together making up eleven active boards for the CTP. This system will receive and align up to 60 trigger inputs in parallel from the trigger detectors. There are three different hardware trigger levels (L0, L1 and L2) with latencies from 1.2 μs to 100 μs. The system allows dynamic partitioning in order to make optimum use of detector readout. The system provides a flexible past-future protection. Outputs from the CTP go to the LTUs of each sub-detector. The LTU serves as an interface between the CTP and the sub-detector readout electronics. The LTU is also able to run in a stand-alone mode of operation, and the LTU fully emulates the CTP protocol, thus enabling sub-detectors to carry out development, test and calibration tasks independently of the CTP. The timing of the emulated trigger sequences is identical to the timing during the global run. The trigger electronics is based on ALTERA Cyclone FPGAs (Field Programmable Logic Arrays), which provide flexibility to modify the trigger system in the future. The system provides a range of monitoring and debugging options.

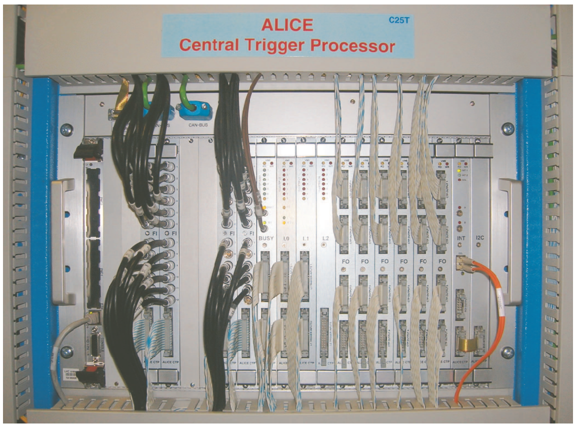

Figure 1: The ALICE Central Trigger Processor

The CTP is based on classes and clusters. The trigger class is a basic processing structure in the CTP logic. The CTP forms 50 independently programmable physics trigger classes [3, 4]. Information about trigger classes is used at each level of the trigger decision. The trigger class condition is realized as a logical AND formed from all the 24 trigger inputs at each level, two scaled-down bunch–crossing (BC) clocks and two random triggers. The two scaled-down BC inputs are 25 ns pulses, synchronous with the BC clock, with a programmable interval between the pulses in a range from

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0 to 25 s (a 30-bit counter). The two random trigger inputs are random patterns of 25ns-pulses, synchronous with the BC clock, which are generated by a 31-bit linear feedback register. Each class has an associated detector cluster, i.e. a designated group of detectors which must be read out when the trigger class is activated.

2. Trigger Input Switchboard

The Trigger Input Switchboard (TIS) has been designed in order to select 24 trigger inputs for CTP and LTUs. As ALICE now has more trigger inputs at L0 than the original design, so the TIS allows us to choose 24 from 50 trigger inputs. TIS is based on four Fanin/Fanout cards [5], originally designed for LVDS signal distribution and merging in ALICE, connected together via user defined pins on the VME backplane. The Fanin/Fanout card can be set as fan-in or fan-out by jumpers on the board. The first two Fan-in cards from the right side receive 50 trigger inputs. The third card is a Fan-out with a switch inside the Actel FPGA, which can chose 24 from 50 trigger inputs and send them to the CTP. The fourth card is the same switch, but it sends selected trigger inputs to the LTU boards and thus allows standalone runs for detectors with the selected trigger input. The TIS has a monitoring counter for each trigger input.

3. LTUvi electronics

The Local Trigger Unit (LTU)[6] has been updated to a 'LTUvi' version which incorporates the TTCvi [3] functions required for ALICE. The TTCvi board is not therefore required any longer. By implementing the TTCvi functionality in LTUvi, power is saved in each VME crate for LTUs, and interconnection and memory overflow protection problems eliminated on the TTCvi board. The LTUvi manages coding, serialization and sending of data for the A and B channel of the TTC system[7] plus the whole functionality of the LTU.

In global mode the LTU receives signals from the CTP and translates them to appropriate format (LVDS or formatted words to be sent through the TTC system). The LTU receives BUSY signals from detectors as LVDS signals and propagates them to the BUSY board, which is the part of the CTP where BUSY signals from all detectors inside a cluster are OR-ed together. It sends the L0 trigger to the sub-detector through an LVDS cable or through the TTC system and it sends L1 and L2 trigger messages through the the A and B channels of the TTC system.

4. CTP Upgrade

The CTP boards have been upgraded with new functionality allowing the status of trigger inputs to be read at the time of the L0 trigger. The trigger inputs data are transmitted to DAQ in the "CTP readout" data stream. The upgrade involves all seven CTP board types.

5. Operation of the CTP in 2008

During the commissioning period, many different configurations of the CTP were tried. The CTP was able to operate stably with up to 12 detectors, both in one or in several clusters. During the brief period of circulating beam in September 2008, timing measurements for trigger input detectors were successfully made.

6. Summary

The ALICE trigger system, including the trigger input switchboard, is installed in the experimental cavern where the full system is integrated with the other experiment service systems. The trigger input switchboard, the upgraded firmware for the CTP boards and the new Local Trigger Unit - LTUvi have been commissioned with all ALICE detectors. The Alice trigger system provided stable operation during first beam from LHC in September 2008.

References

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