The high rate data acquisition system for the SLIM5 beam test

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Vertex detector requirements for future experiments:

- excellent position resolution
- speed readout
- trigger feasibility
- high radiation tolerance
- high DAQ live time
- low material budget

CMOS Monolithic Active Pixel Sensors (MAPS) is one of the most promising candidate for such applications

SLIM5 Collaboration

The Slim5 collaboration focused its program in the development of a unique design approach for CMOS MAPS to improve the readout speed potential of these devices and at the same time to increase the sensitive element area.

In September 2008 the collaboration - consisting of six Italian institution - submitted a low material budget silicon demonstrator to test with protons at the PS-T9 test-beam at CERN.

The beam test setup was composed of two different detectors (DUTs) placed inside a reference telescope. The first was a 4k-Pixel Matrix of Deep N Well MAPS, developed in a 130 Nm CMOS Technology, providing digital sparsified readout. The other one was a high resistivity double sided silicon detector, with short strips at 45° angle to the detector's edge, read out by the FSSR2 chip.

Beam test setup

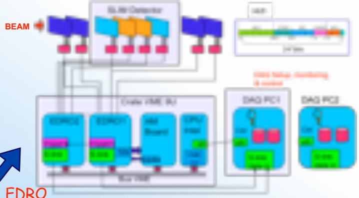
Beam conditions:

- 12 GeV/c momentum protons;
- 480 ms spill length;
- $10^4 - 10^6$ particles/spill;

Track reconstruction:

- 4 double-sided silicon strip detectors;
- 50 μm readout pitch;
- 2×2 cm^2 area;

The device under test (DUT) was placed on a motorized table with remote control inside the tracking volume, with two telescope detectors placed upstream and the other two downstream the DUT, respectively.



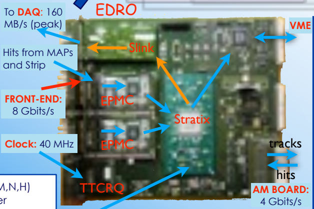
Data Acquisition

2 electronic board for Event Dispatch and Read-Out (EDRO)

- programmable and customized;
- used in Master and Slave configuration;

EDROs used to:

- configure the front-end chips of the DUTs (MAPs and Strip)
- configure the reference telescope
- collect data
- provide global trigger signal (30-35k tracks/spill)
- provide global system clock
- provide time-stamp identification



Electronic features

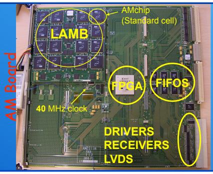
1 Master board + 5 mezzanine

Main mezzanine:

- PCB 16 layers
- FPGA Stratix II Altera 1508 pins (6 Mb RAM, 120 MHz)

Input mezzanine:

- PCB 8 layers
- FPGA Cyclone II Altera 484 pins (~500 kb RAM, 120 MHz)



Multiplicity trigger: (M,N,H)
M = # hits per layer
N = # hit layers
H = # of total hits

- (1,4,4), (1,6,6), (1,8,8)

AM trigger

- **Hit-match**: 4, 6 or 7 bits out of 9 match
- **Pattern-match**: match of all the 6 hits is required

DAQ performances

≥ 5 Trigger types:

- Scintillator
- Multiplicity
- Central Chip
- Random
- Associative Memory

DAQ rates:

- 3kHz (start)
- 40 kHz (running condition)

Read out channels: 12 000
Events: ≈ 90M
Live Time fraction ≈ 46%

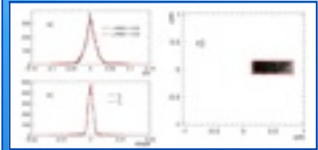
Associative Memory Board

- 4 LAMBs (Local Associative Memory Banks), 32 AMChip/LAMBs able to process 4 events simultaneously
- 20k different patterns of track (Roads) each pattern bank

Technical features

- Input data rate: 4 Gbit/s
- Clock: 40 MHz
- Latency < 780 ns → **provide first level trigger**

- The AM first level trigger functionalities were successfully tested.
- Residuals compatible with the Road pitch are obtained by comparing the offline track parameters and the Road parameters stored in the pattern bank.
- Preliminary results on trigger efficiency are satisfactory, though final results require more studies which are ongoing.



Comparison between offline track parameters and road parameters evaluated at the first microstrip layers. a)difference between coordinates (x, y); b)difference in track slopes(x slope, y slope); c) impact point of the tracks having a match with an AM track at the z coordinate of the MAPS chip.