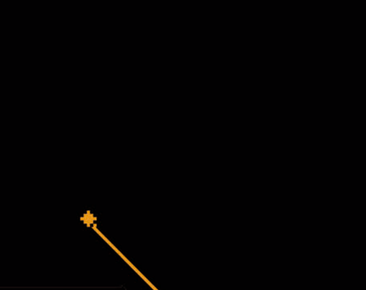
The FE Electronics of the LHCb Straw Tube Tracker

HV

The High Voltage board provides the interface between the Front End electronics and the anode wires of the Outer Tracker straw tube detector. On one side a HV board plugs into a Feed-Through board that is built into a detector module and on the other it connects to two ASDBLR preamplifier boards. The high voltage on the anode wires is decoupled from the small hit charges caused by passing particles by a 330pF capacitor, which is chosen as an optimum between minimizing signal loss and protection from sparks. Both the capacitors and the signal channels are embedded in the circuit board to reduce leakage currents and allow a high channel density of 5mm/ch.



ASDBLR

The ASDBLR (Amplifier-Shaper-Discriminator with BaseLine Restoration) receives the small signal induced by a passing particle from the HV board, amplifies it, discriminates it against a threshold and outputs a fixed binary signal to the OTIS time-to-digital converter in case the induced signal passes the threshold. The long ion tails of Argon gas following the rapid electron avalanche is an order of magnitude longer than the LHC bunch crossing cycle of 25ns. To reduce signal pile-up, the ASDBLR incorporates fast shaping and base line restoring of the signal, effectively reducing its dead time to less than 20ns. Noise and oscillations through feedback are reduced by a differential and low logic swing.

OTIS

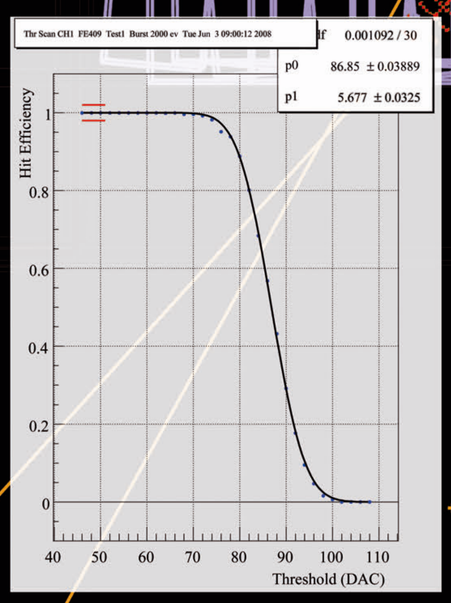
The OTIS time-to-digital converter measures the arrival time of an ASDBLR signal with respect to LHC clock, by digitizing the 25ns bunch crossing cycle into 64 steps of 390ps with the help of a Delay Locked Loop. The 6 bit fine time of 32 channels is written into a 160 stages deep pipeline buffer, covering the 4µs trigger latency. Upon a trigger, the corresponding hits are copied into a derandomiser buffer, where the fine time receives an additional two bits that indicate which bunch crossing the hit was registered in (1st,2nd,3rd,no-hit) and allows for an electron drift time of up to three bunch crossings. The design of the OTIS is such that the DLL state of half a clock cycle is processed in the next half, thereby eliminating dead time. A channel mask allows individual channels to be blocked from the data stream.

GOL

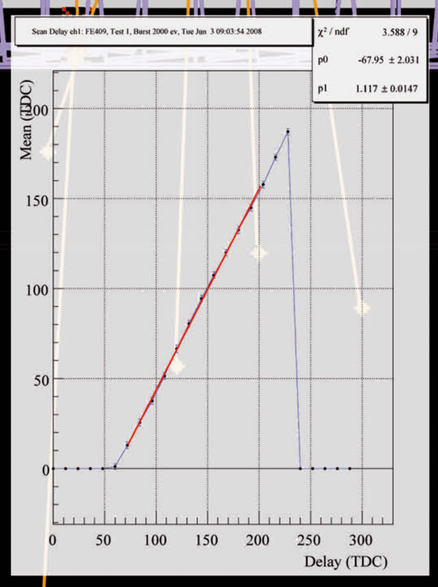
The GOL board (Gigabit Optical Link) takes the data of a triggered event from four OTIS time-to-digital converters and ships it off-detector via a single optical fiber, operating at 1.6Gb/s. As all electronics components in the Front End Electronics the GOL is created to be radiation hard, being able to cope with a radiation dose of 1MRad far exceeding the expected dose of 7kRad/10year.

quality assurance

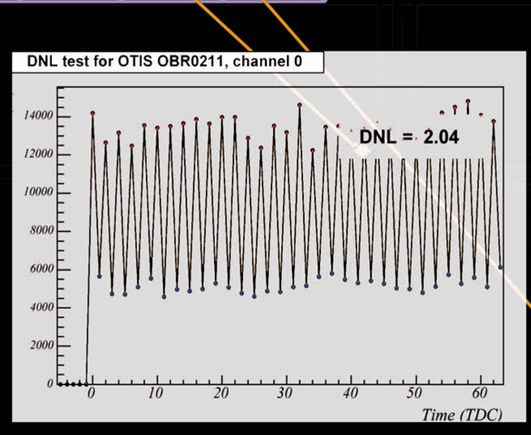
Each component in the Front End electronics has been individually tested by dedicated test setups. Besides these individual tests every Front End Box as an assembled whole has been subjected to tests of performance and quality assurance. Most significantly the Front End Boxes were tested against threshold behavior (Threshold Scan) and Time Linearity Behavior (Linearity Scan, Differential Non-Linearity).



The ASDBLR threshold should be chosen as low as possible to minimize the loss of detection efficiency, while being sufficiently high to reduce noise to an acceptable level. In the Threshold Scan the value of the threshold is increased in steps while fixed size charges are injected into the channels of a Front End Box. Per channel and for each threshold value is recorded the fraction of two thousand injections that pass the threshold and this fraction is plotted against the threshold value. Although the threshold can be set per eight channels, only ASDBLR were selected with high threshold uniformity.



The linearity of the OTIS time-to-digital converter is of the essence for usage with drift tubes. In the Time Linearity Scan the time phase (with respect to the LHC clock) at which charges are injected into the Front End Box is increased in steps. At each step the mean time at which two thousand injections are registered is recorded and this is plotted against the delayed injection time. Linearity is assured in all implemented OTIS.



The Differential Non-Linearity (DNL) quantifies the deviation from the nominal sizes of the time bins of the OTIS time-to-digital converter. In testing the Differential Non-Linearity (DNL), charges are injected into the channels of a Front End Box at uniformly random times and the amount of registered hits is per channel plotted against the time steps. For ideal bin sizes the resulting TDC spectrum is flat, while DNL shows up as a variation in the amount of registered hits. Design choices of the OTIS cause a small systematic difference between even and odd TDC bins as seen in the plot above. However, the final DNL value (+/- 0.5 bin size) is still better than our specifications.