Simulation of electrical parameters of new design of SLHC silicon sensors for large radii

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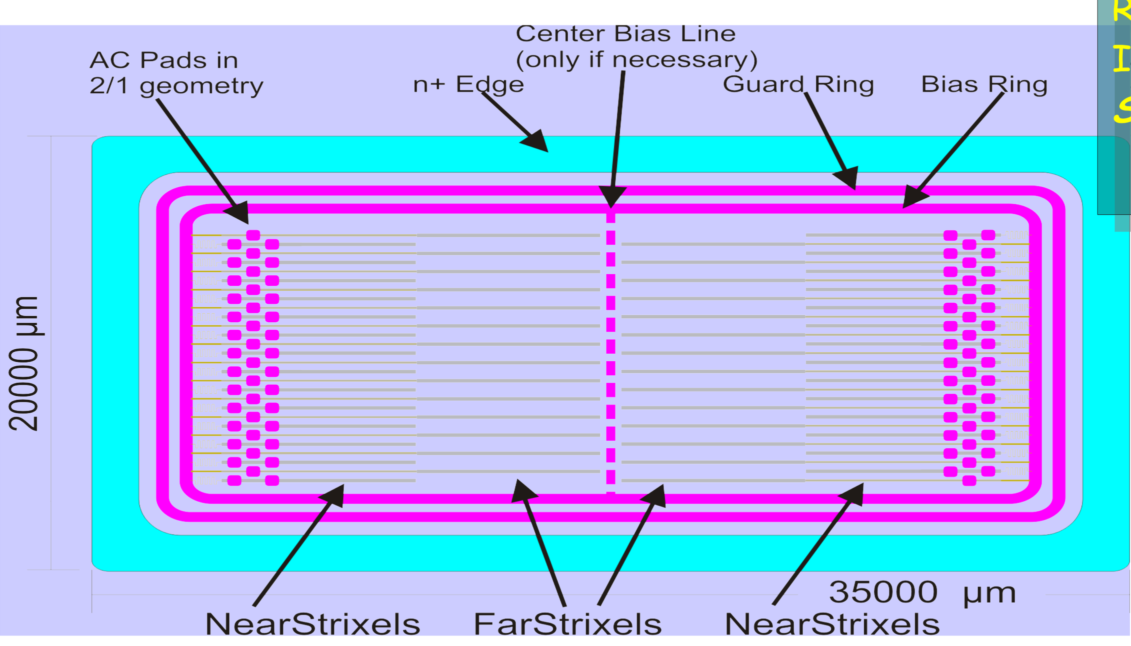
For the very high luminosity phase of the SLHC, about 300 tracks are expected; therefore a tracking system with a very high granularity is mandatory. As a result of the high luminosity the sensors will have to withstand an extreme radiation environment of up to 10^{16} part/cm^2. On this basis, a new geometry with silicon short strip sensors (strixels) is proposed. In order to understand the behaviour of such devices, test geometries are developed whose performance can be verified and optimized using simulation of semiconductor structures. used the TCAD-ISE (SYNOPSYS package) software in order to simulate the main electrical parameters of different strip geometries, for p-in-n type wafers. Several corresponding simulations to make these developments possible are described.

- FarStrixel: p+ is only under the far half of each strixel and is connected to the bias ring with a long PolySiResistor (Option A) or to the Center Bias Line (Option B). A thin metal routing connects the readout strip to the pads.
- NearStrixel: p+ is only under the near (bias) half of each strixel and is connected to the bias ring with a short PolySiResistor. The area with no p+ underneath has no metal above.
- Pitch between FarStrixel – NearStrixel: 50 µm
- Pitch FarStrixel – FarStrixel (NearStrixel –NearStrixel) 100 µm
- Width of p+ is 25 µm

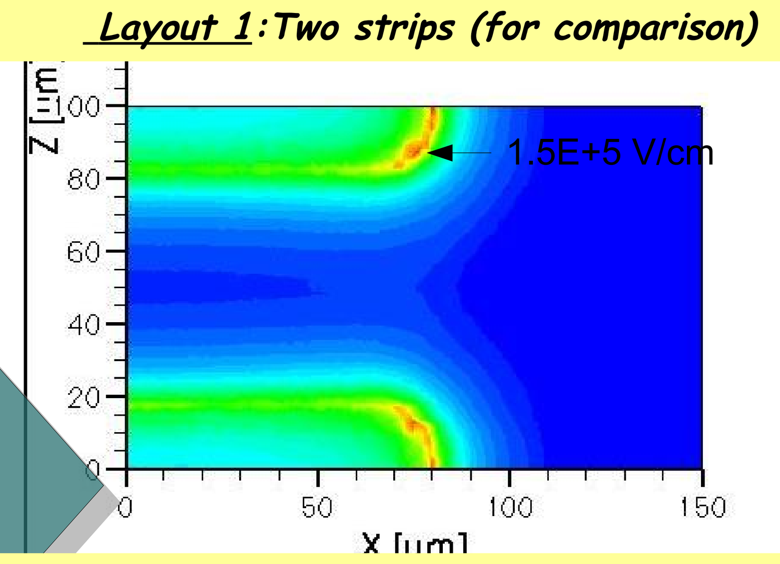


TCAD SYNOPSIS simulations
DEVISE> DESSIS> TECPLOT_ISE

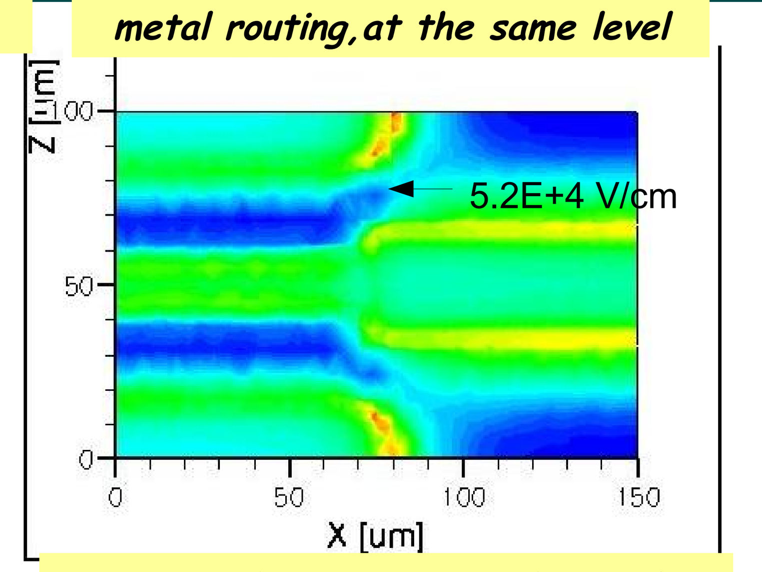
Simulation models used:
Effective Intrinsec Density(Slotboom)
Mobility: eHighFieldSaturation, hHighFieldSaturation, Doping Dependence
Recombination: SRH (Doping Dependence), Avalanche
Material Interface Silicon/Oxide:
Recombination (SRH)
Interface charge: 0.7E+11 q/cm^3
Solver: ILS

Simulated devise parameters:
- n-type silicon bulk, constant doping 1E+12 at/cm^3
- p+ implants on t-type silicon bulk, gaussian shape with Peak of 1E+16 at/cm^3 at 0.3 µm and junction at 1µm;
- Back, ohmic contact with n+ implant 10 µm width;
- Silicon oxide, 200nm
- Aluminium layer 1 µm for AC contact
- For DC simulations the applied bias is 350V; for AC simulations, a 50 mV AC signal is applied, 10 KHz.

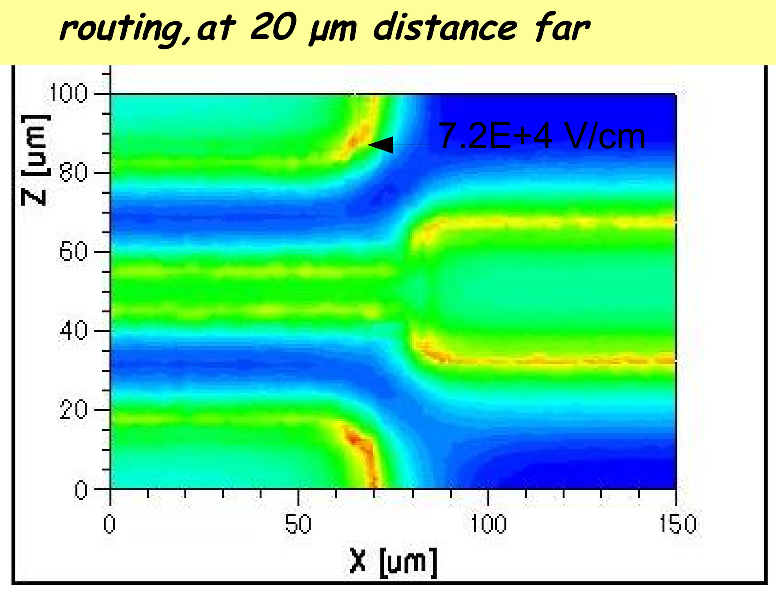
Layout 1: Two strips (for comparison)



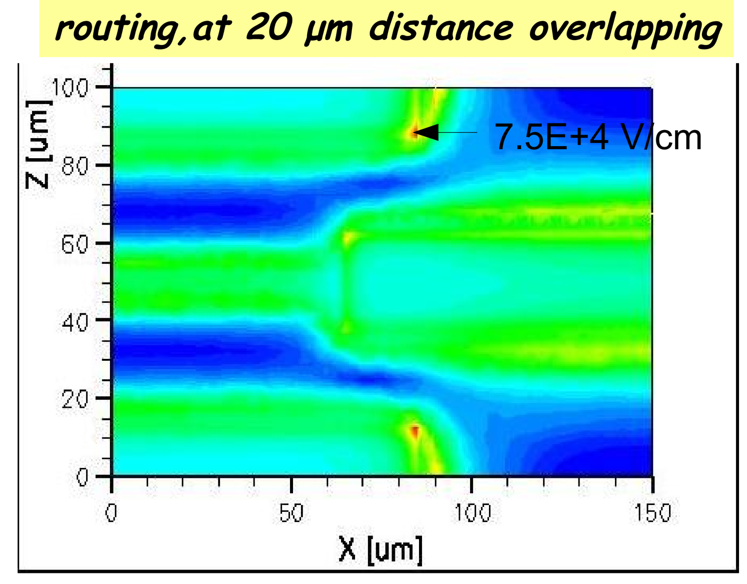
Layout 2: Three strips, with metal routing, at the same level



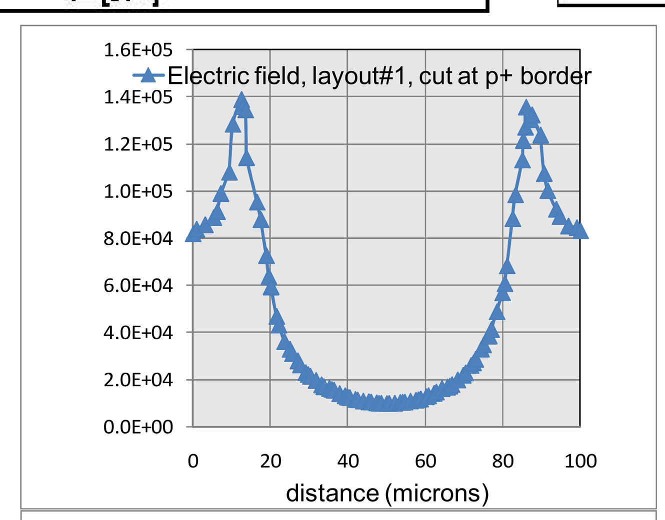
Layout 3: Three strips, with metal routing, at 20 µm distance far

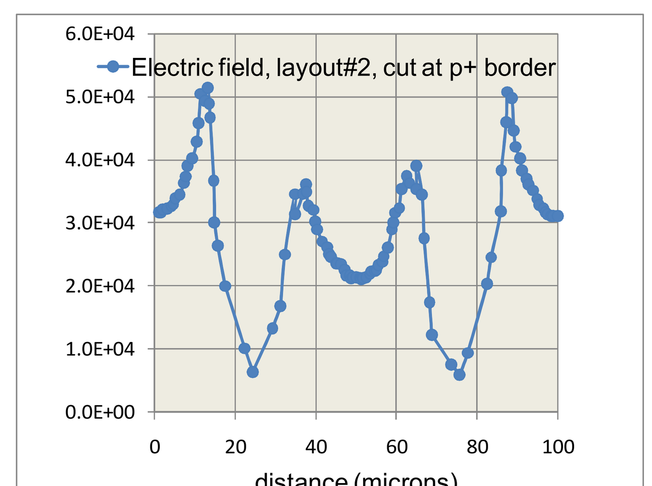


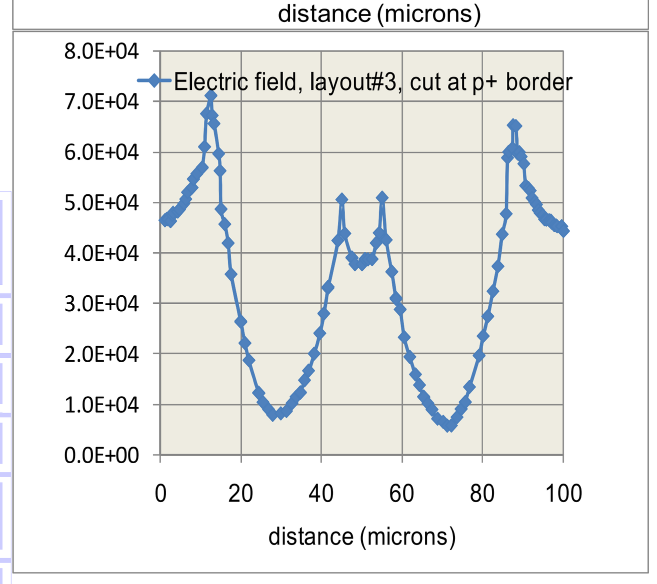
Layout 4: Three strips, with metal routing, at 20 µm distance overlapping

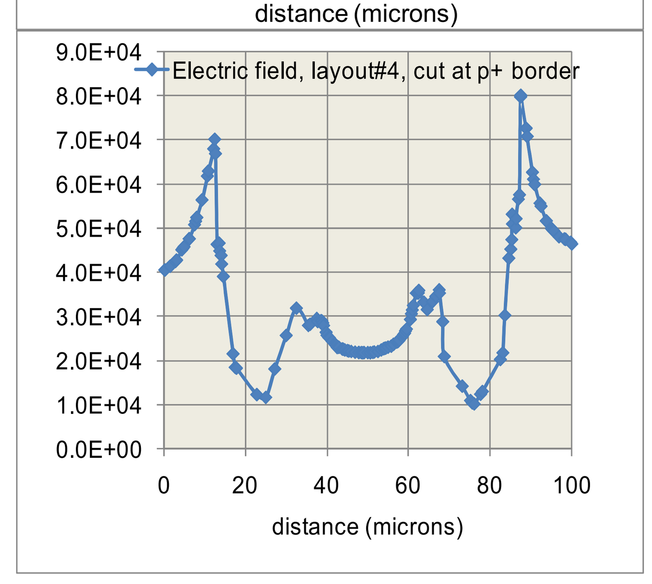


Distribution of the electric field for all four layouts, at 1µm under the surface (2D representation) and at the border of the 'Near' strips P+ implant edge (graphical dependence over z direction).
For layout #1 : the peaks in electric field are given by the junction curvature of the 'Near' strips;
For layout #2 : apart the junction peaks, the metal routing (kept at zero potential) introduces regions of high electric field, along the metal routing stripe;
For layouts #3 and #4: the high electric field given by the metal routing vary little;

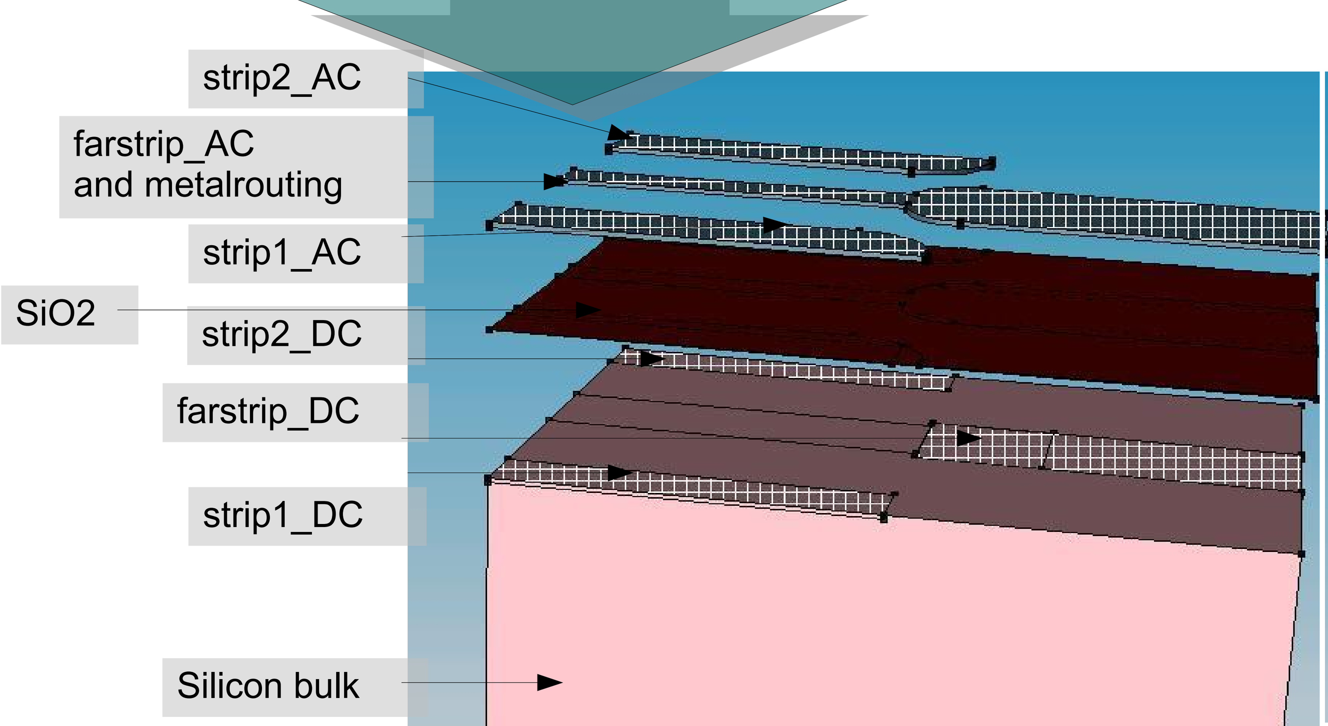


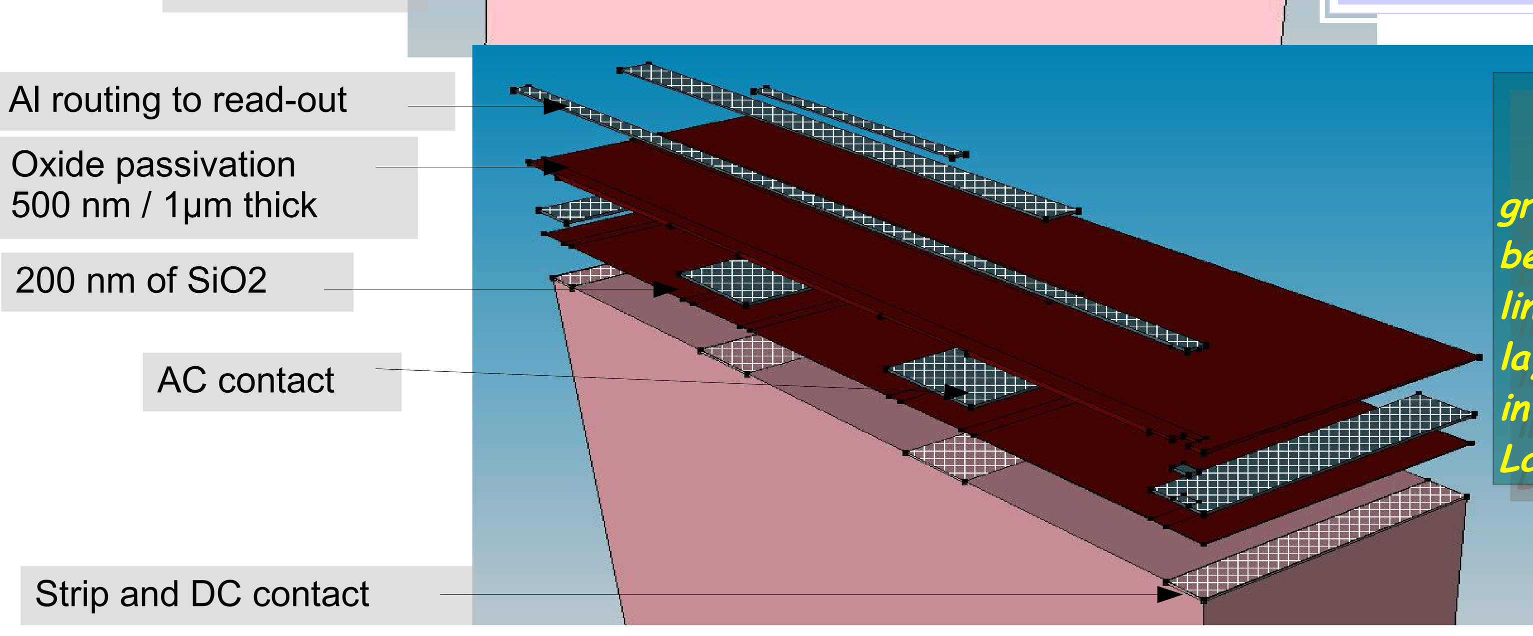




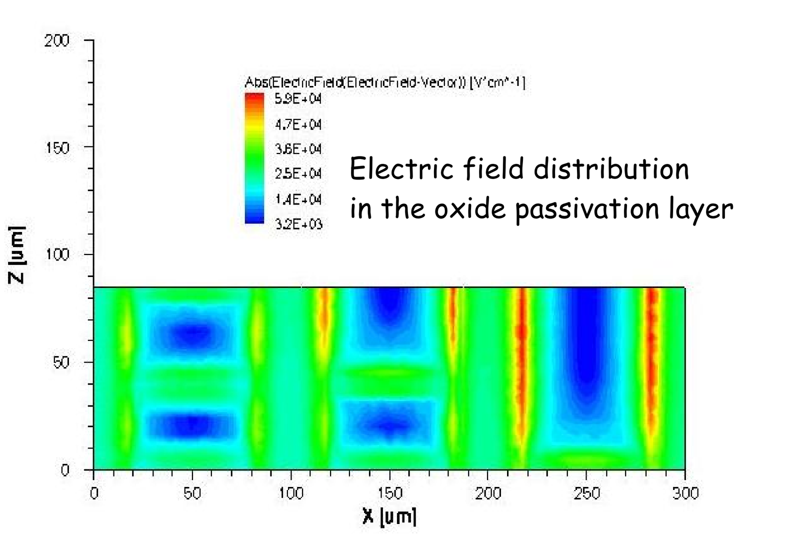


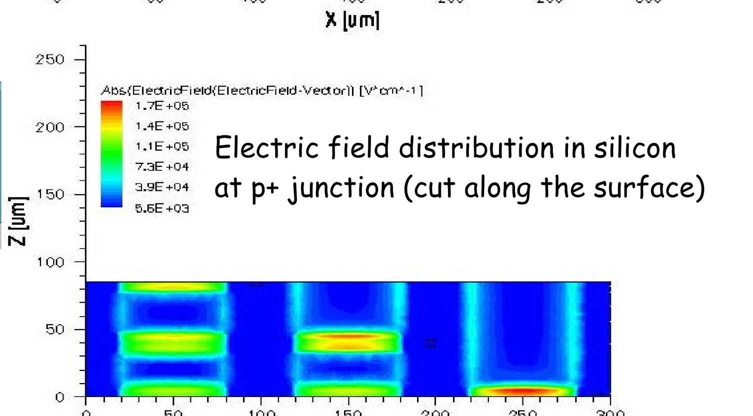
	Layout 1 (pF/cm)	Layout 2 (pF/cm)	Layout 3 (pF/cm)	Layout 4 (pF/cm)
strip1_DC -strip2_DC	0.11	0.05	0.04	0.05
strip1_AC-strip2_DC	0.08	0.03	0.03	0.027
strip1_AC-strip2_DC	0.06	0.02	0.02	0.014
strip1_DC-farstrip_DC/ strip2_DC-farstrip_DC		0.17	0.10	0.16
strip1_DC-farstrip_AC/ strip2_DC-farstrip_AC		0.30	0.20	0.27
strip1_AC-farstrip_AC/ strip2_AC-farstrip_AC		0.22	0.23	0.17
strip1_AC-strip1_DC/ strip2_AC-strip2_DC	24.00	26.00	24.00	27.00
farstrip_AC-farstrip_DC		52.00	50.00	51.70
strip1_AC-farstrip_DC/ strip2_AC-farstrip_DC		0.13	0.07	0.10





For strixel geometry projected, with high granularity, the readout electronics have to be connected to the strips by metal routing lines, which introduce an additional metal layer in the geometry. Double-metal level introduce an extra field stress in the oxide Layers, and cross-talk between electrodes





Conclusion

For the avalanche breakdown process, the structure demonstrates a good resistivity, the metal routing lower the electric field at the Near Strips junction. In Table, can be seen the clear variation of the different components of the interstrip capacitance between neighbour strips. The influence of the opposite strip to this parameter starts to be significant when the Far Strip junction is at the same level or closer to Near Strips.

References
[1] https://twiki.cern.ch/twiki/bin/view/CMS/CEC
[2] http://www.synopsys.com/Tools/TCAD/Pages/default.aspx