In the new KLOE experiment, at DAPHNE particle accelerator of LNF-INFN, a pair of tagger detectors will be installed in order to investigate gamma-gamma physics. We shall need to acquire a 32 bits pattern for each detector and to allow an high time-resolution event reconstruction with KLOE data. To address this issue we are going to use, respectively, R/F (366MHz) and bunch reference (Fiducial) signals from DAPHNE as external clock and reference signal. The first level trigger signal (T1) from KLOE will indicate which data have to be saved and which can be discarded. Due to the high work-frequency, we will implement the data acquisition system with a XILINX Virtex5 FPGA: this choice is cheaper then TDC. The real time sampling and holding system, reference providing bits pattern for each detector and to allow an high time-resolution event reconstruction with KLOE data. To address this issue we are going to use, respectively, R/F (366MHz) and bunch reference (320 MHz) signals.

### Input data characteristics

We shall need to acquire a 32 bits pattern for each tagger detector. Each hit will be 1 DAPHNE R/F period long but, due to detectors, connections and electronic processing delays, its phase relationship is unknown. Electronic noise will also cause signal jittering which could compromise the events reconstruction. The electronic system will have one channel for each bit dedicated to resynchronize the hits to the system clock (R/F). There is also the requirement to refer the data to the DAPHNE Fiducial signal which mark the particles accelerator cycles.

### Acquisition logic general scheme

The aim of the acquisition system is to get data (2 DAPHNE cycles each 32bits pattern) and store it in the RAM every time the trigger signal (T1) from Kloe switches. To make the event reconstruction with Kloe possible some control systems are required (Registers management logic). Great efforts were necessary to design an enough fast electronic system.

### Shift registers and management Logic

The shift registers store every time the last 240 x 32 bits (2 DAPHNE/Fiducial cycles) sampled by the input stages. There is the requirement to refer the data to the Fiducial signal. The Fiducial period is 120 x (R/F PERIOD) and mark the first bunch. Due to noise effects there is also the requirement to check the Fiducial periodicity; Registers Management Logic counts 120 clock beats each Fiducial period and generate a 2 bits control signal (management, alias gestione).

### General scheme

The acquisition logic is a part of a microcomputer system implemented with the Virtex 5. This computer allows to interface with a personal computer trough RS232 or with others processors trough BUS line. The Microblaze accesses data trough a Dual Port RAM.

### Input stage

In order to make possible data digital recording and processing, we need to re-synchronize (lower figure) incoming data signals with the system clock (DAPHNE R/F). The Xilin XAPo225 “Data to clock phase alignment” circuit addresses this issue up to 500MHz.

### System tests require very fast pattern generator. We used a Tektronix TLA7016 Logic Analyzer for testing up to 270 MHz. For testing up to 500 MHz we implemented a very simple pattern generator with a Virtex5 FPGA. So, the test bench is made up of a clock generator (Wavelet Synthesiz ed Signal Generator 2410 and a Motorola E116 LVDS_25 converter), two Virtex5 ML505 evaluation boards, a personal computer and a LeCroy 104MXi 1GHz oscilloscope.

### Conclusion

Great efforts were done to design an enough fast electronic system. We finally reached the wanted results. One Virtex5 XC5VFX70T -1 can be used to implement a 32 bits pattern acquisition system. A lot of communication systems with outside apparatuses, using Microblaze or PowerPC embedded processors, are feasible and make possible to use this system with different experiments. This acquisition system can be easily used to implement a coincidences detection system between the two tagger detectors. Other acquisition techniques are under consideration.