Data Acquisition System for Gamma-Gamma Physics at KLOE

Iafolla Lorenzo[12], Archilli Flavio[12], Babusci Danilo[3], Badoni Davide[2], Beretta Matteo[3] , Gonnella Francesco[12], Messi Roberto[12], Moricciani Dario[2]

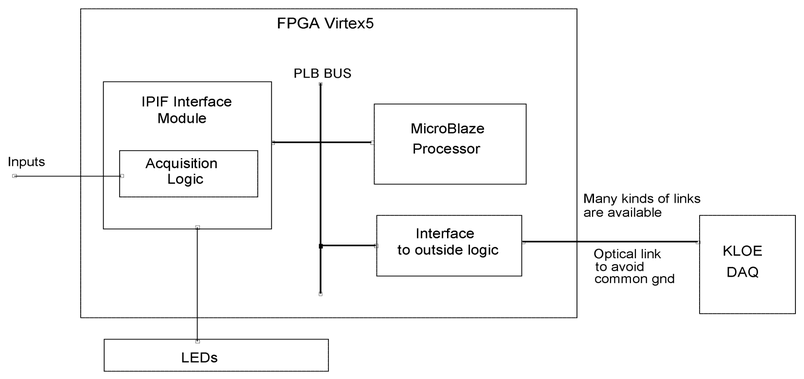
[1]Università degli Studi di Roma "Tor Vergata",
[2]INFN, sez. "Tor Vergata",
[3]INFN, Laboratori Nazionali di Frascati

In the new KLOE experiment, at DAPhNE particle accelerator of LNF-INFN, a pair of tagger detectors will be installed in order to investigate gamma-gamma physics. We shall need to acquire a 32 bits pattern for each detector and to allow an high time-resolution event reconstruction with KLOE data. To address this issue we are going to use, respectively, R/F (366MHz) and bunch reference (Fiducial) signals from DAPhNE as external clock and reference signal. The first level trigger signal (T1) from KLOE will indicate which data have to be saved and which can be discarded. Due to the high work-frequency, we will implement the data acquisition system with a XILINX Virtex5 FPGA: this choice is cheaper then TDC. The real time sampling and holding system, reference providing system, memorization and transfer data system will be described.

Input data characteristics

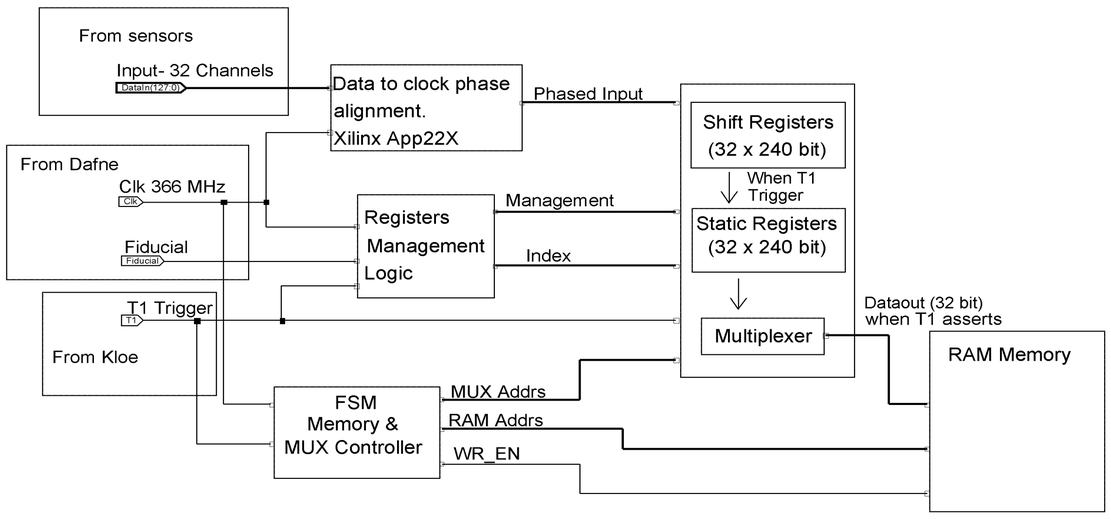
We shall need to acquire a 32 bits pattern for each tagger detector. Each hit will be 1 DAPhNE R/F period long but, due to detectors, connections and electronic processing delays, its phase relationship is unknown. Electronic noise will also cause signal jittering which could compromise the events reconstruction. The electronic system will have one channel for each bit dedicated to resynchronize the hits to the system clock (R/F). There is also the requirement to refer the data to the DAPhNE Fiducial signal which mark the particles accelerator cycles.

General scheme



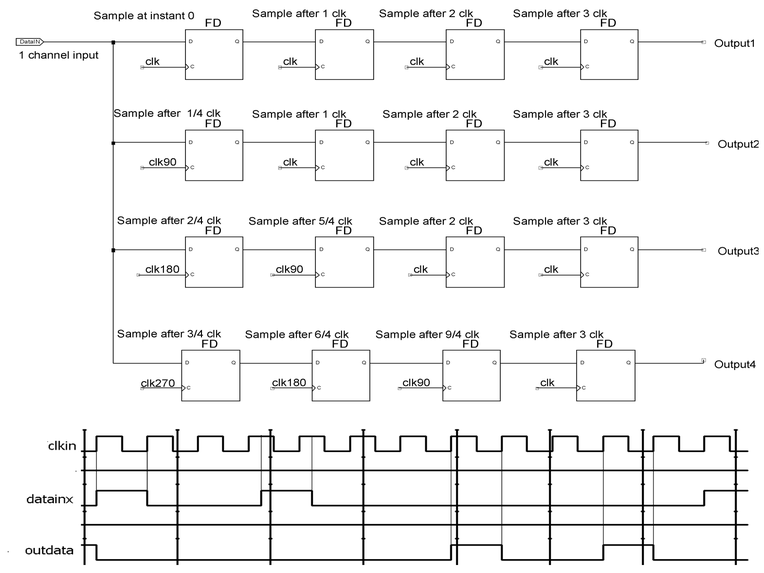
The acquisition logic is a part of a micro-computer system implemented with the Virtex 5. This computer allows to interface with a personal computer trough RS232 or with others processors trough BUS line. The Microblaze accesses data trough a Dual Port RAM.

Acquisition logic general scheme



The aim of the acquisition system is to get data (2 DAPhNE cycles each 32bits pattern) and store it in the RAM every time the trigger signal (T1) from Kloe switches. To make the event reconstruction with Kloe possible some control systems are required (Registers management logic). Great efforts were necessary to design an enough fast electronic system.

Input stage



In order to make possible data digital recording and processing, we need to re-synchronize (lower figure) incoming data signals with the system clock (DAPhNE RF). The Xilinx XApp225 "*Data to clock phase alignment*" circuit addresses this issue up to 500MHz. The method is to sample the data on four phases of the same clock (upper figure), decide which phase is the most "valid", and then resynchronize the data to the system clock.

Shift registers and management Logic

The shift registers store every time the last 240× 32 bits (2 DAPhNE/Fiducial cycles) sampled by the input stages. There is the requirement to refer the data to the Fiducial signal. The Fiducial period is 120 x (R/F PERIOD) and mark the first bunche. Due to noise effects there is also the requirement to check the Fiducial periodicity: *Registers Management Logic* counts 120 clock beats each Fiducial period and generate a 2 bits control signal (*management*, alias *gestione*).

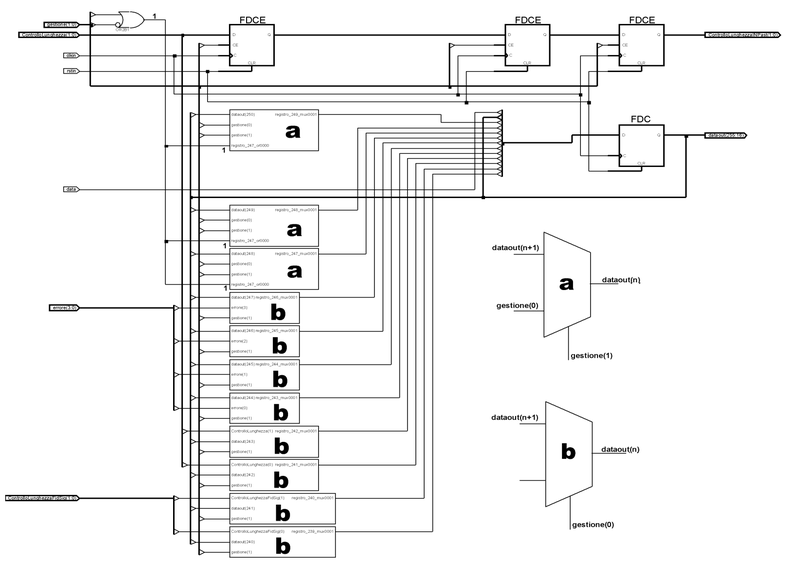


Fig. 1 Shift register

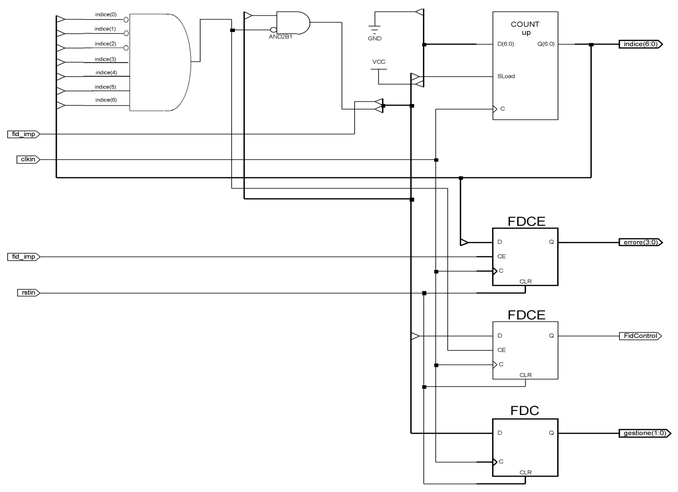
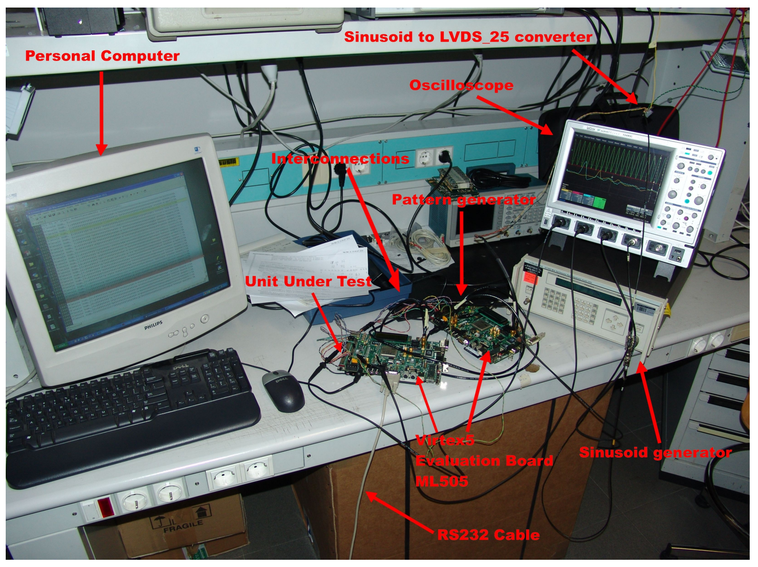


Fig. 2 Register Management logic

This signal tells the shift-registers if the Fiducial switched and its periodicity is correct.
The last 20 data bits of each Fiducial cycle are unimportant cause they don't carry any information (the corresponding bunches don't contain any particle): we used these 20 bits to save some useful information to restore the input stream with respect to the Fiducial.

Test bench and implementation system



System tests require very fast pattern generator. We used a *Tektronix TLA7016 Logic Analyzer* for testing up to 270 MHz. For testing up to 500 MHz we implemented a very simple pattern generator with a *Virtex5* FPGA. So, the test bench is made up of a clock generator (*Wavetek Synthesized Signal Generator 2410* and a *Motorola E116* LVDS_25 converter), two *Virtex5 ML505* evaluation boards, a personal computer and a *LeCroy 104MXi 1GHz* oscilloscope.

We checked the recorded data using oscilloscope. The electronic systems worked properly up to 450 MHz with 32 channels on a *Virtex5 XC5VFX70T -1* and up to 500MHz with 24 ch. The *Virtex®-5* family provides the newest most powerful features in the FPGA market. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks. Additional platform dependant features include also high-performance *PowerPC® 440* microprocessor embedded blocks. The 550 MHz clocking technology is, of course, one of the most interesting features in our application.

Conclusions

Great efforts were done to design an enough fast electronic system. We finally reached the wanted results. One Virtex5 *XC5VFX70T* -1 can be used to implement a 32 bits pattern acquisition system. A lot of communication systems with outside apparatuses, using Microblaze or PowerPC embedded processors, are feasible and make possible to use this system with different experiments. This acquisition system can be easily used to implement a coincidences detection system between the two tagger detectors.
Other acquisition techniques are under consideration.