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Front-end Electronics for DEPFET Pixel Detectors at SuperBelle

Hans Krüger, University of Bonn
for the DEPFET Collaboration

The DEPFET Collaboration

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- University of Barcelona(*)
- University Ramon Lull, Barcelona
- University of Bonn(*)
- University of Heidelberg(*)
- University of Giessen
- University of Göttingen
- University of Karlsruhe
- IFJ PAN, Krakow
- MPI Munich
- Charles University, Prag
- University of Santiago de Compostela
- IFIC Valencia

Collaboration started with µVTX R&D for ILC – now in good position for PXD development for Belle 2

(*) ASIC design activity

Overview

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- Upgrade of the Belle detector at KEKB – Belle 2 (aka SuperBelle)
- Detector concept
- Front-end electronics
- Prototype results

Upgrade of the KEK B factory

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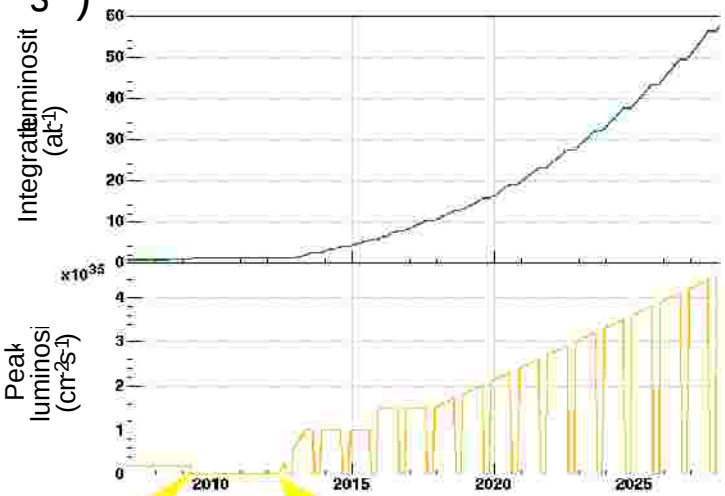
Belle detector

- Asymmetric e^+/e^- collider (3.5 GeV, 8 GeV)
  - 900 million B meson pairs (since 1999)
  - study CP violation via B^0/B^0-bar decays
  - rare decay modes à need even more statistics

- Machine upgrade: Super KEK B
  - increase luminosity (1.7×10^{34} è up to 8×10^{35} $cm^{-2}\,s^{-1}$)
  - high beam current (9.4/4.1A) or
  - nano beam
  - crab crossing
  - …



2009: shutdown

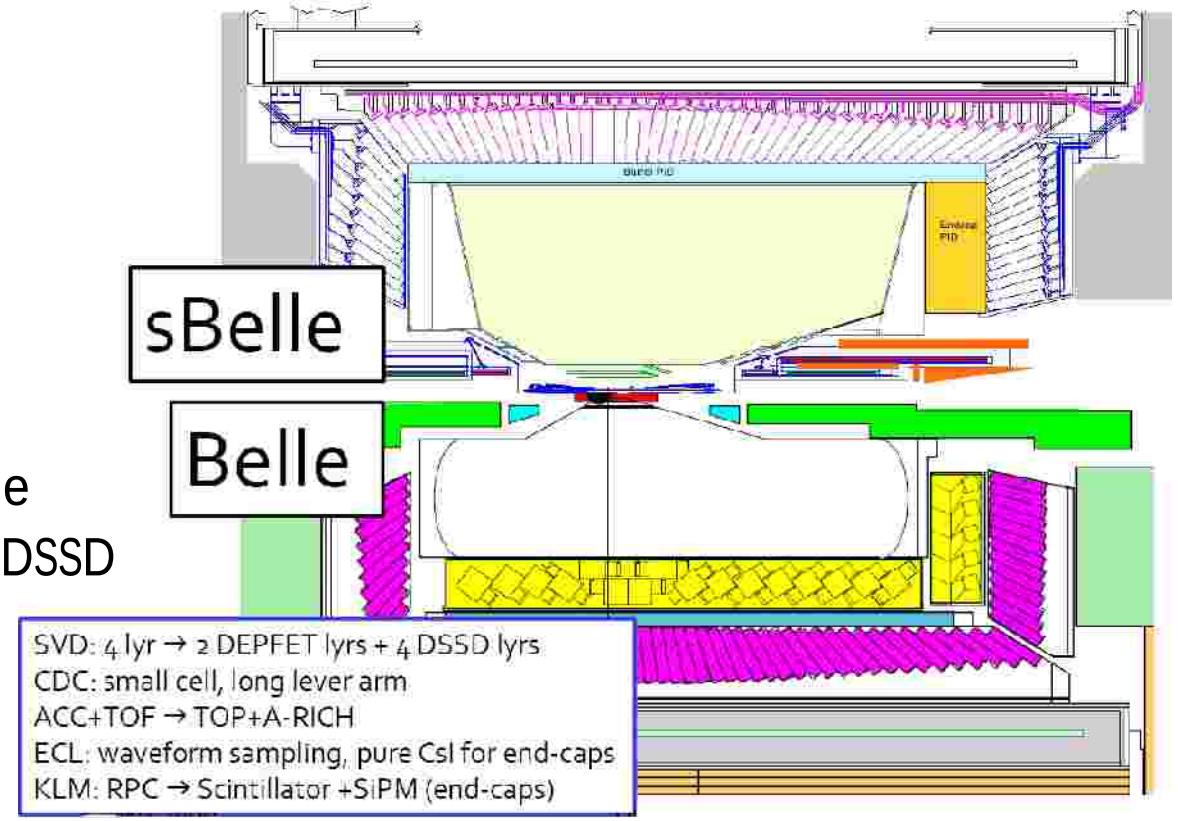
2013: start of Belle2 operation

Belle Detector Upgrade – SuperBelle

- various upgrades for all sub detectors
  - background reduction
  - vertex resolution
  - rate capability
  - particle identification

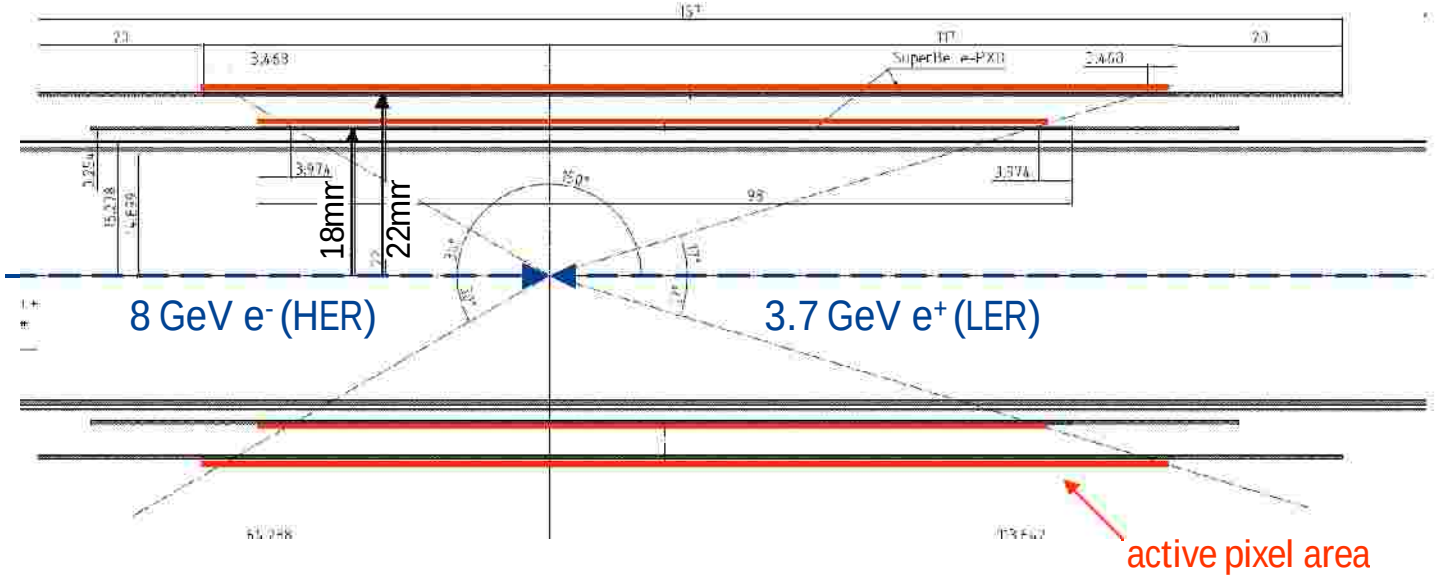
- silicon vertex detector upgrade

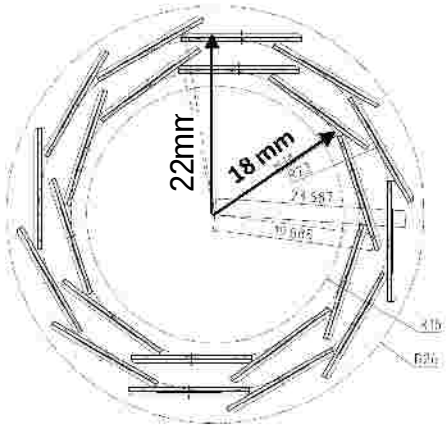
4 layer DSSD à 2 layer pixels + 4 DSSD



- challenges for the detector
  - higher background (x20) à radiation damage, occupancy
  - higher event rate (x50) à higher trigger rate, DAQ, computing

DEPFET Pixel Vertex Detector – PXD





- Two layer vertex detector
  - layer 1: 10 modules at 1.8 cm radius
  - layer 2: 12 modules at 2.2 cm radius
  - optional layer 0 at 1.3 cm radius with beam pipe upgrade
  - 17° - 150° acceptance (η = [0.55 .. 0.3])

Some more Specifications…

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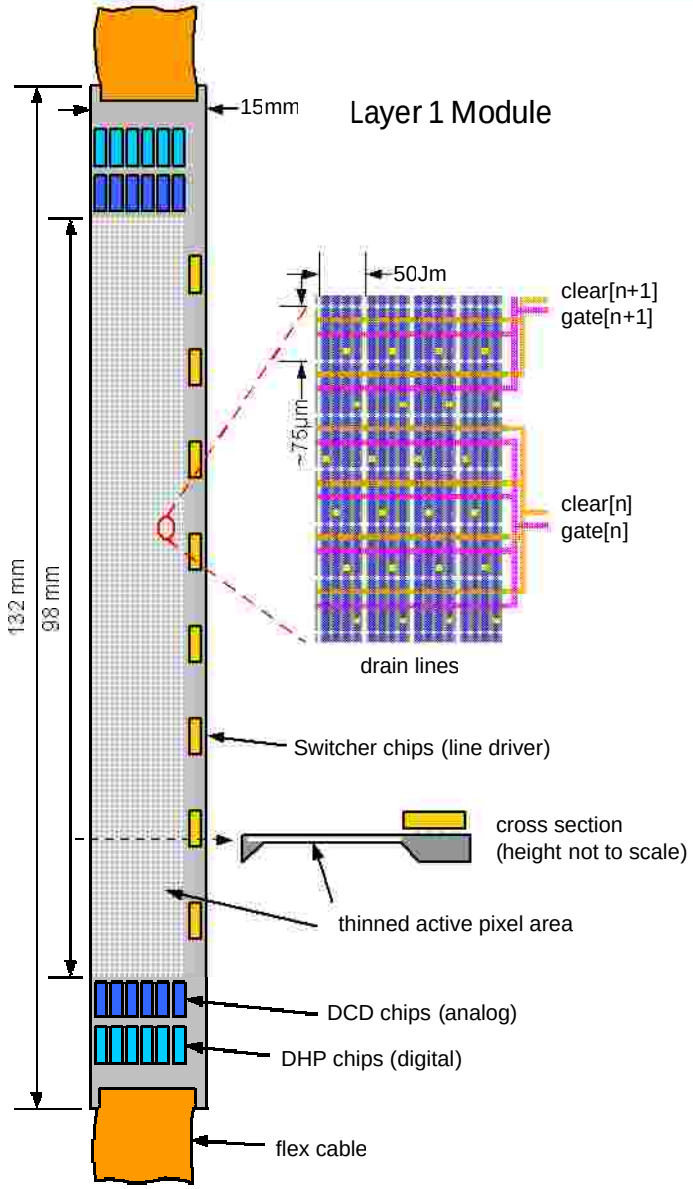
- occupancy: ~0.2 hits/μm^2/sec (estimated for $1x10^{35}$ $cm^{-2}sec^{-1}$, @ 1.8cm radius)
- spatial resolution : < 10 µm (r-phi) (can be less in z)
- pixel size: 50 µm (r-phi) x ~60 µm (z-axis)
- material budget < 0.15 % X_0 per layer
- read-out time: 10 µs (20µs)
- sample (row) rate: 12 MHz
- layer1 half-module active area: 4.9 cm x 1.2 cm
- #pixels: 240 x 500 (800)
- anticipated radiation: ~1 Mrad per year of operation

“All-silicon” DEPFET Module

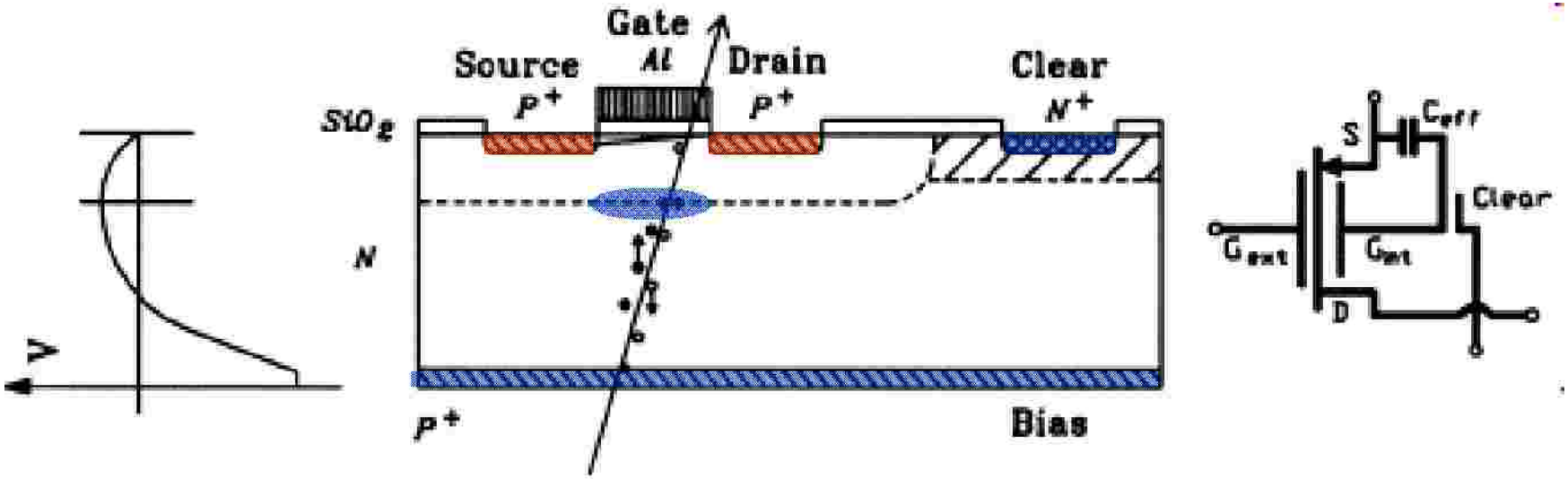
- active pixel area thinned to 50 µm
  - low mass design
- surrounding (non-thinned) frame
  - mechanical support
  - mounting and routing for the ASICs
- ASICs bump bonded directly to the DEPFET substrate
- Independent read-out from both sides (half modules)

see talk by Carlos Lacasta on Friday afternoon for more details on the DEPFET sensor design & performance



The DEPFET Principle

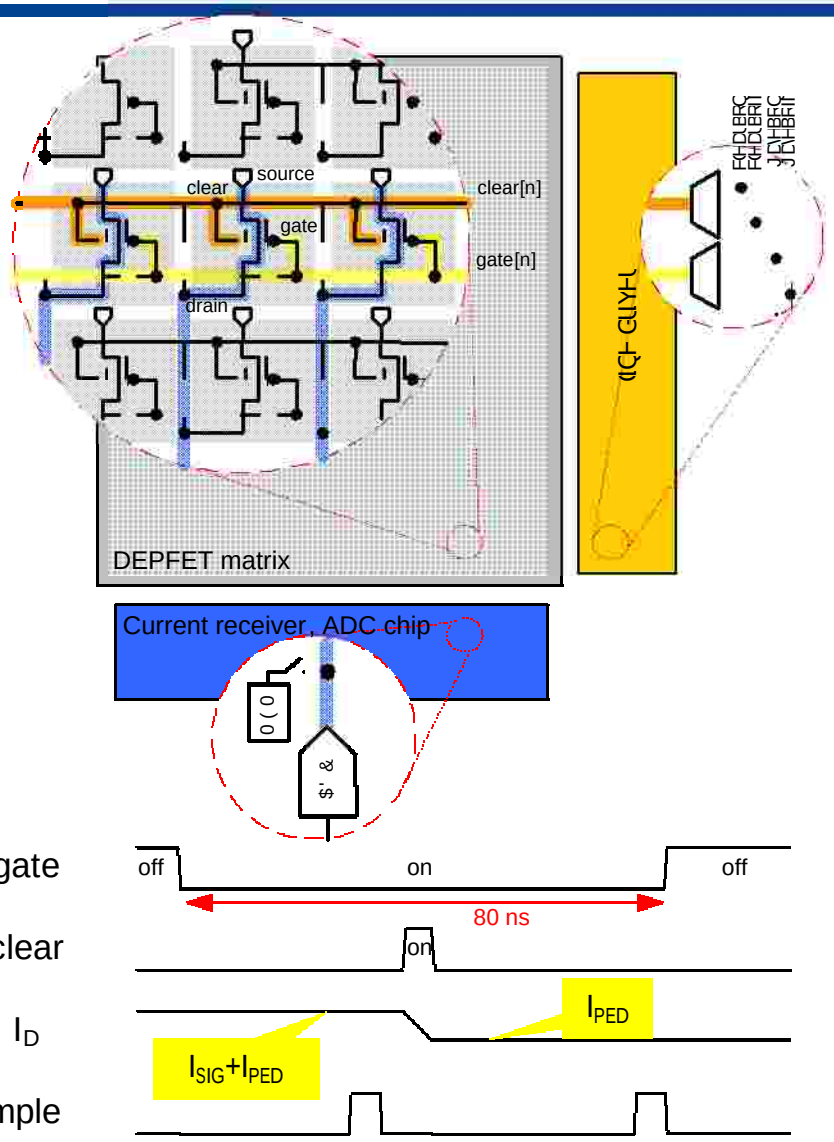
- p-FET (MOSFET) integrated in the sensor substrate
- fully depleted bulk (sideward depletion)
- internal gate (deep n implantation) collects signal electrons à low C_D, low noise
- charge collection during external gate being switched off à low power
- integrating device, discharge internal gate with positive pulse applied to the clear contact



J. Kemmer and G. Lutz Nucl. Instr. and Meth. A 253 (1987), p. 365

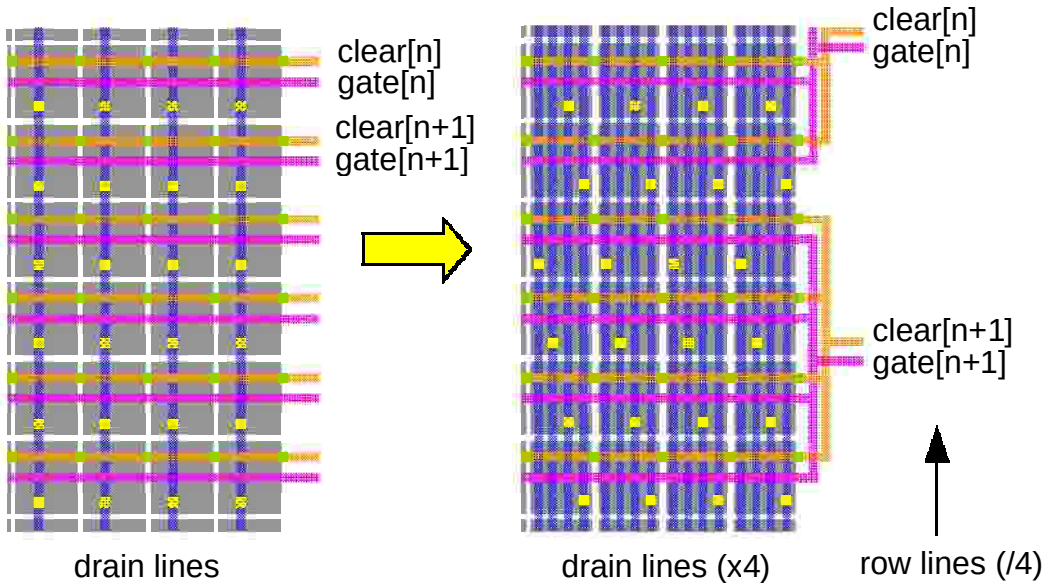
DEPFET Matrix Read-out

- ‘correlated double sampling’
  1. one row selected at a time
  2. sample drain current (I_{ped} + I_{sig})
  3. clear internal gates of selected row
  4. sample drain current (I_{ped}) again and subtract from stored current à I_{sig}
  5. digitize I_{sig}
- clear requirements (complete clear)
  > 10V swing
  > 15 ns pulse width
- read-out speed
  – drain (current) read-out à low voltage swing
  – low input resistance of the r/o chip



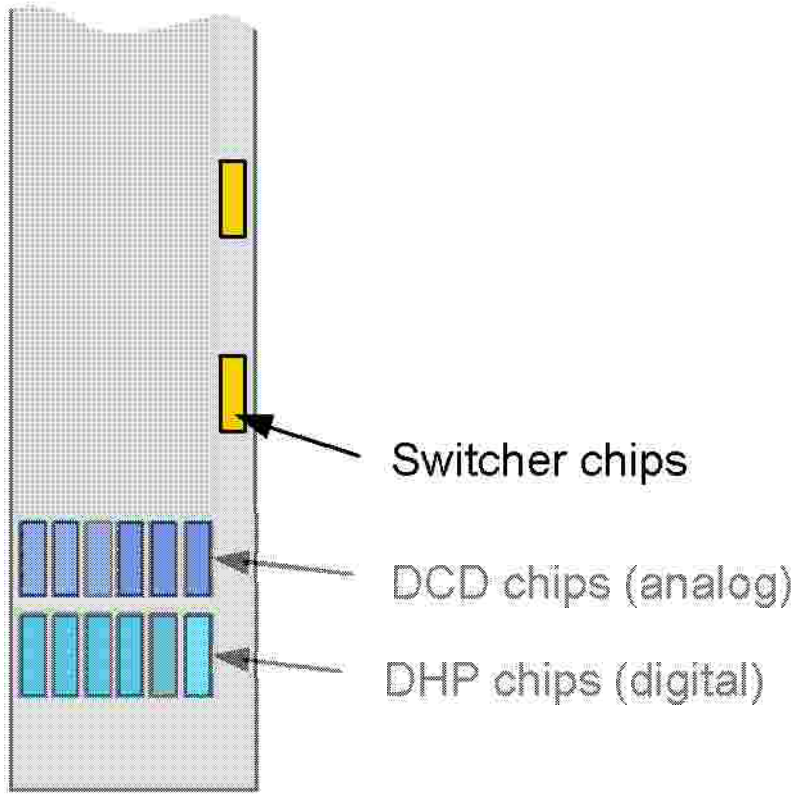
DEPFET Matrix Layout

- 4-fold parallel column read-out
  - increase r/o speed by x4
  - reduced number of line driver channels (rows)
  - less material in the acceptance region
  - 50 µm pixel width à 12.5 µm drain line pitch (technology limit)
  - need to flip chip the read-out chip



increase read-out speed (x4)

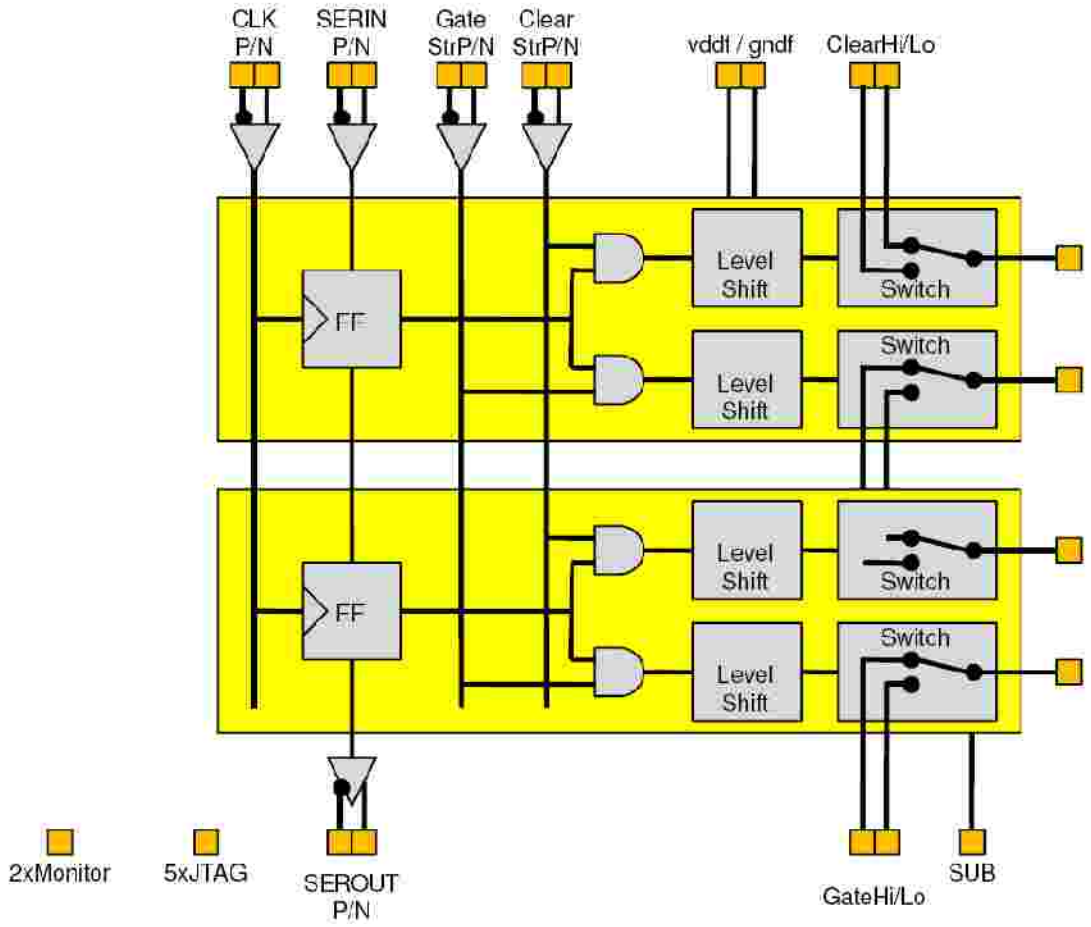
Switcher Chip (Line Driver)



Switcher Chip Block Diagram

- high voltage (10-20V) pulses for clear and gate lines
- low output resistance (speed)
- radiation hard
- low power
  (chip inside acceptance volume)

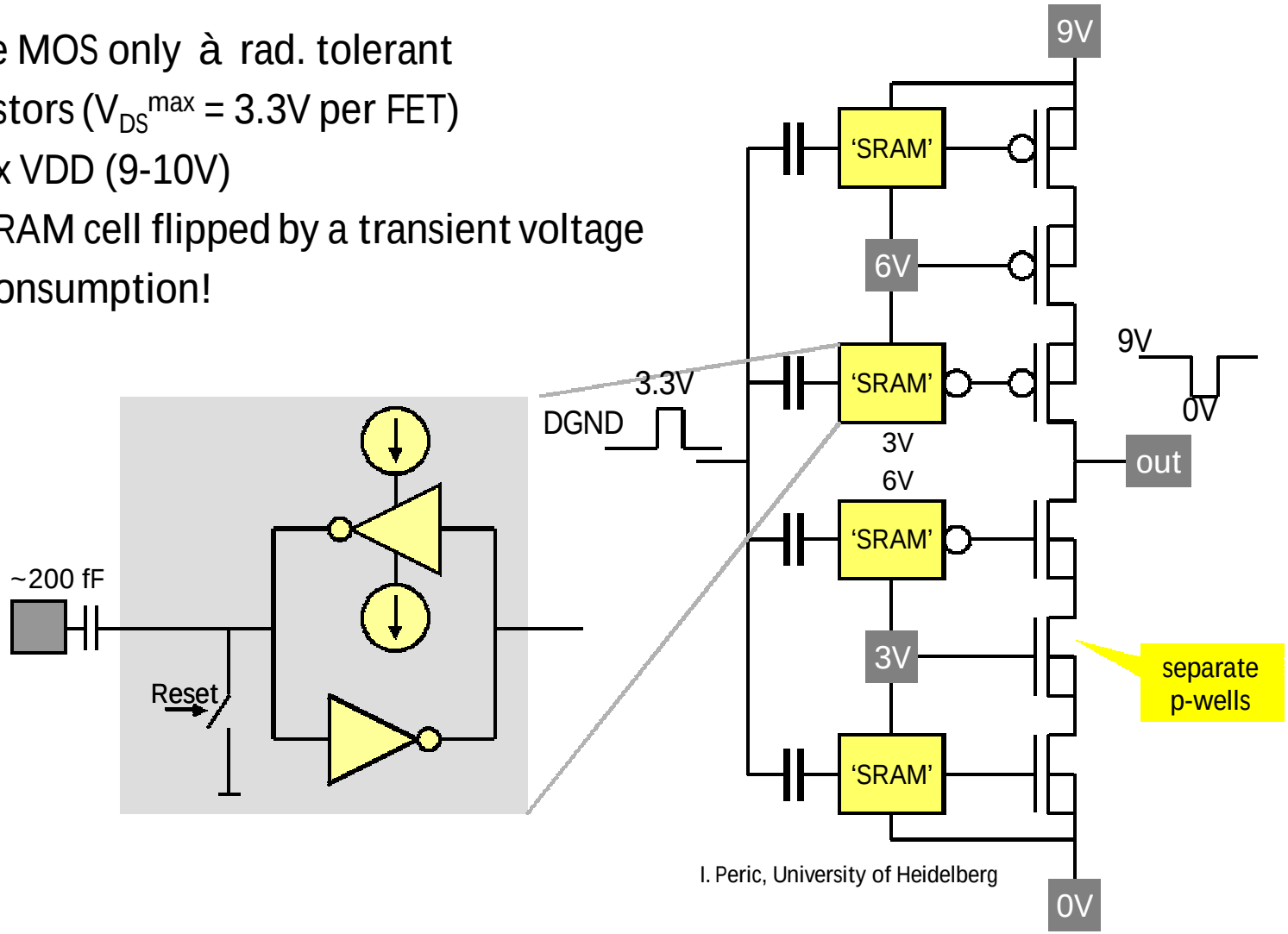
- Switcher chip developments (ILC, X-ray astronomy):
  - Switcher 2: 64 ch., analog l.s., dU = 25 V
  - Switcher 3: 128 ch., cap. l.s., dU = 10V
  - Switcher 4: 64 ch., analog l.s., dU > 30V
  - Switcher 5 (sBelle): tbd.



I. Peric et al, University of Heidelberg

Switcher 3 – Concept

- thin gate oxide MOS only à rad. tolerant
- stacked transistors (V_{DS}^{max} = 3.3V per FET)
- max dU_{out} = 3 x VDD (9-10V)
- level shifter: SRAM cell flipped by a transient voltage
- no dc power consumption!



Switcher 3 – Implementation

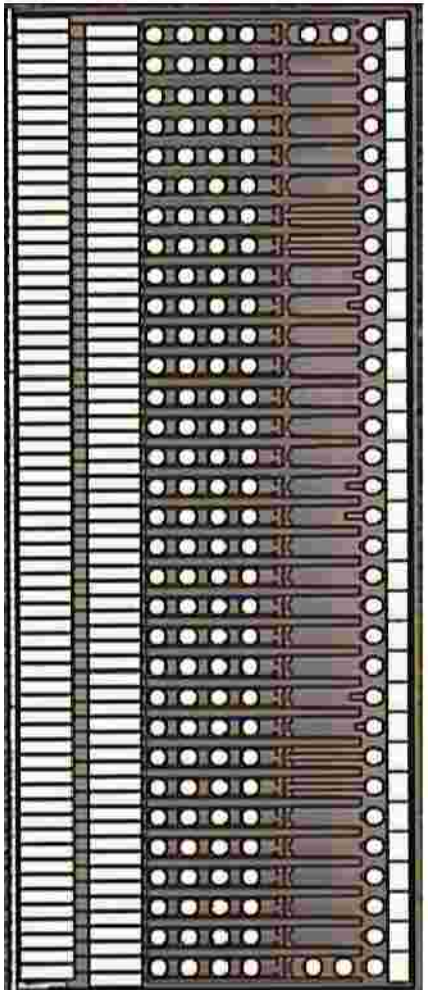
- Radiation tolerant layout in 0.35 µm twin-well technology
- 128 channels
- programmable sequencer

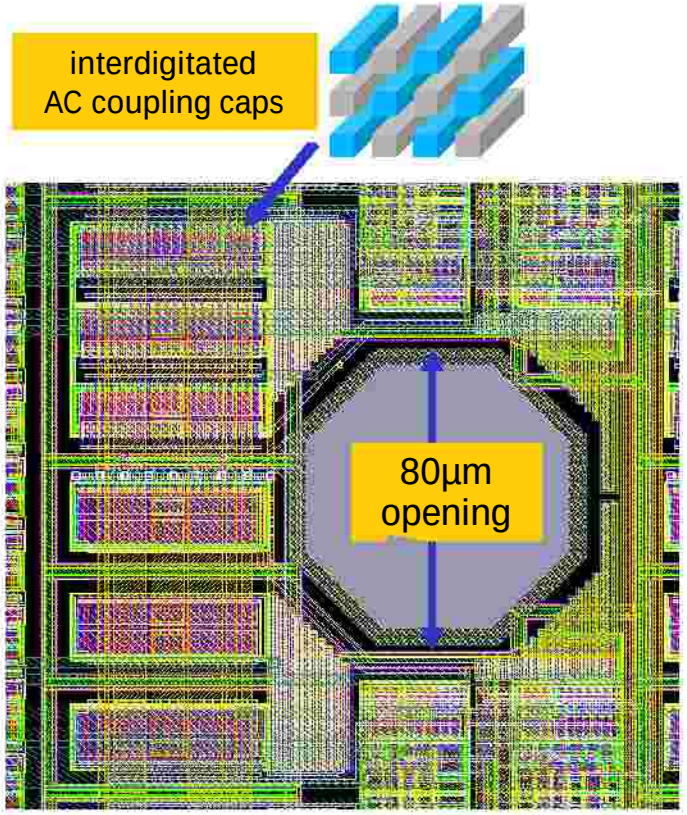
pro:

- very fast
- no DC power consumption

con:

- operation limited to 11.5 V
- need separate chips for clear and gate
- SEU in SRAM level-shifters can cause shorts





HV channel with 3+3 Switch transistors and
4 AC coupling stages (180x180µm, M4 not shown)

I. Peric, University of Heidelberg

Switcher 3 – Measurements

up to 5.7 Mrad:

- chip running with 50 MHz clock
- increased rise/fall times

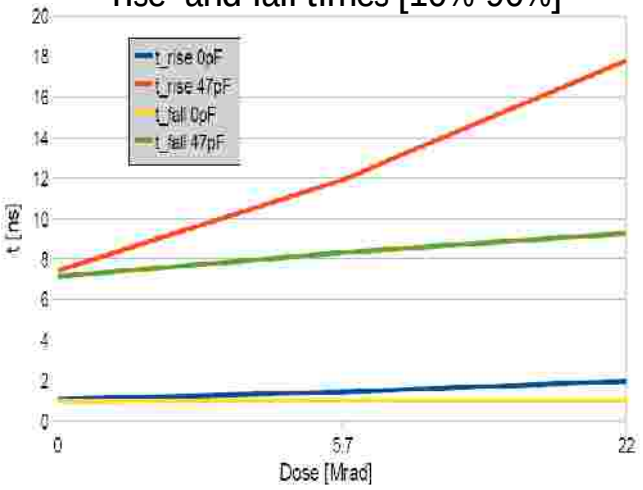
after 22 Mrad:

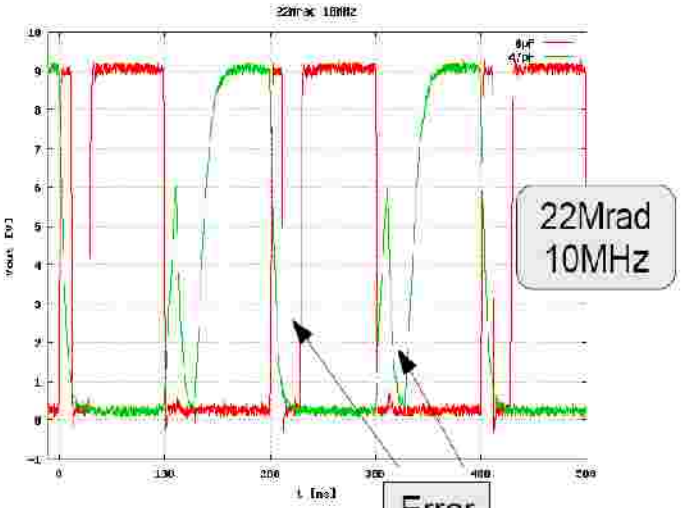
- digital errors
- even with lower (10 MHz) clock

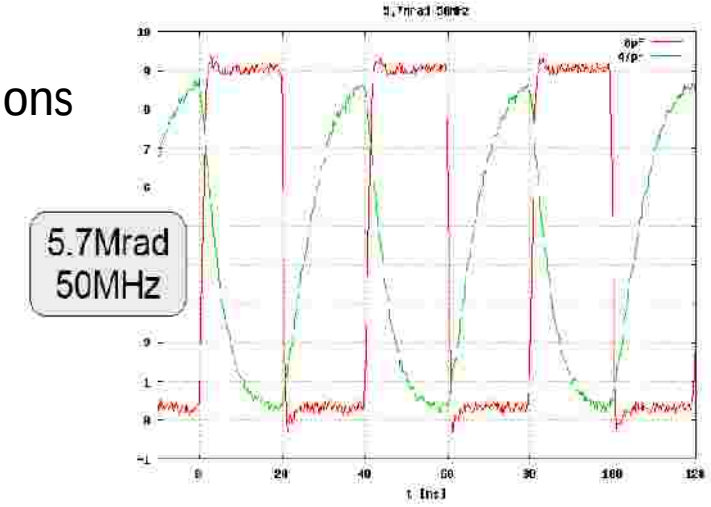
reminder: Belle 2 conditions

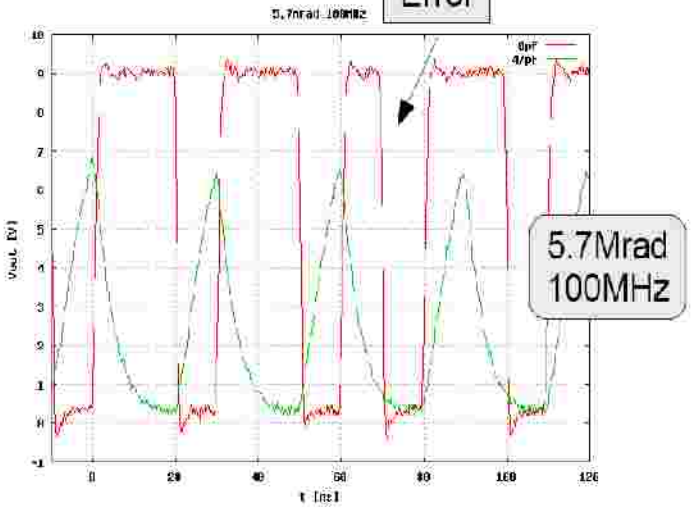
- ~1Mrad/yr
- 12 MHz clock

rise- and fall times [10%-90%]







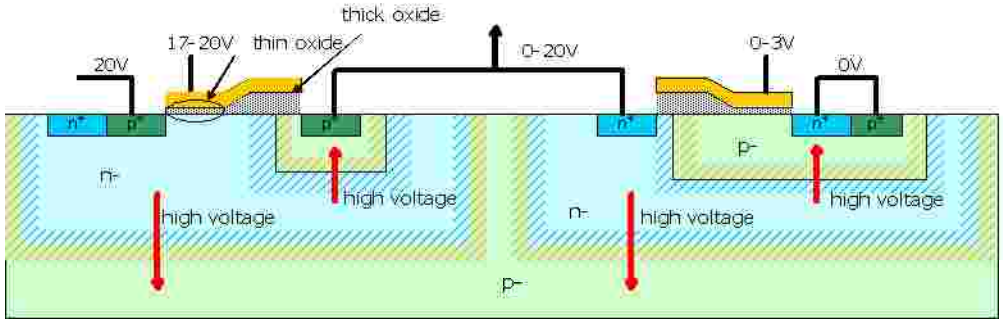


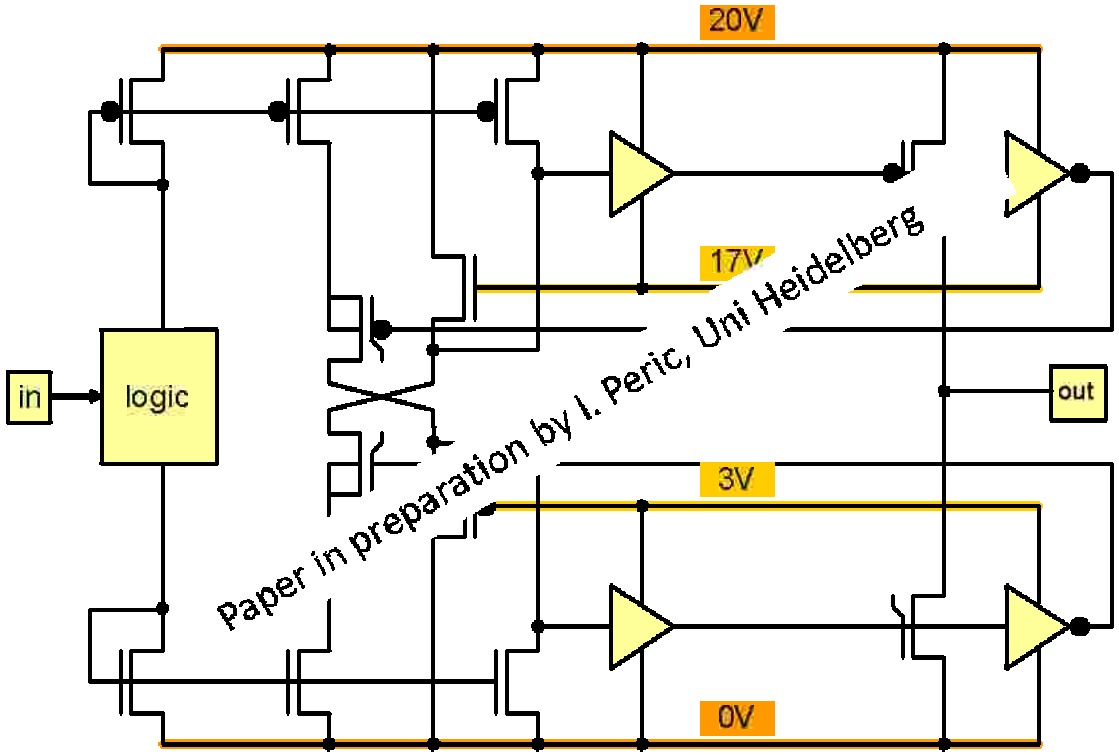
C. Kreidl, University of Heidelberg

Switcher 4 – Concept

- new concept to achieve higher voltage swings
- 0.35 HV technology
  - rad. tolerant thin gate oxide MOS
  - lateral diffusion MOSFETs (LDMOS) for high voltage
  - rad. tolerant, enclosed design of NMOS HV transistors

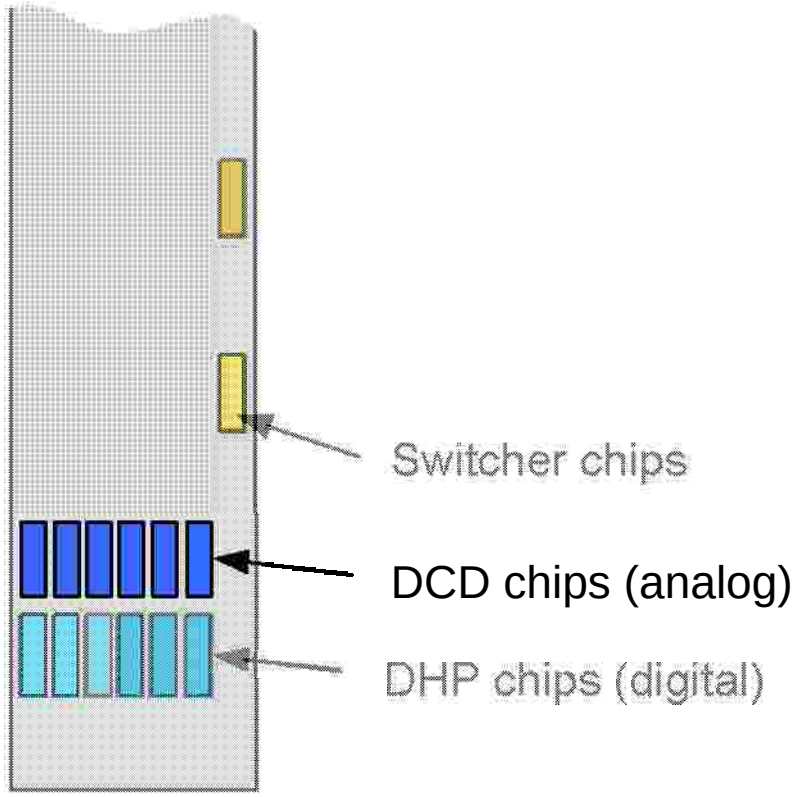
- block diagram
  - drive N- and P-MOS output switches from separate rails (3V & 17V, generated on-chip)
  - 'break before make' switching





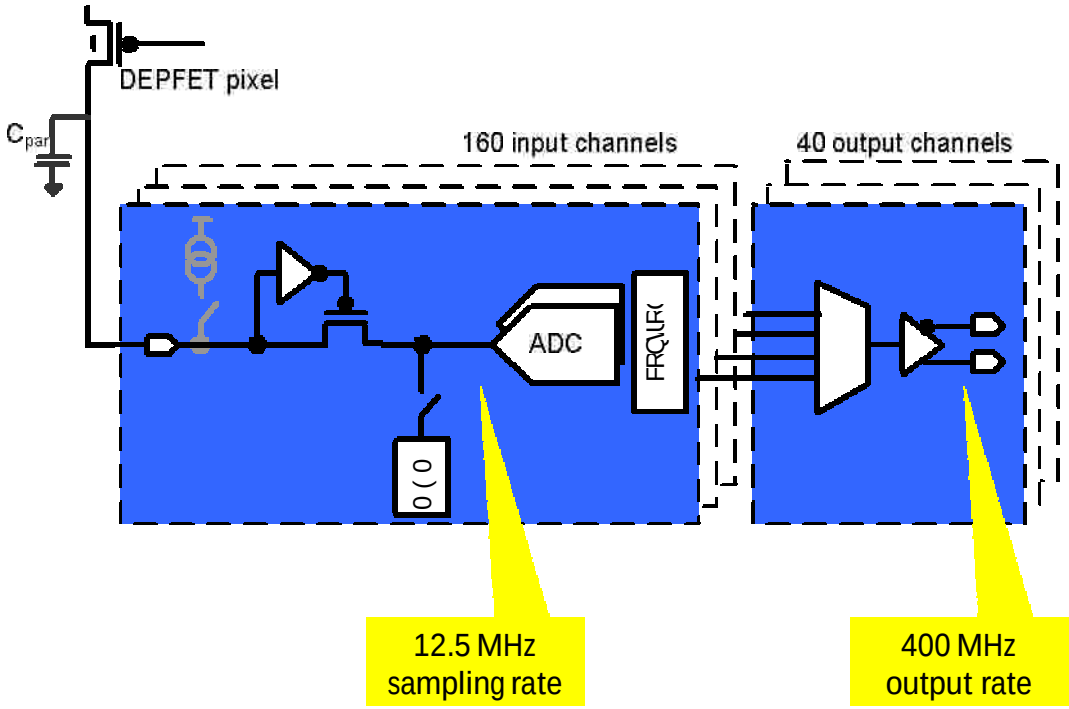
I. Peric, University of Heidelberg

Drain Current Digitizer – DCD



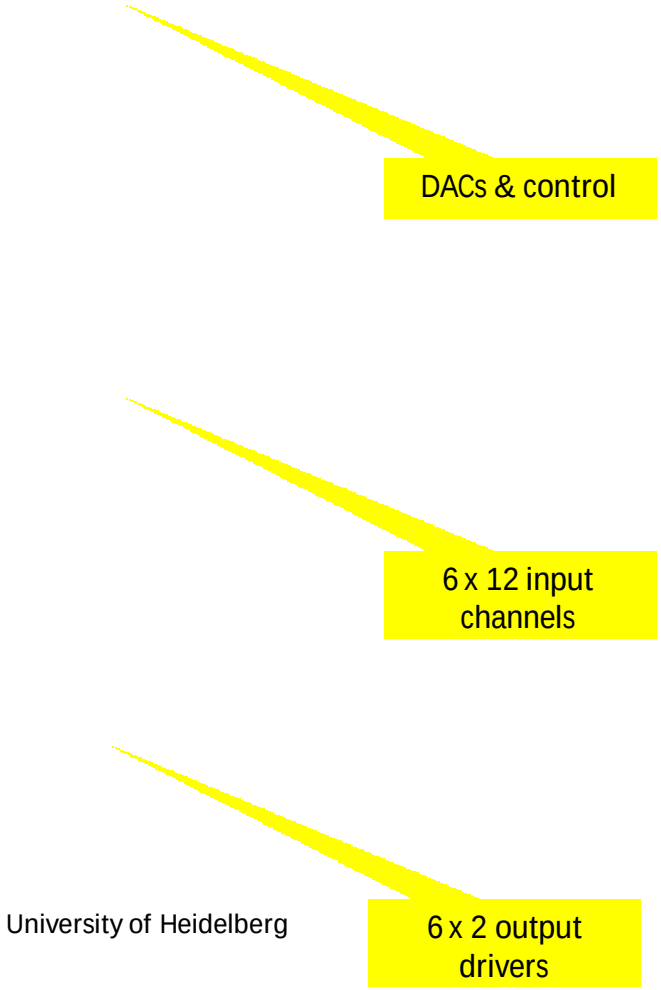
Drain Current Digitizer – DCD Chip

- receive drain current signals from the DEPFET matrix
  - need low r_{in} for fast settling time (C_{PAR} ~50 pF)
  - regulated cascode
- sample and subtract pedestal currents
  - current memory cells
- digitize signals
  - algorithmic ADC, 8 bit, 160 ns
  - two ADCs per channel à 80 ns
  - serial output
- 4:1 multiplex ADC outputs (6:1) in current test chip



Drain Current Digitizer – DCD

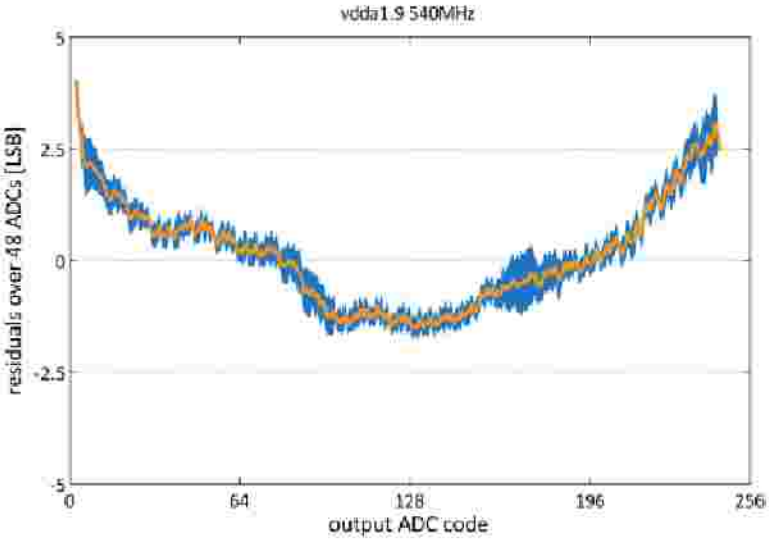
- DCD2: 72 ch. test chip
- 0.18 µm technology
- regulated cascode
- current memory cells
- two 8-bit algorithmic ADCs
- different test channels with parameter variations
- 6:1 multiplexed LVDS outputs
- bump bond IOs + wire bonds for testing

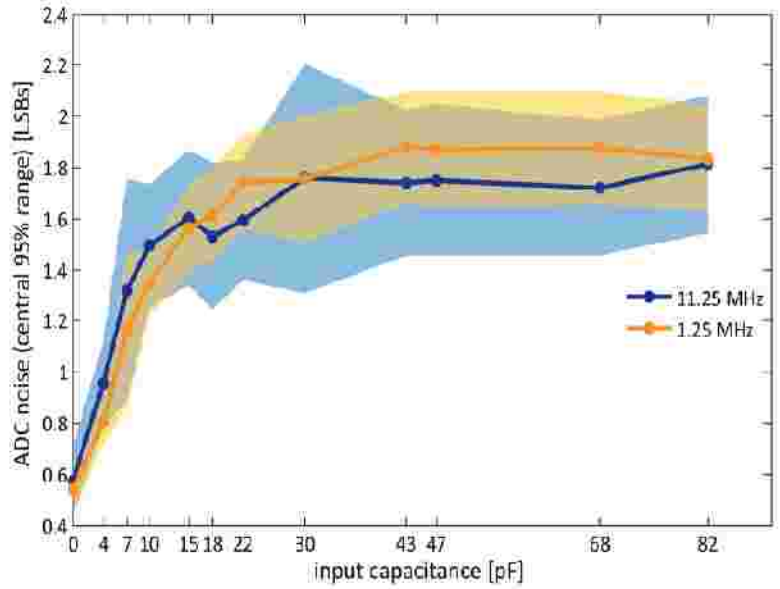


DCD2 – Measurements

- linearity (@ 12.5 MHz sample rate)
  - max INL: 4 LSB
  - max DNL: 1 LSB

- noise (including reg. cascode)
  - 0.6 – 1 LSB (w/o cap. input load)
  - < 2 LSB with up to 82 pF load





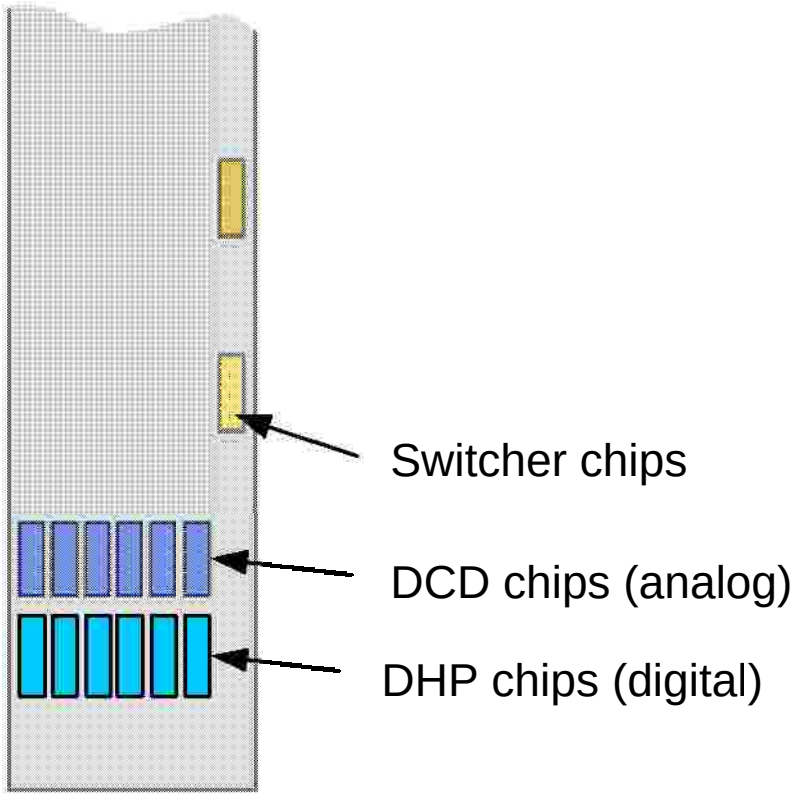
DCD2 – Measurements (contd.)

- input range: [0..24µA] (I_{SIG_MIP} ~12 µA @ 450 µm, 1.3 µA @ 50 µm)
- LSB: 100 nA (higher than designed à increased bias for 500 MHz operation)
- gain: 10 ± 0.1 LSB / µA
- noise: < 2 LSB @ 60 pF input capacitance
- power consumption: 6 mW/channel

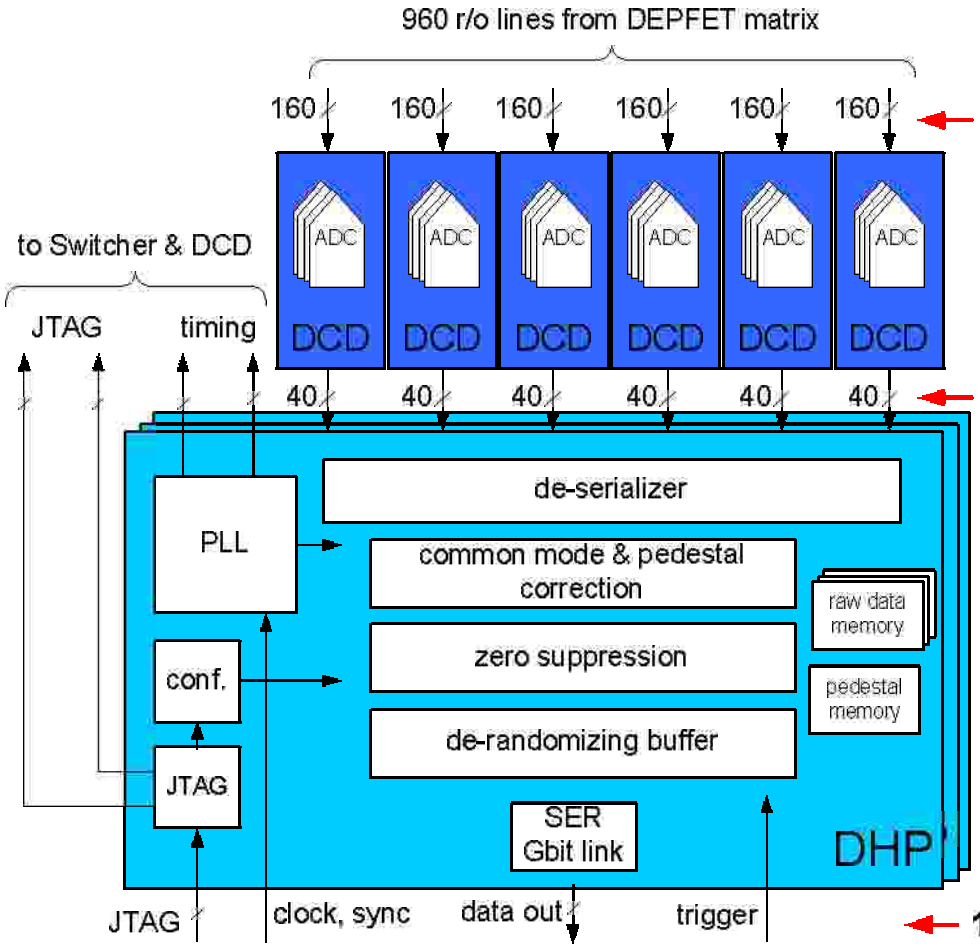
- DCD fully operational @ 600 MHz clock speed (12.5 MHz sampling frequency)
- adjust input range to dynamic signal range from thin detectors

- to do: dynamic tests (settling time, bandwidth ...), radiation tests

Data Handling Processor – DHP



DHP – Signal Rates & Data Flow



12.8 MHz line freq. (sample rate)

DCD chips:
- 8 bit ADC per input channel
- 4 channels per output

96 Gbit/sec (410 MHz output data x 240 lines)

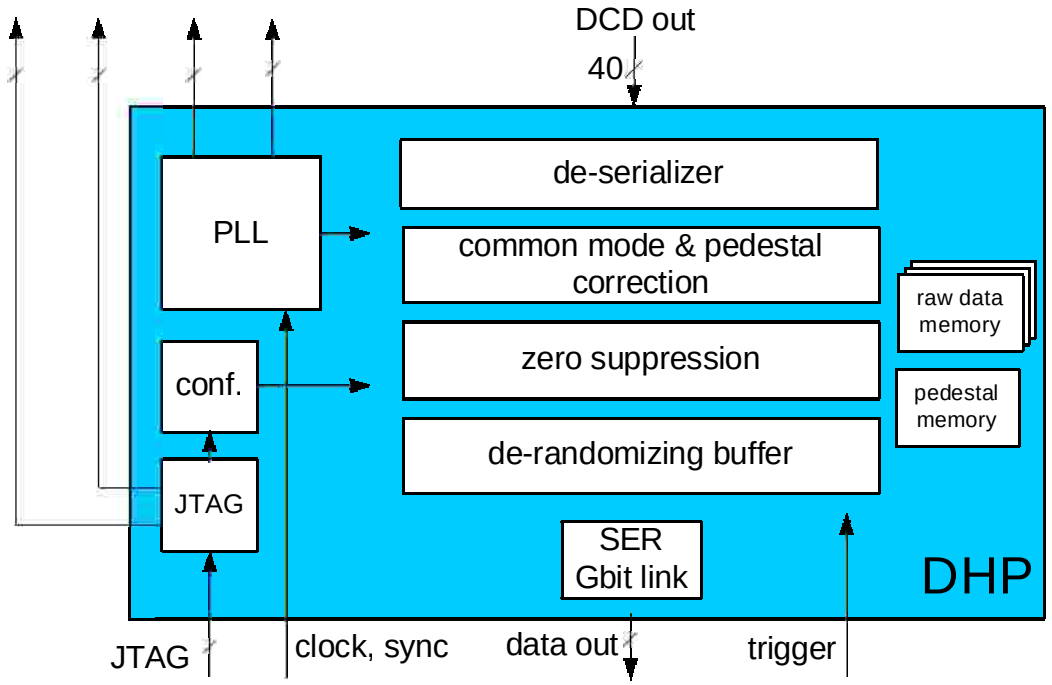
DHP chips (one per DCD):
- raw data correction
- zero supression → 18 Gbit/sec
- trigger r/o→ 1.8 Gbit/sec

1.8 Gbit/sec

Assumptions (à extended specs.)
- 10µs r/o time (à 20 µs)
- 128 switcher channels (à 256)
- 10 kHz trigger (à 30 kHz or more)
- 3-4% occupancy

Data Handling Processor – DHP

- receive & de-serialize ADC data from the DCD
- raw data correction
  - pedestal subtraction à correct for fixed offset per individual pixel
  - common mode correction à time dependent offset for all simultaneously sampled pixels (quad-rows)
- data reduction
  - zero-suppression
  - trigger coincidence
- module control functionality
  - PLL
  - DCD / Switcher timing
  - slow control (JTAG)
- 90 nm tech.
- 6 chips per half module



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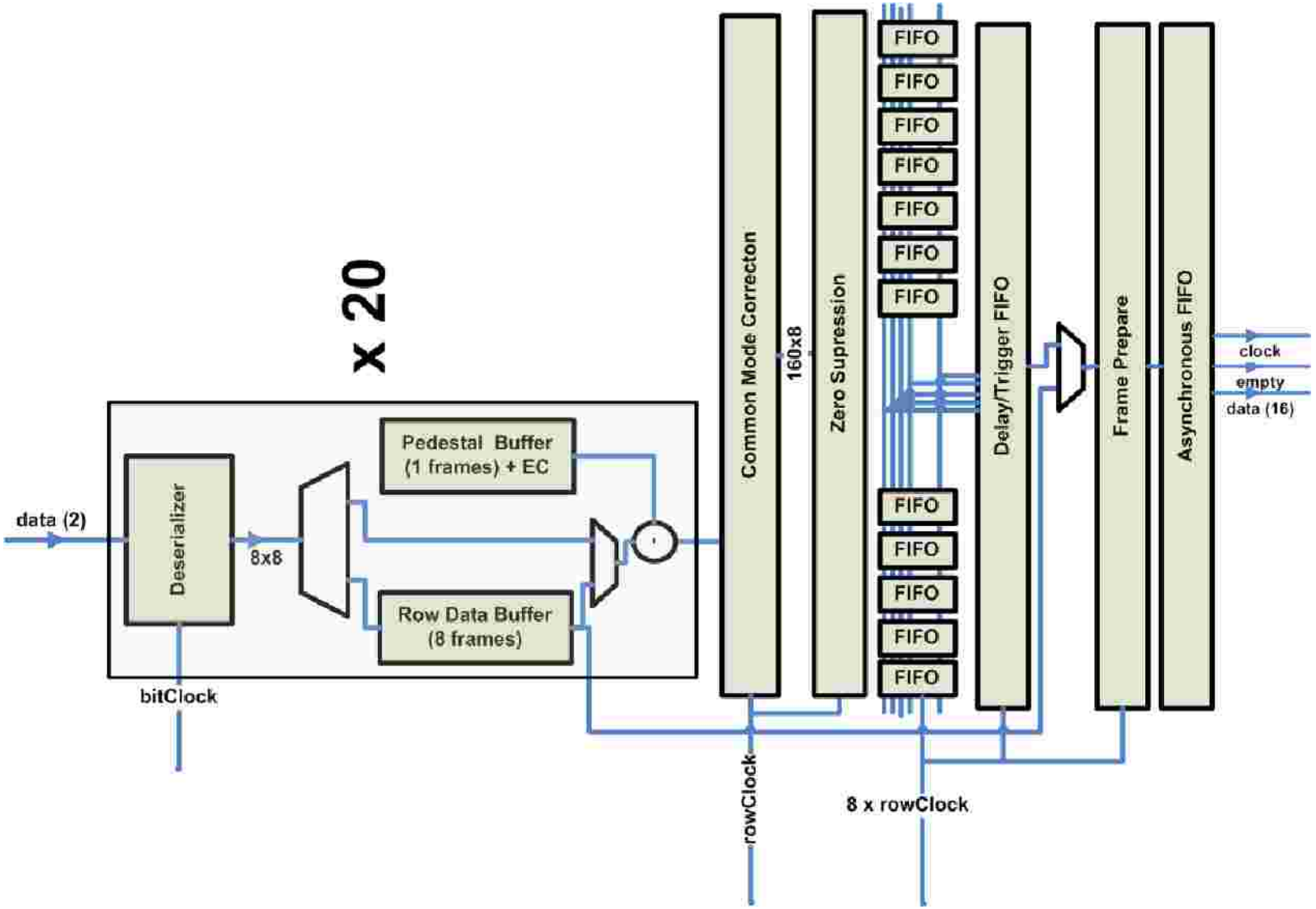
DHP Data Processing



Conclusion

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- DEPFET collaboration going to develop a pixel vertex detector for Belle 2
- Many design aspects make use of the ILC driven R&D
  - sensor development: thin sensor, 'all-silicon module'
  - chip development
- Prototypes of the Switcher chips designed and successfully tested, new development for higher output swing are under development
- DCD2 chip (test chip) close to final performance
- Design of the digital chip (DHP) just started

see talk by Carlos Lacasta on Friday afternoon for more details on the DEPFET sensor design & performance

Thank you!

backup

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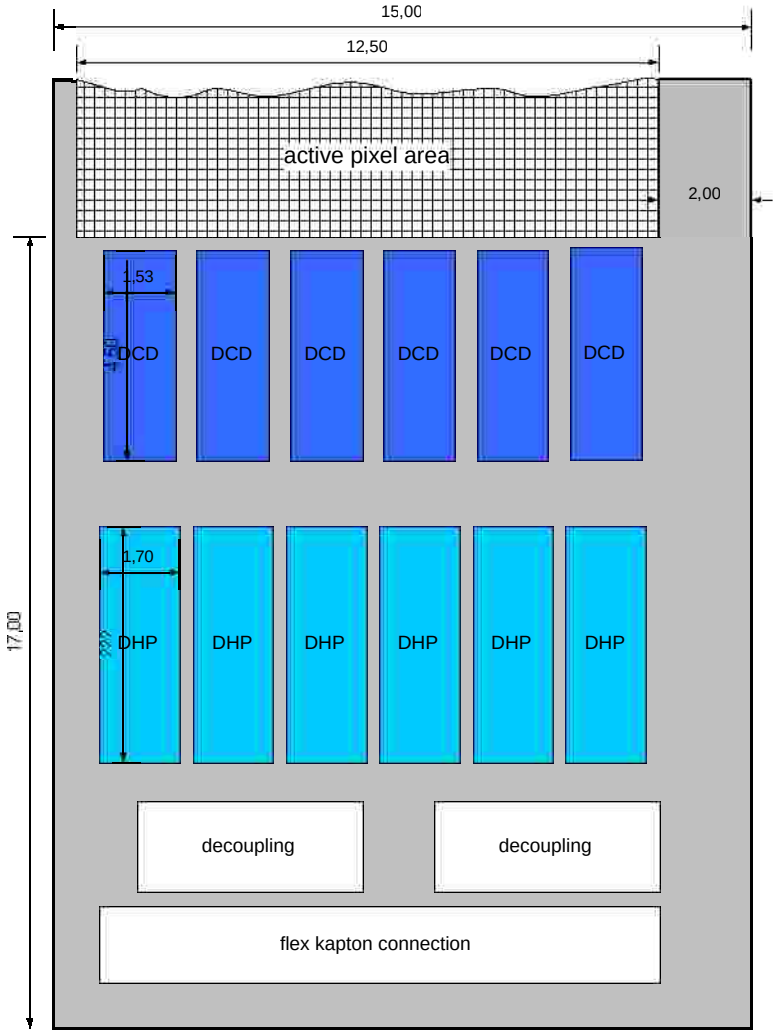
End of Module Layout



DCD

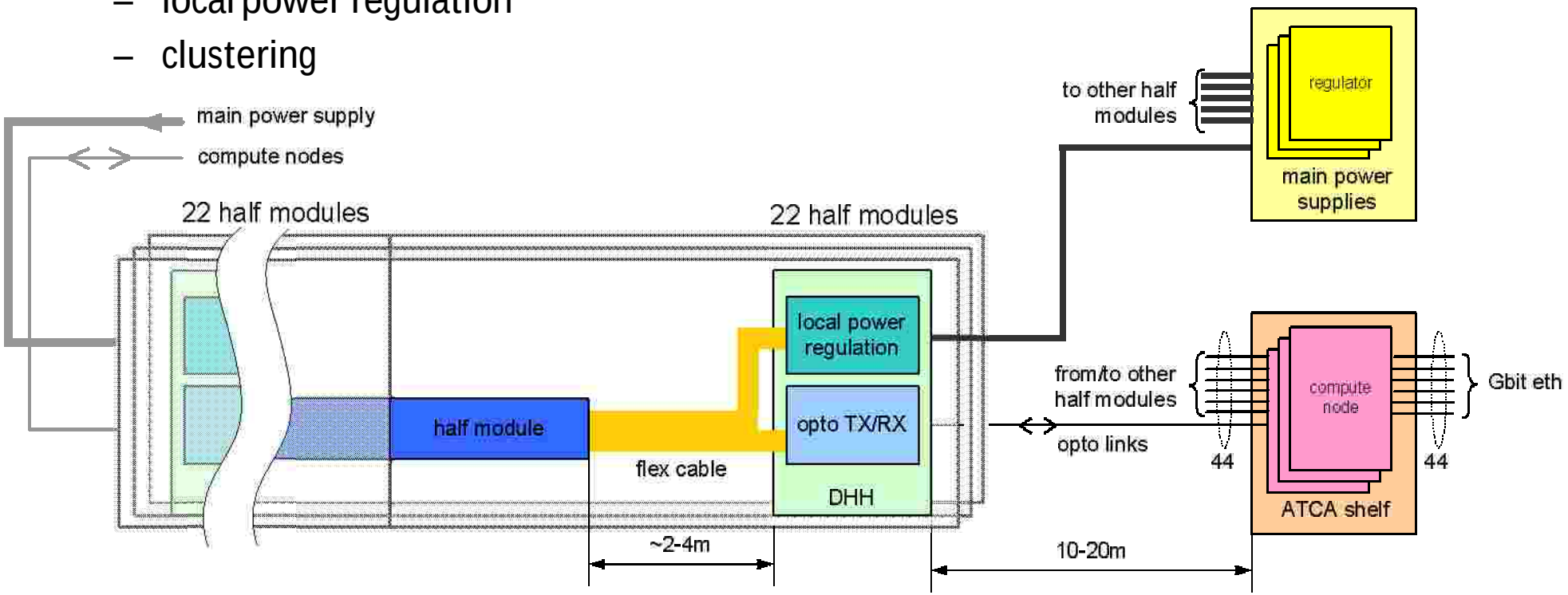
- 150 µm x 150 µm cells
- 6 chips, 1.5 x 4.7 mm
- Input: 16 rows, 10 columns
- Output: 4 rows, 10 columns

DHP

- 200 µm bump bond pitch
- 6 chips
- 1.7 x ??? mm
- One 1Gbit link per DHP
  à 6 Gbit per module
- Need to change input layout:
  - 5 rows, 8 columns

DEPFET PXD – Backend Electronic

- individual r/o for 44 half-modules
- intermediate board (data handling hybrid, DHH) between module and rack electronic (ATCA shelf with 'compute node' cards)
  - opto links
  - local power regulation
  - clustering



Switcher 4 – Implementation

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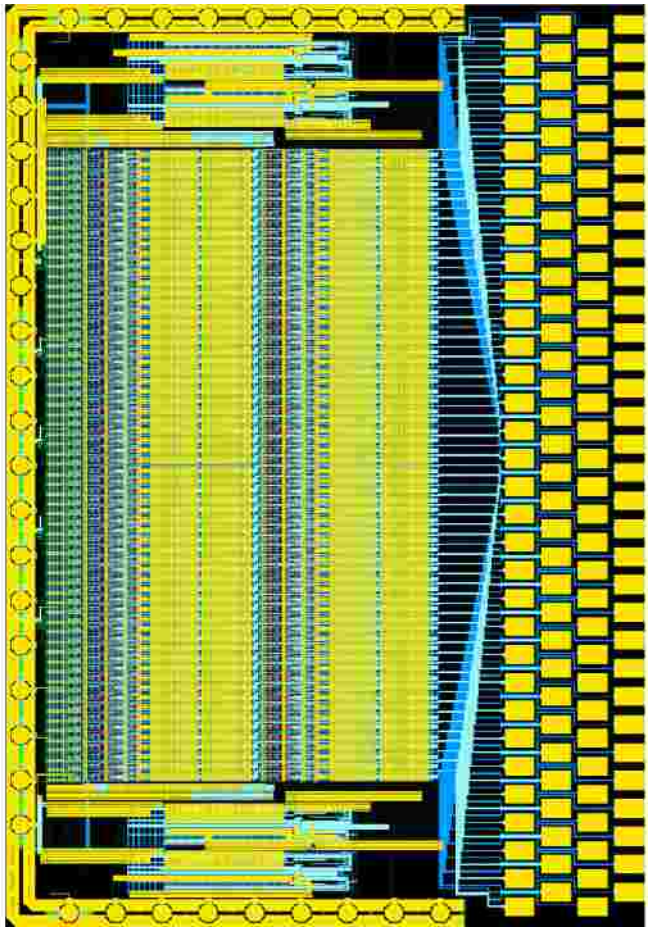
- 0.35 HV technology
- radiation tolerant
- 64 channels (x2, clear & gate)

pro:

- Possible operation up to 50 V (30V tested)
- gate and clear switches on one chip

con

- not as fast as SW3
- moderate DC power consumption (0.4mW/channel)



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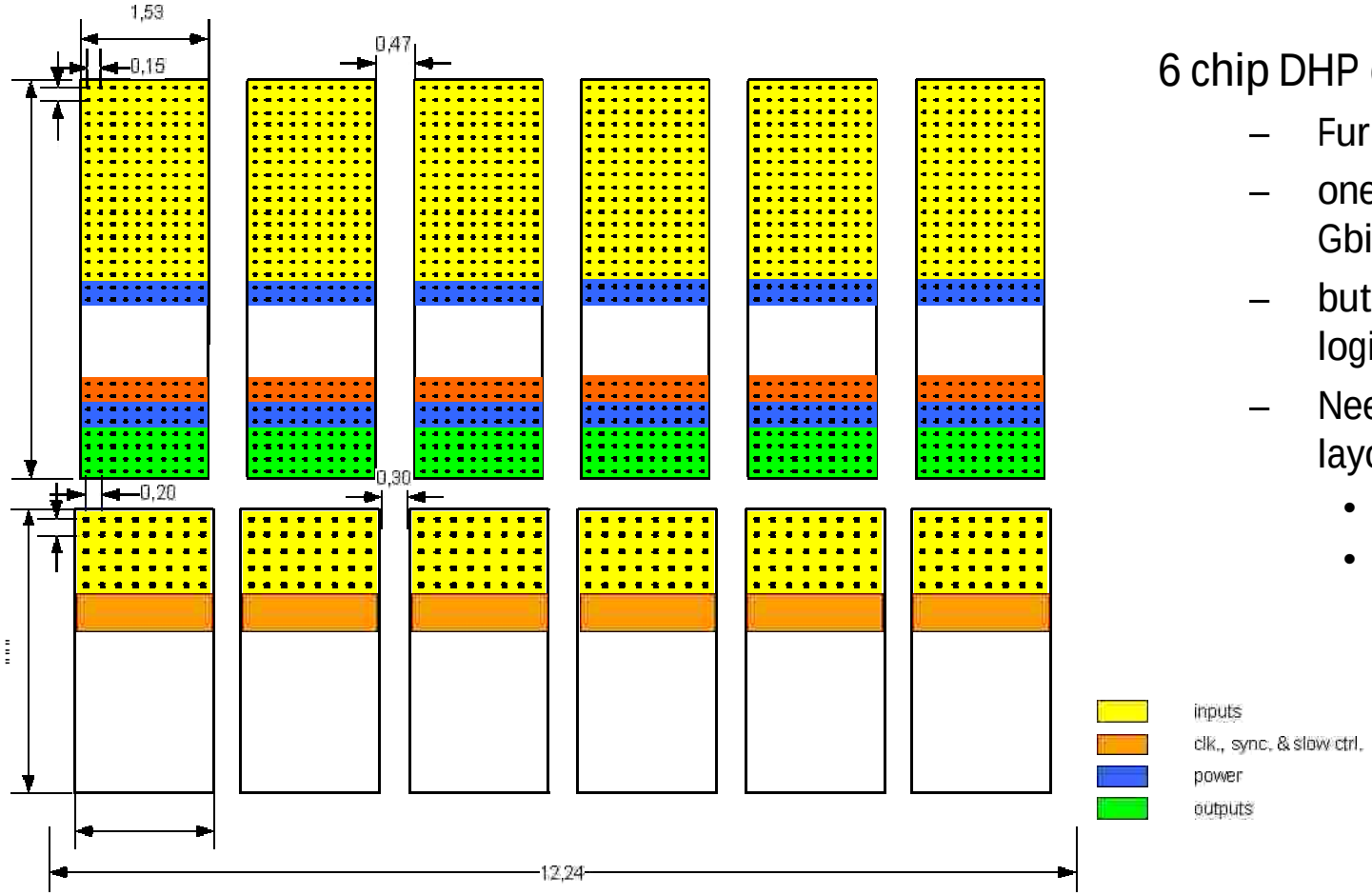
DCD + DHP footprints



6 chip DHP option

- Further reduced costs
- one Gbit link per chip @ 6 Gbit r/o per module
- but: even more redundant logic
- Need to change input pad layout
  - DCD: 4 x 10 @ 150µ
  - DHP: 5 x 8 @ 200µ

SuperKEKB timing

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- SuperKEKB RF frequency f0 = 508 MHz (508.89 MHz precisely)
- Number of slots per cycle: 5120
- Circulation time: 10.061 µs
- System clock f0/12 = 42.3 MHz (or f0/4, f0/8, f0/16, f0/256)
- Abort gap: 200 ns (~100 bunches)
- Clock for abort gap available (frame clock)

- DEPFET read-out synchronous with beam circulation (128 rows):
  row clock = 508 MHz / (5120/128) = 508 MHz / 40 = 12.7 MHz
- Use f0/8 and divide by 5 (DHH?)