A CMOS Front-End for SiPM devices aimed to TOF applications with adjustable threshold and high dynamical range

Davide Badoni[(a)] (davide.badoni@roma2.infn.it), **Francesco Gonnella**[(a,b)](francesco.gonnella@roma2.infn.it),
Roberto Messi[(a,b)](roberto.messi@roma2.infn.it), **Dario Moricciani**[(a)] (dario.moricciani@roma2.infn.it), **Flavio Archilli**[(a,b)] (flavio.archilli@roma2.infn.it),
Lorenzo Iafolla[(a,b)] (lorenzo.iafolla@lnf.infn.it)

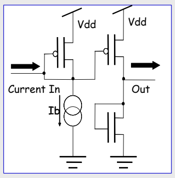
(a) "Roma Tor Vergata" Section I.N.F.N.
(b) Physics Department University "Tor Vergata"

Abstract

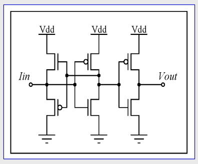
In recent works we presented the results of the characterization and the study of performance of several Silicon Photomultipliers delivered from MEPHI and we proposed an electrical model of the SiPM to be used in analog simulations for the VLSI design of the pilot chip with 0.35 μm technology produced. The results of the simulations was also presented. In this work we present the results of several test performed on the SiPM connected to the pilot chip. We also describe the prototype board with a microcontroller designed to adjust the parameters of the chip and to provide an adjustable and temperature controlled power supply to the SiPM. The results of the tests obtained allow us to refine the circuits design for the next chip. This chip has been developed inside the ALTCRISS and KLOE collaboration.

The chip

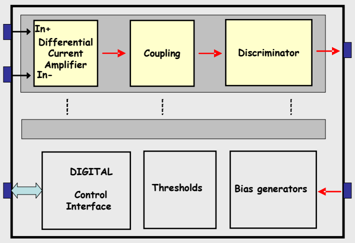
The chip is made of 8 channels for 8 SiPM. Each channel consists basically of one amplifier and one discriminator. The discriminators thresholds are adjustable for each channel. The main goals of this pilot prototype chip are the fast response of the discriminators, reduced jitter and adjustable thresholds providing a large dynamical range. In order to obtain these performances we have chosen a current amplifier approach.



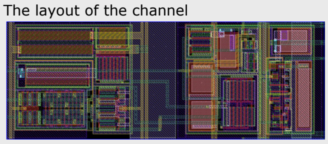
The figure on the left shows the simplified schematic of one of the two parts of the *fully balanced* input stage. Another identical side is implemented to obtain a *fully differential* functionality with a feedback. This improves the bandwidth and the input impedance of a factor of two. On the right side the simplified schematic of the fast current amplifier is shown.

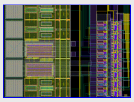


The figure on the bottom left shows the general architecture of the chip, putting in evidence the block diagram of a single channel.



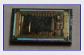
The layout of the channel





The layout of the eight channels and a portion of padframe. The technology used is AMS 0.35 μm, four metals, double polysilicon.

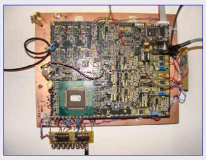
The chip →



A more detailed description of the chip is reported in (1).

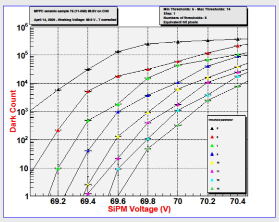
Chip-SiPM test Board

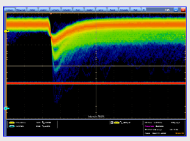
A dedicated board has been developed for testing the Chip-SiPM functionality. The board provides the adjustable biasing and thresholds for the chip and all the power supply needed. A circuit based on MAX1932 from MAXIM™ is onboard. It provides 8 independently adjustable power supplies for the SiPM devices. All parameters can be set via a standard RS232 PC port handled by a ATMEL™ 89C5132 microcontroller with a custom-firmware.
An AD 590 sensor is used to monitor the temperature in the SiPMs area.



Dark current measurements

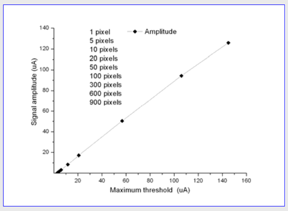
Dark current measurements have been performed using the test board and a 1x1 mm Hamamatsu™ SiPM. In the bottom right figure, we reported the dark-rate of the SiPM (connected to one chip channel) varying the power supply voltage. Different values of the threshold were used as a parameter. The working voltage of the SiPM was corrected (according to Hamamatsu datasheet) to keep the SiPM gain constant as the temperature changed. The voltage correction has been taken into account during the offline analysis.

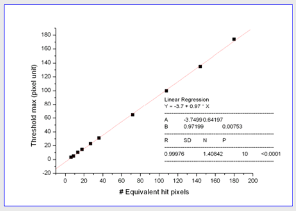




We built an analog output in each channel of the chip, for debugging purposes. During the dark current studies, we monitored the analog analog output through a DPO. The structure of 1, 2 and 3 hit pixel is clearly visible in the screenshot shown on the left.

Measurement vs. Simulation

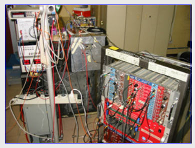


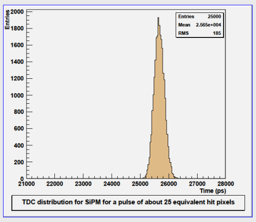


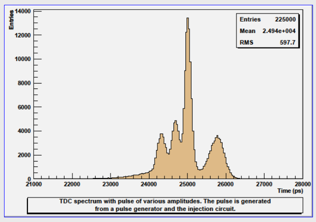
We investigated the dynamical range and linearity of the chip. We made a simulation by mean of a model of the 3x3 mm^2 SiPM from MEPHI (Moscow Engineering and Physics Institute) developed in a our previous work (2).
We compared the results of the simulations (on the left side) with the real measurement performed on the chip (on the right side).

Timing

We performed several measurement in order to check the timing capability of the device.
We made use of the same injection circuit to connect the pulse generator to the input channels of the chip. We measured the distribution of the arrival times of many pulses of fixed amplitude and RMS (jitter). Then we repeated the measure for various values of the pulse amplitude. All the timing measures were obtained with a V775 VME module by CAEN (35 ps per channel) in common stop mode.



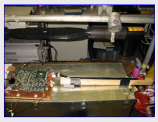




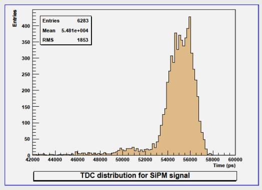
The figure above on the left shows the time distribution obtained with a fixed pulse amplitude corresponding to about 27 equivalent hit pixels.
The figure above on the right shows the global spectrum obtained from the sum of the whole set of time measurements made with all the different amplitudes.

A cosmic ray test has also been performed using a 1x1mm Hamamatsu SiPM coupled with a small BC418 plastic scintillator.

We used a telescope made of two scintillators of the same type coupled with two PM. The signal coming form the PMs have been discriminated with a CFD in order to avoid the time-walk.



We made use of the same ACQ system. The resulting spectrum is shown on the bottom right plot.



Conclusions

We have designed, produced and tested the pilot chip of a CMOS frontend for SiPM devices.
Thanks to the encouraging results of the performed tests the developing of the second version of the chip is already in progress.
We plan to make several improvements: get a better time resolution refining both the amplifying and discriminating sections; make a chip that fits the input characteristics of a wide range of SiPM devices; provide the new version with a high performance analog output.

References

(1) **SiPM: Characterizations, modelling and VLSI front-end dedicated development.** D. Badoni, R. Messi, V. Bidoli, V. Capuano, M. Casolino, P. Picozza, and A. Popov.- ***IL NUOVO CIMENTO Vol. 30 C, N. 5 - April 2008***

(2) **Silicon photomultipliers: On ground characterizations and modelling for use in front-end electronics aimed to space-borne experiments.** Davide Badoni, Francesco Altamura, Alessandro Basili, Raffaele Bencardino, Vittorio Bidoli, Marco Casolino, Anna De Carli, Tom Froysland, Marcello Marchetti, Roberto Messi, Mauro Minori, Piergiorgio Picozza , Gaetano Salina, Arkady Galper, Mikhail Korotkov and Alexander Popov. ***Nuclear Instruments and Methods in Physics Research Section A, 2006 - A 572 (2007) 402–403***