Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

mpi halbleiterlabor

SiMPl - An avalanche diode array with bulk integrated quench resistors for single photon detection

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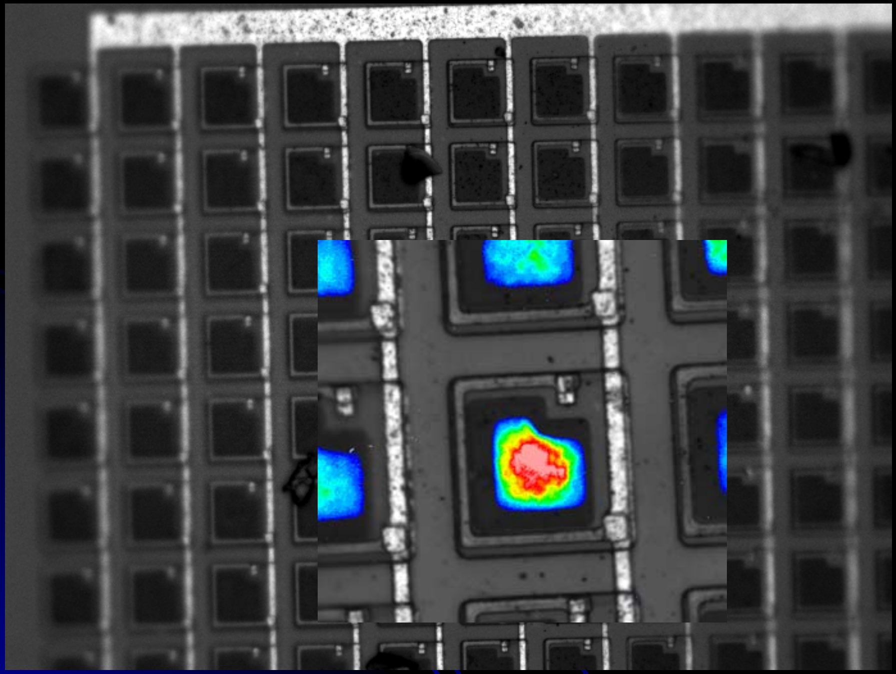
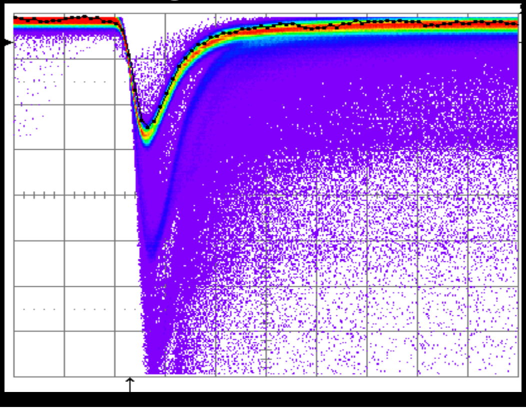
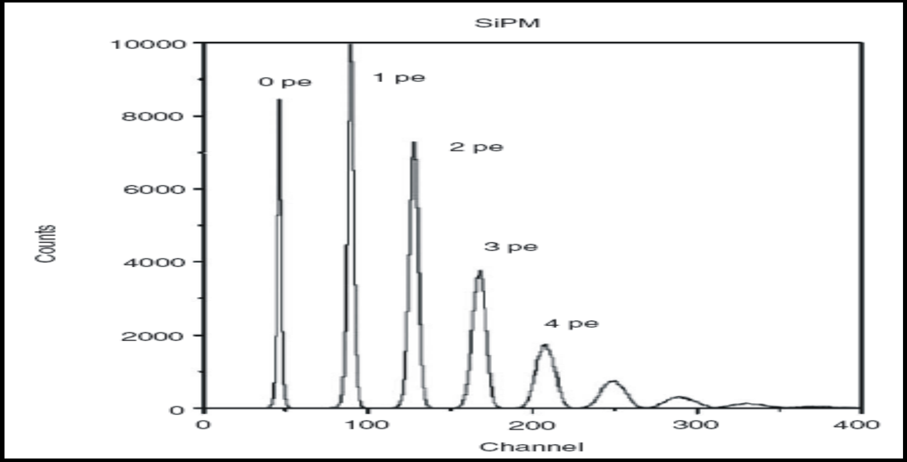
What is a Silicon Photomultiplier – SiPM ?

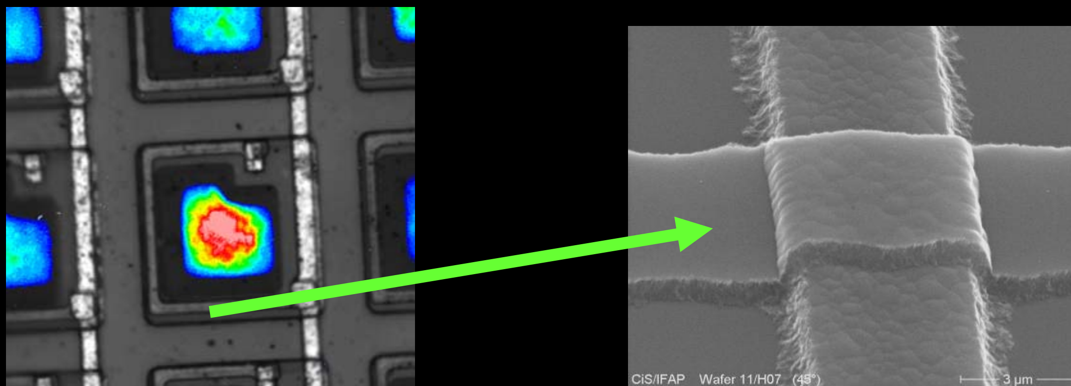
- An array of avalanche photodiodes
  - operated in Geiger mode → binary device
  - passive quenching by integrated resistor
  - read out in parallel → signal is sum of all fired cells





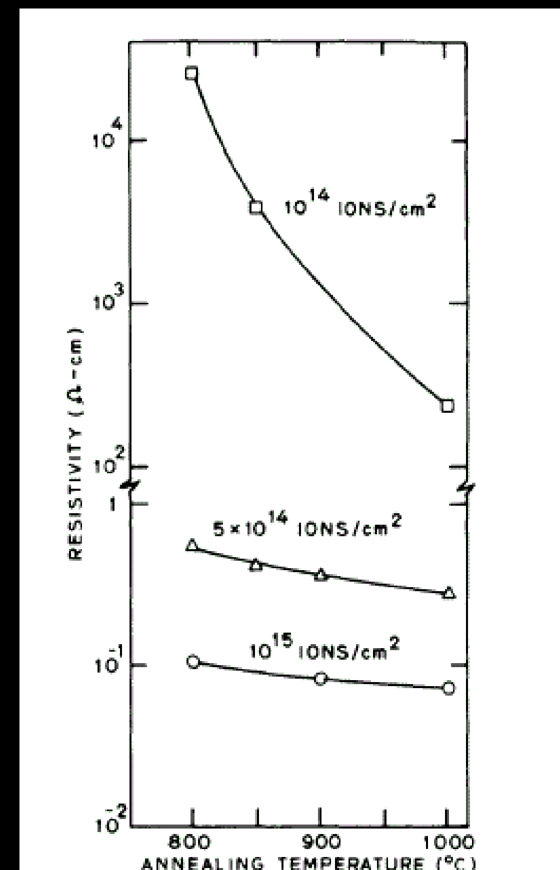


Polysilicon Quench Resistors



- Complex production step

- Critical resistance range
  influenced by: grain size, dopant segregation in grain boundaries, carrier trapping, barrier height
- Sheet resistance depends on:
  Deposition conditions, implantation dose, layer thickness, annealing temperature, preconditioning (cleaning steps before deposition)

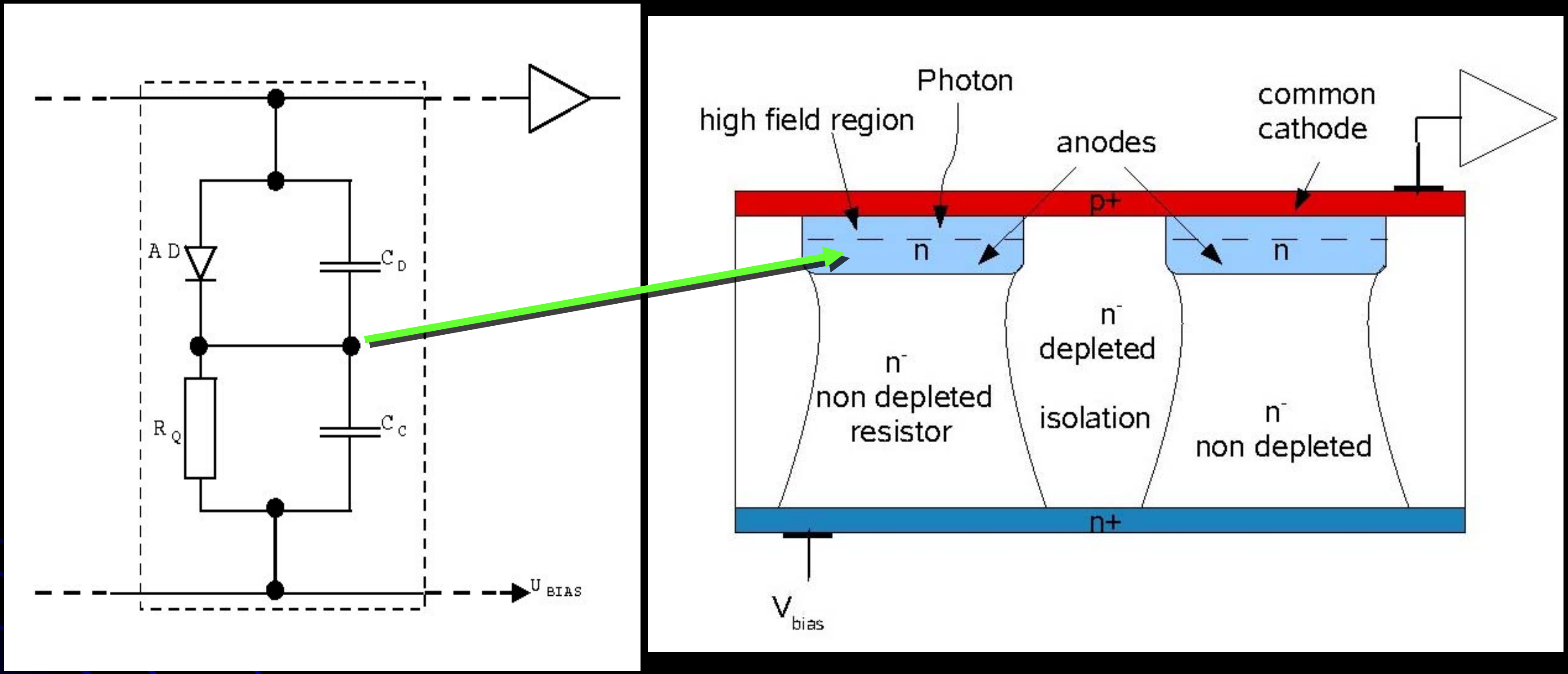


M. Mohammad et al.
'Dopant segragation in polycrystalline silicon',
J. Appl. Physics, Nov.,1980

Rather unreliable process step and an obstacle for light

SiMPl(e) approach

Components of a SIPM cell



Front side p$^+$ cathode and backside n$^+$ region are common for the entire array

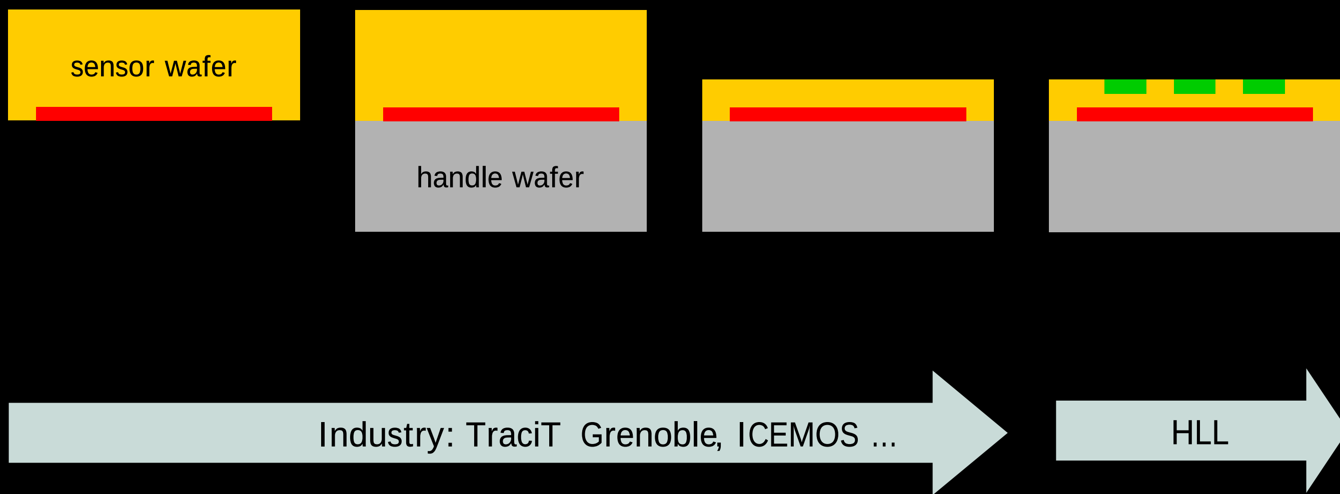
Anode region becomes an internal node within silicon

Bulk region beneath the anode acts as vertical resistor shielded by the anode from depletion

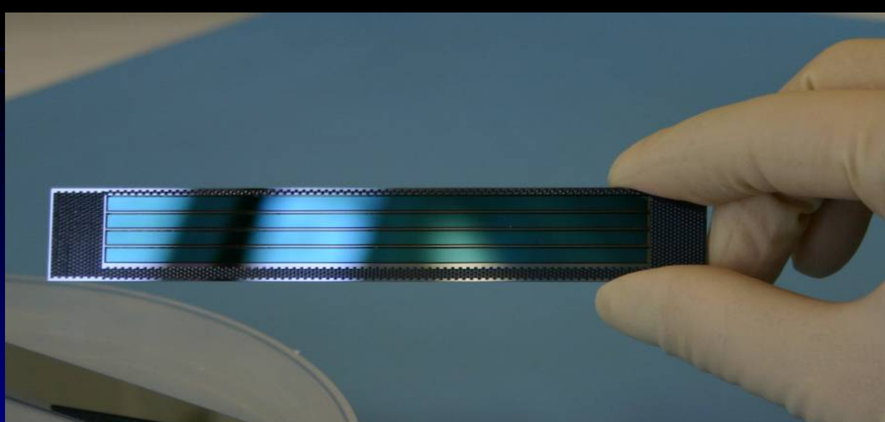
Gap regions are depleted and isolate the individual resistors

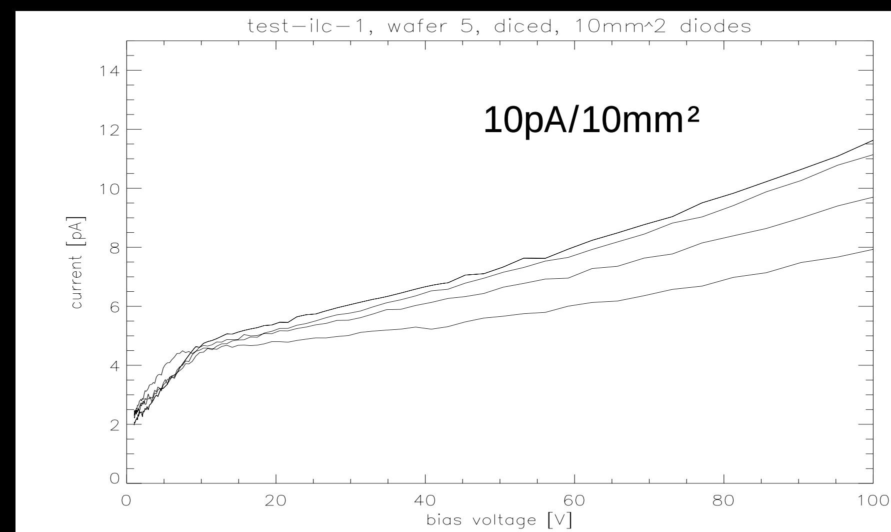
But resistor matching does not work with a wafer of usual thickness !

SOI wafers



sensor wafer
handle wafer
Industry: TraciT Grenoble, ICEMOS ...
HLL





test−ilc−1, wafer 5, diced, 10mm^2 diodes
10pA/10mm²
current [pA]
bias voltage [V]
0
2
4
6
8
10
12
14
20
40
60
80
100

Matching of resistor requirements with bulk geometry

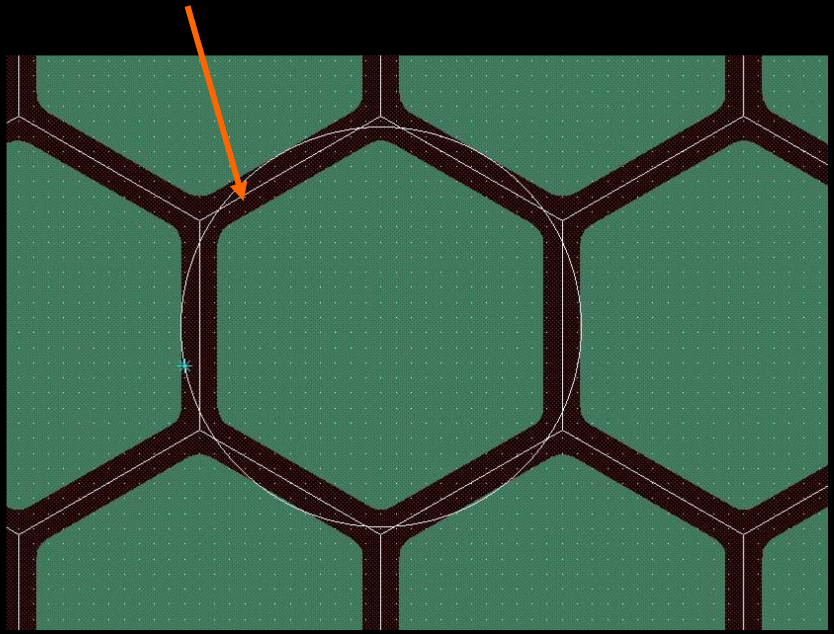
A simple resistor problem (bulk resistivity and geometry)

but ...

- carrier diffusion from top and bottom layer into the resistor bulk
- sideward depletion

➔Extended device simulations performed and showed promising results

cylindrical approximation of hexagons for quasi 3d simulation



Pros and Cons

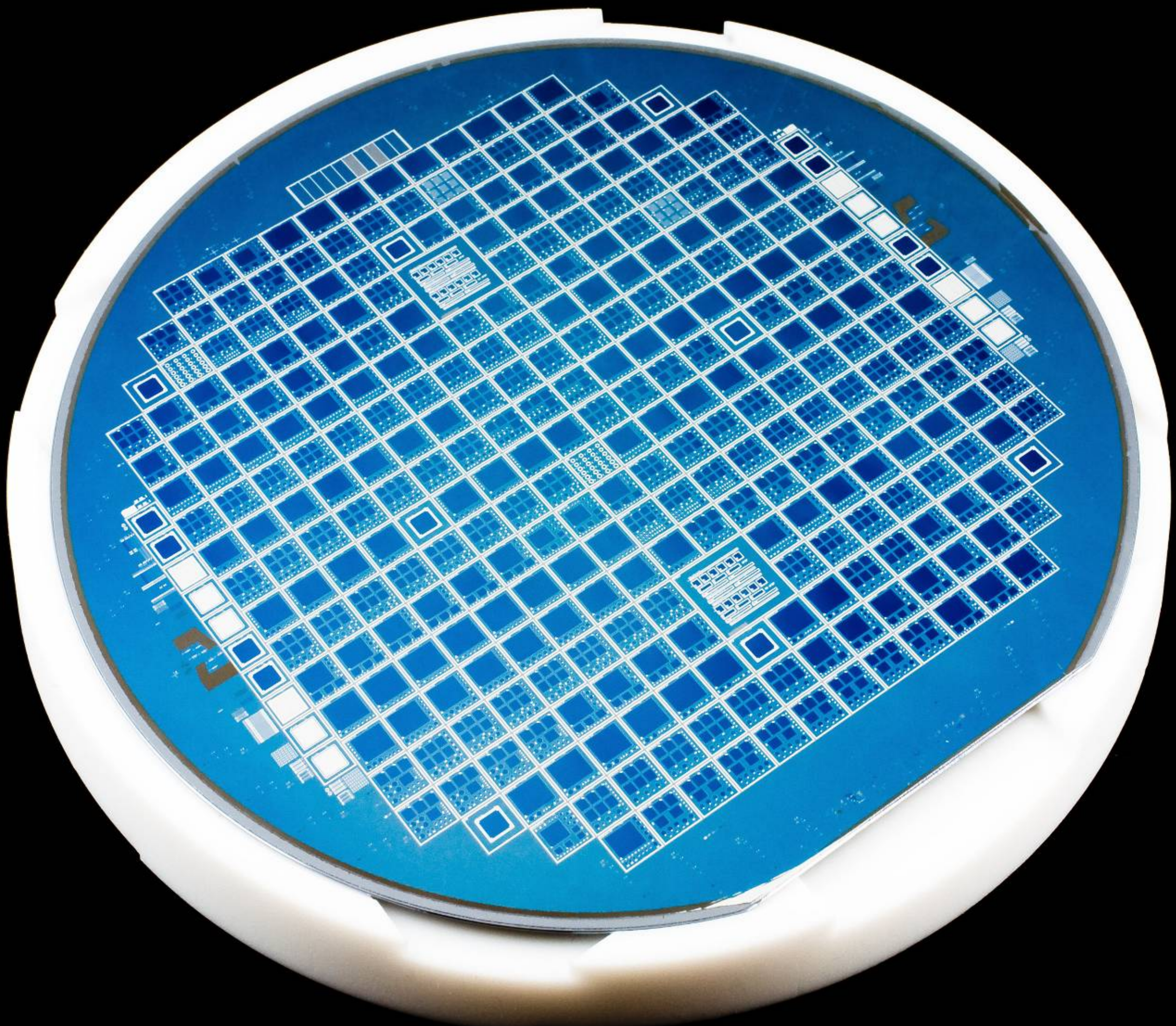
Advantages:

- no need of polysilicon
- free entrance window for light, no metal necessary within the array
- coarse lithographic level
- simple technology
- inherent diffusion barrier against minorities in the bulk -> less optical cross talk
- hopefully better radiation hardness

Drawbacks:

- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes
- significant changes of subpixel size requires change of material
- vertical ‘resistor‘ is a JFET -> parabolic IV -> longer recovery times

1st Production run

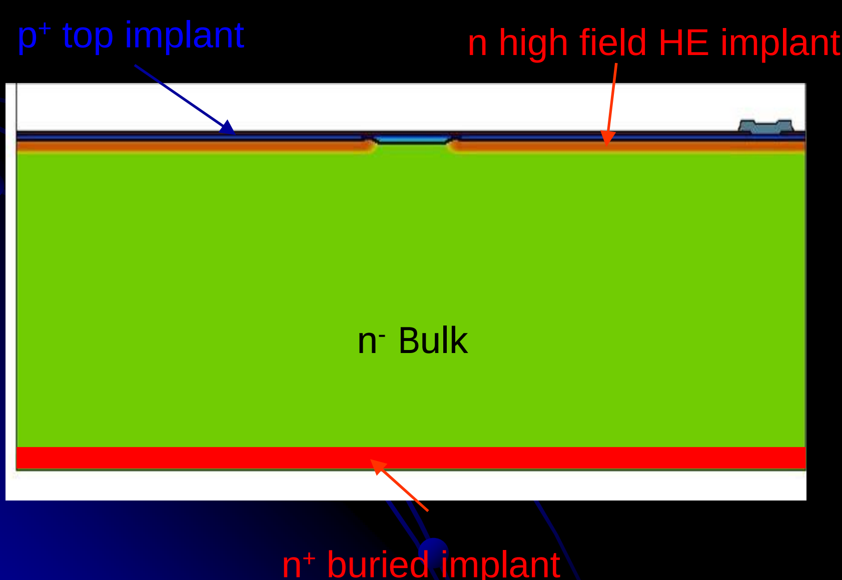


Proof of principle production

Simple technology

SOI material – 70µm top wafer
(wafers from TOPSIL, bonding at ICEMOS)

4 mask steps
- 2 implantations
- contacts
- metal

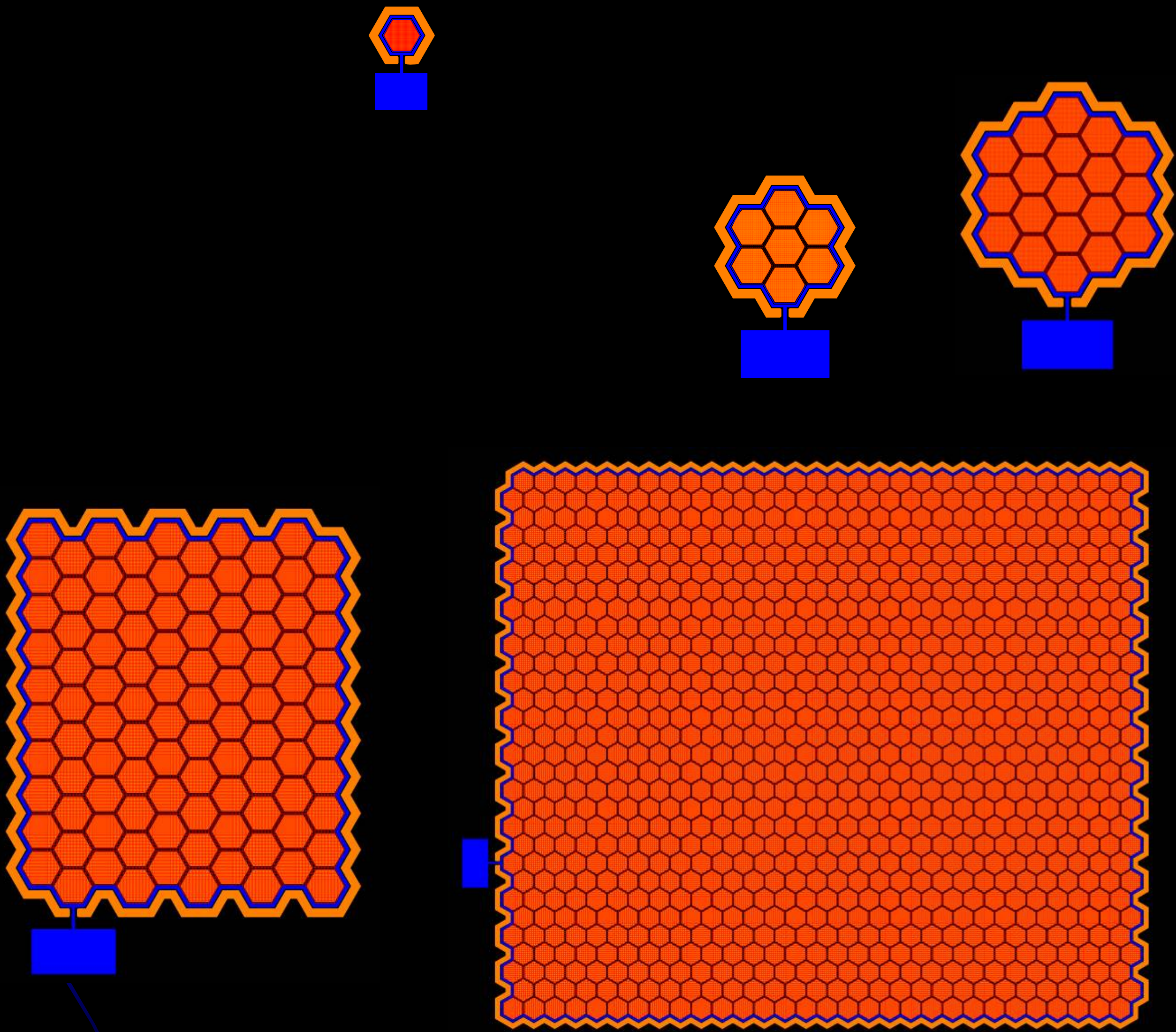


Hexagonal subpixels
120 different pitch – gap combinations

Free entrance window for light without obstacles

Design

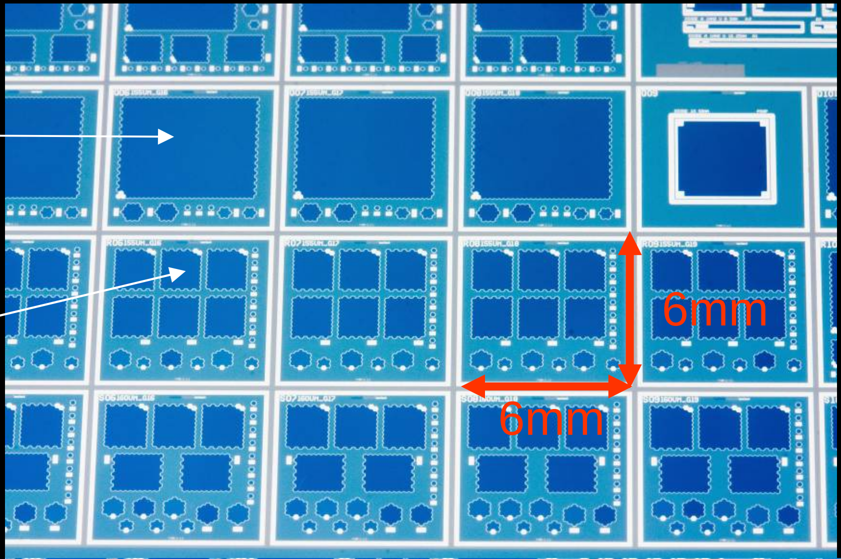
- single cells
- Arrays:
  - 9 cells
  - 19cells
  - 10x10
  - 30x30

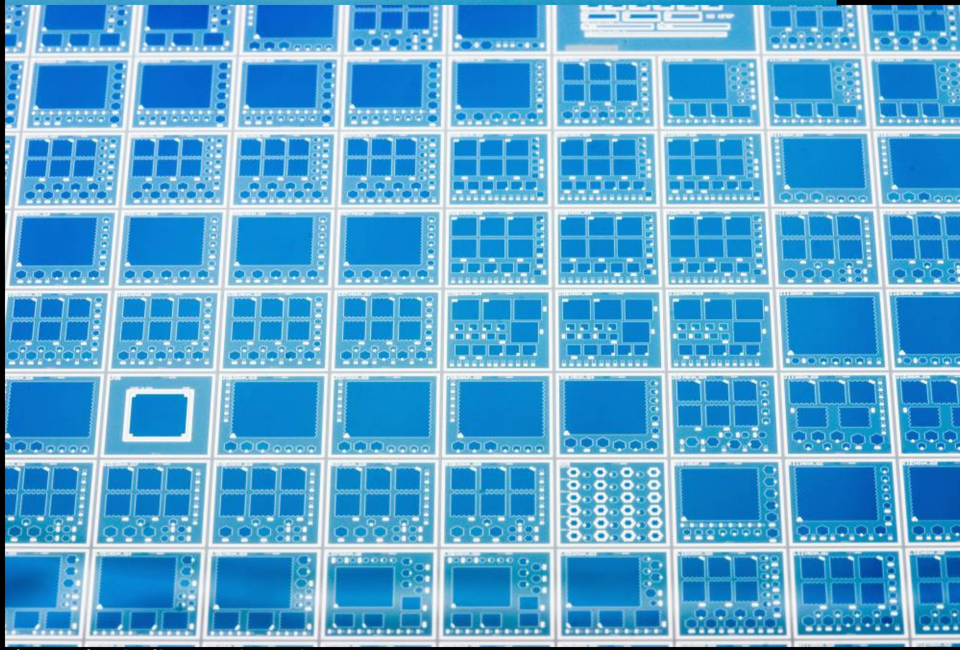


Production

30x30 arrays

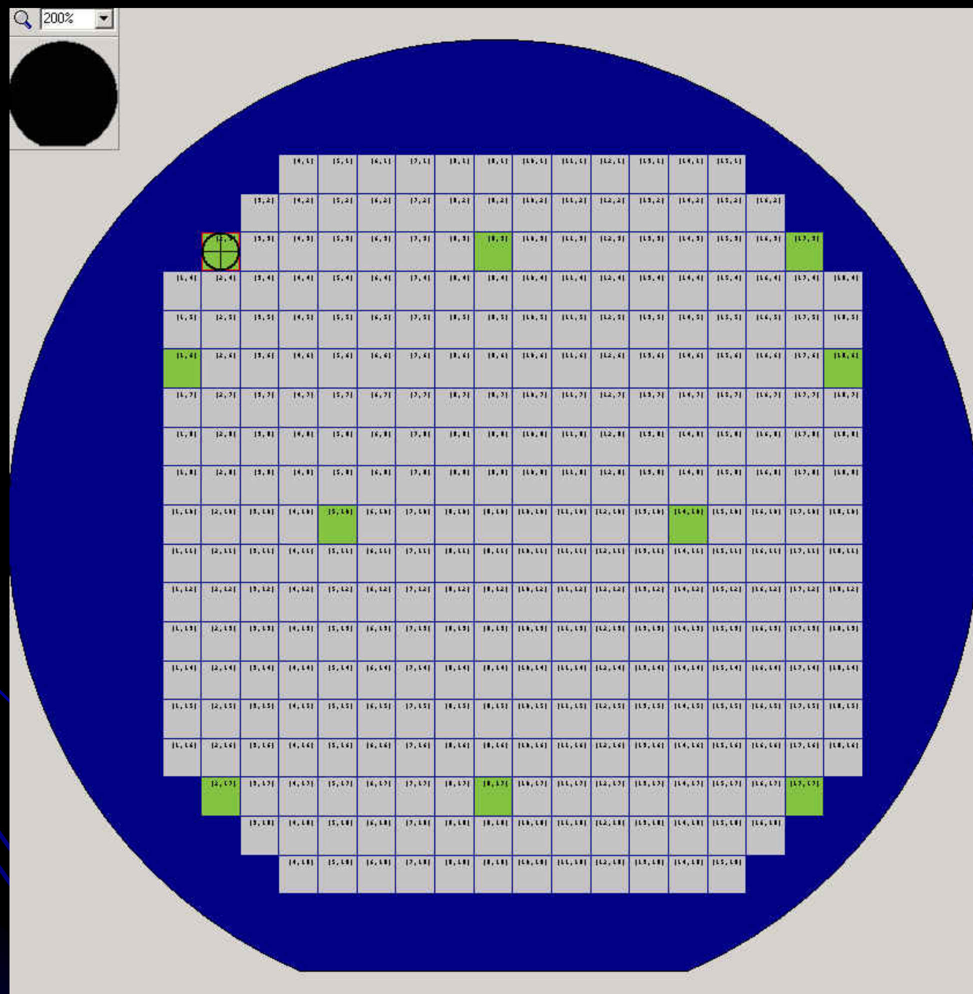
10x10 arrays





Bulk doping variation of the top wafers measured on 10 diodes*/wafer (CV)

(*test diodes without high energy implantation)



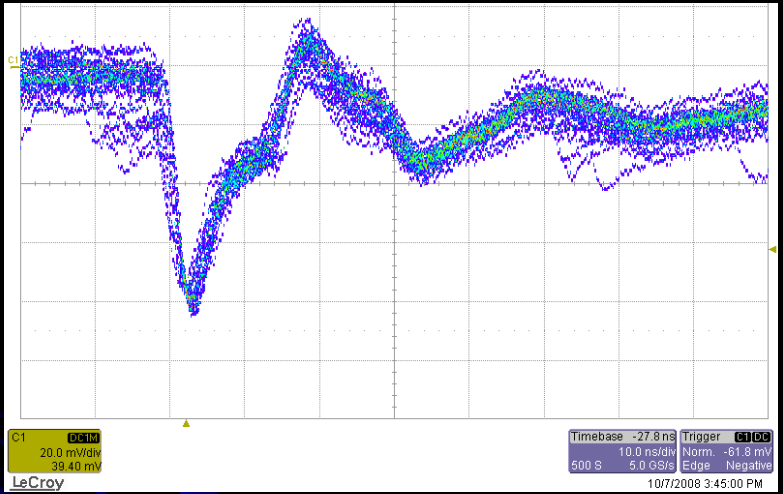
Bulk doping variation of the top wafers measured on 10 diodes*/wafer (CV)

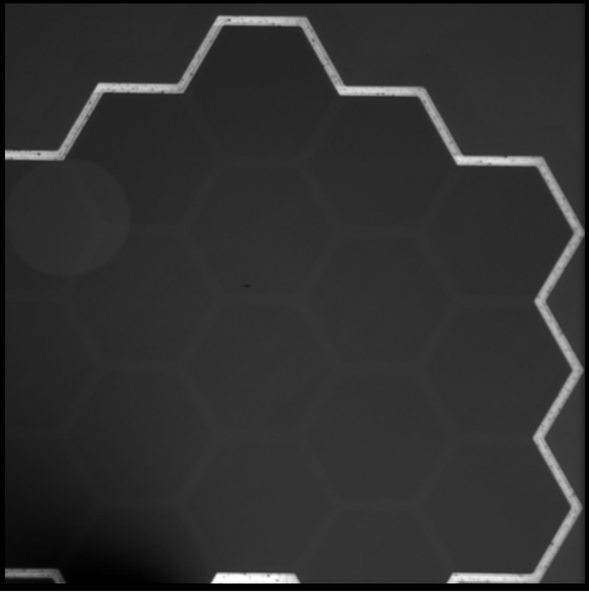
(*test diodes without high energy implantation)

Wafer	Mean (cm^{-3})	Stdev (cm^{-3})
#737	2.87e+12	3.8e+10
#749	2.87e+12	3.4e+10
#739	2.64e+12	5.7e+10
#752	2.64e+12	3.1e+10

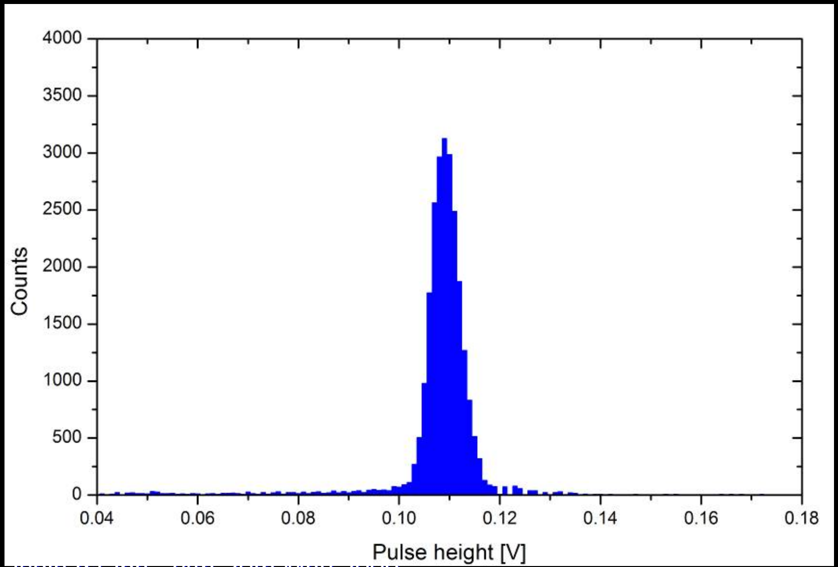
Proof of principle –
Signals → Quenching works

- 19cells , 3V overbias, RT, pitch 130µm, gap 14µm



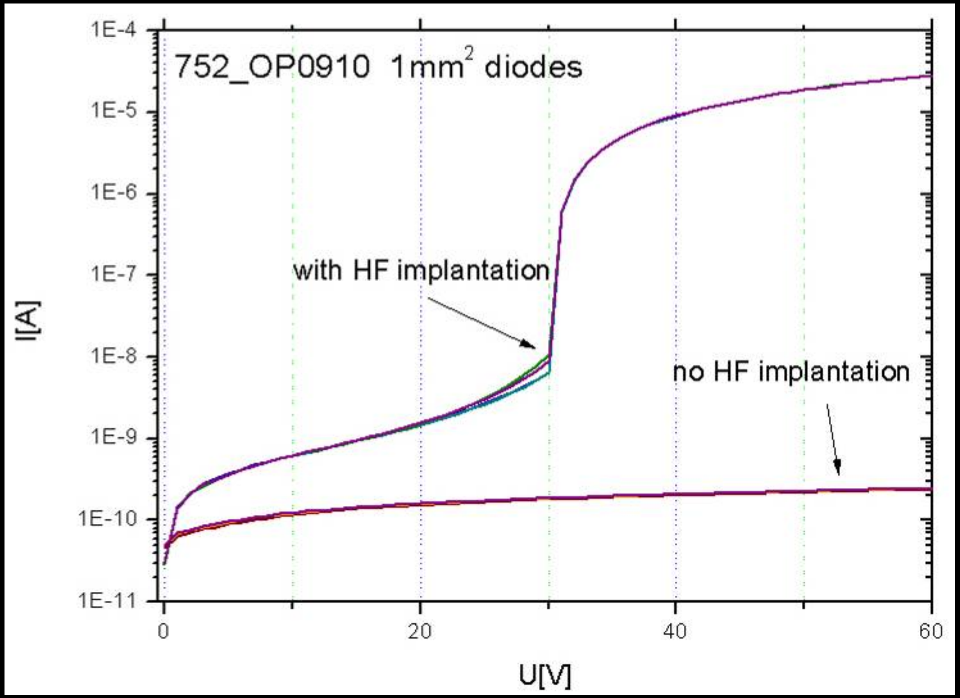


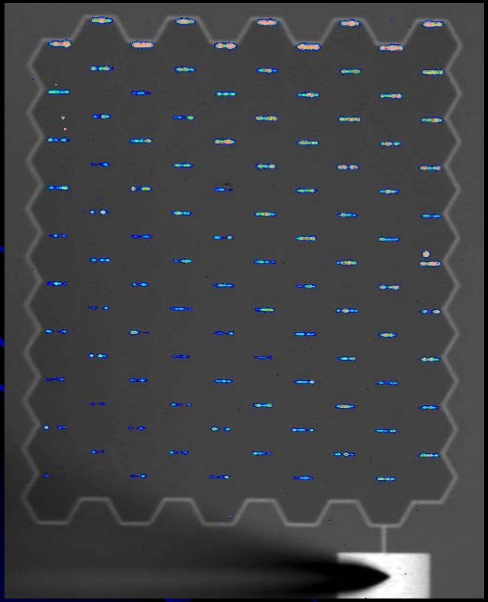
T = -46°C



1st production run - Still some problems

- High leakage current (dark rate) – not sufficient annealing of the high field implant
- Edge breakdown
  due to a wrong tilt angle of the high field implant



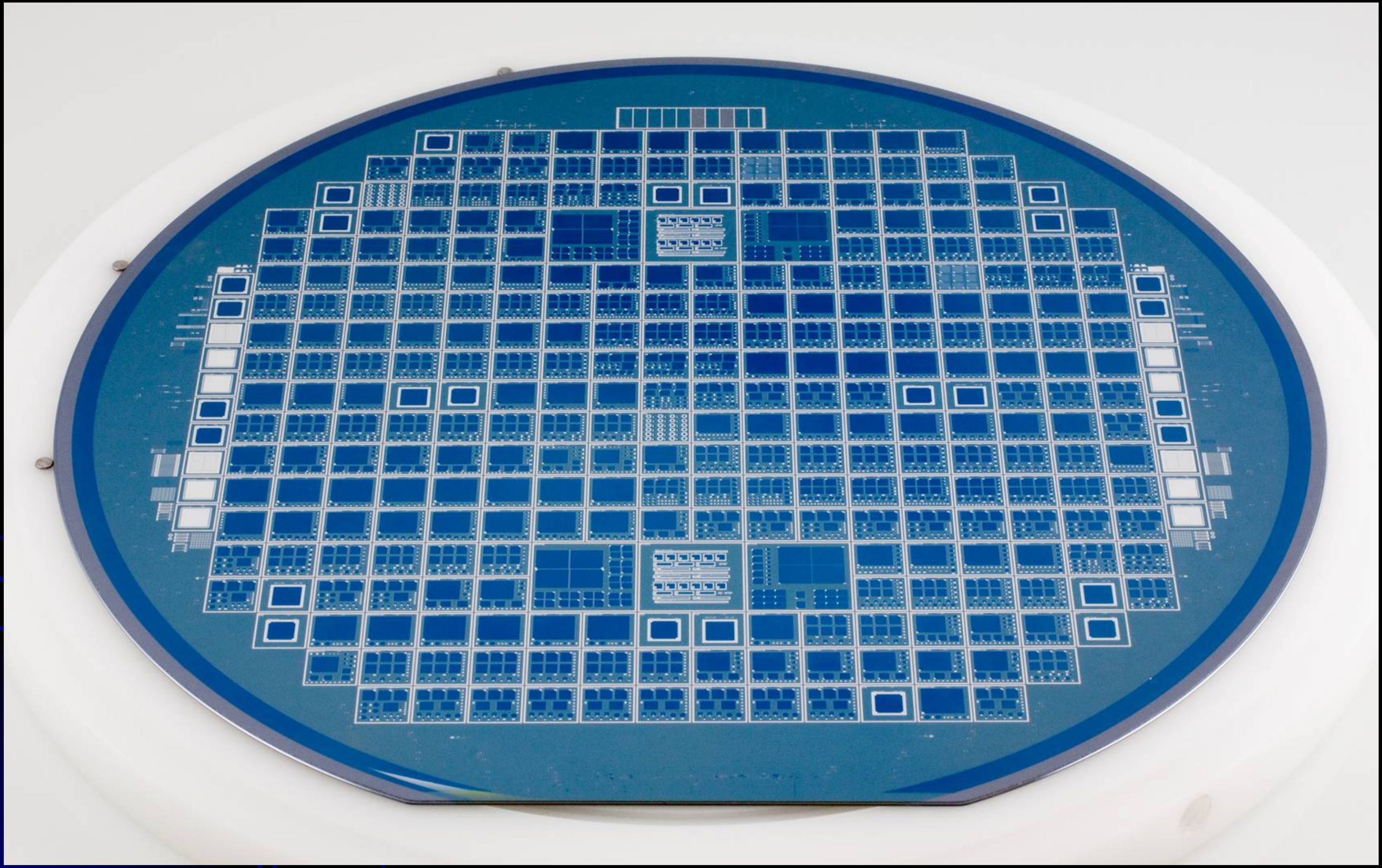


Thermal emission microscope picture

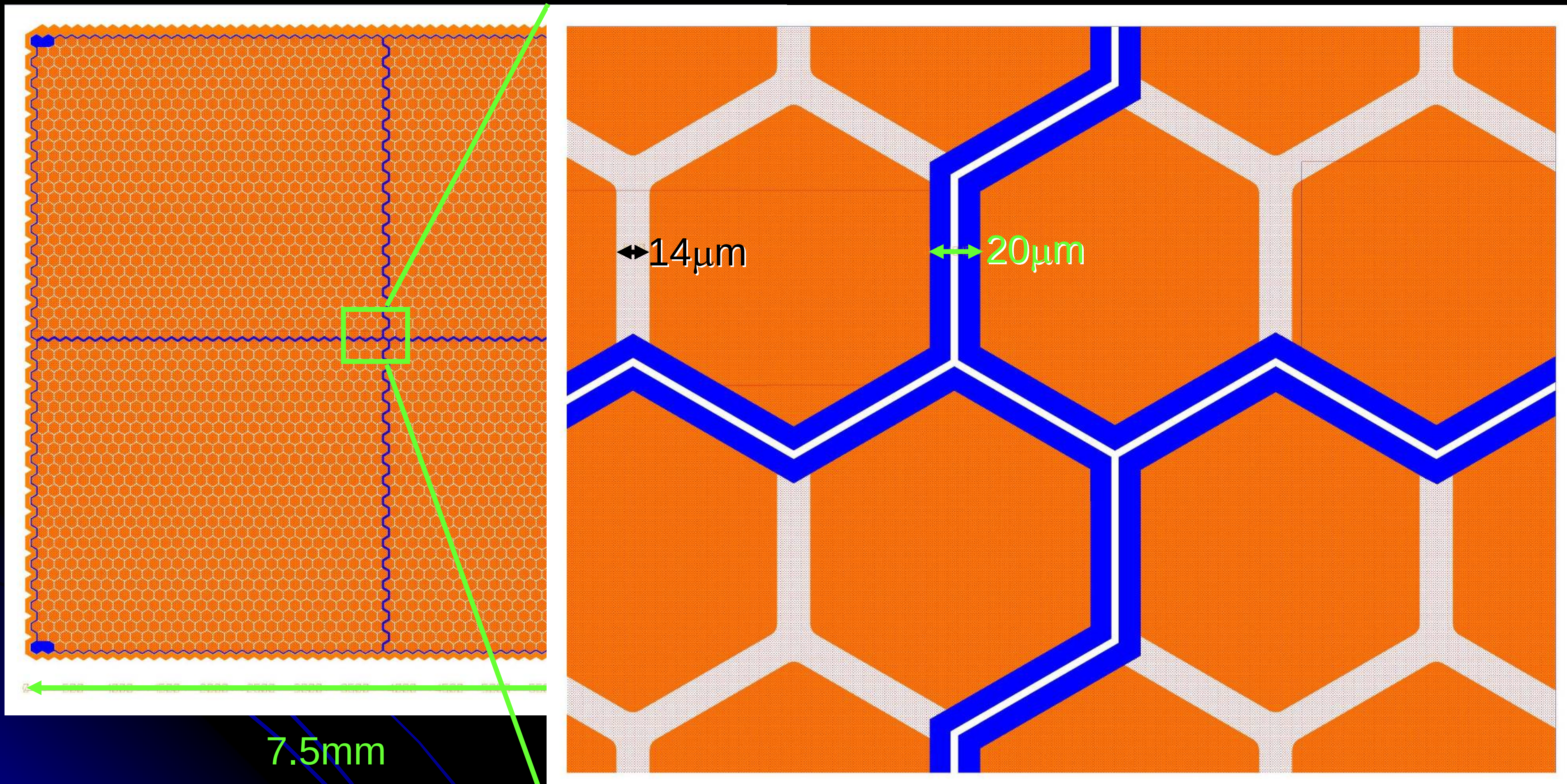
2^{nd} production run – Prototype production

- Goal:
  - Optimize technological parameters
  - Produce fully working device
- Production finished 10 days ago

2nd production run – Prototype production

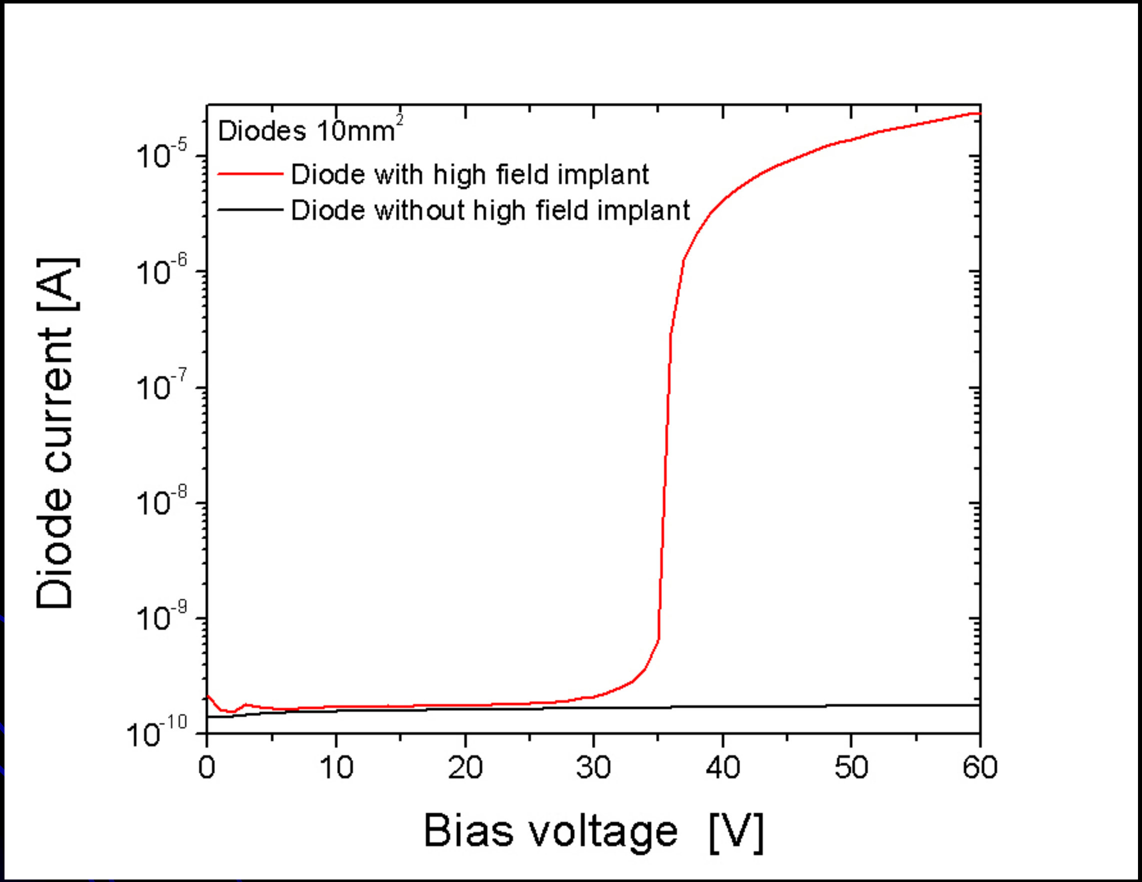


New structures – matrices



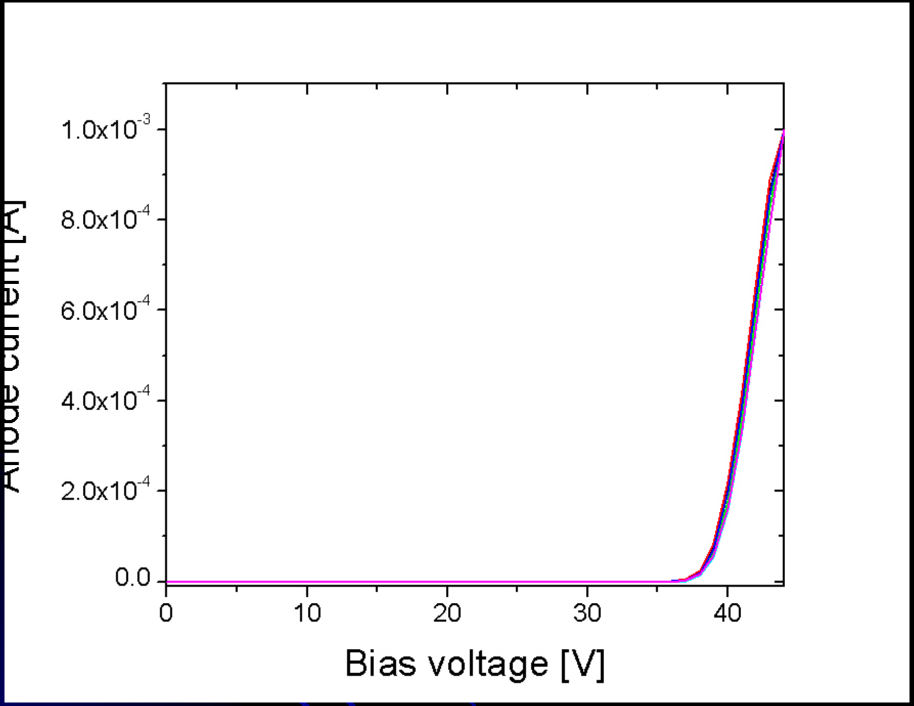
2^{nd} production run: Results

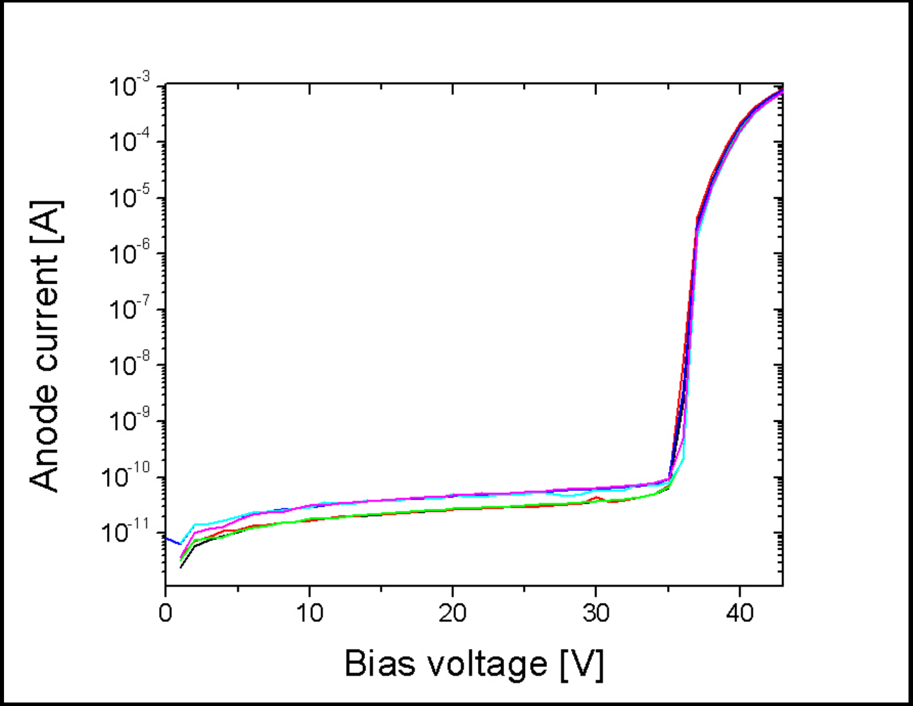
- Leakage current lowered



2nd production run: Results

- Homogeneous break down voltage

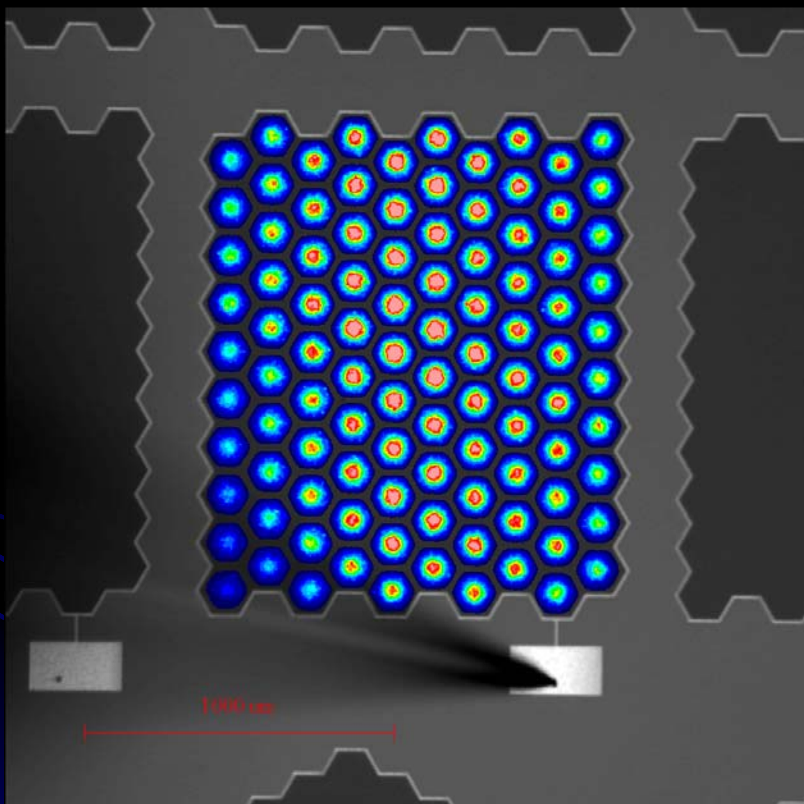


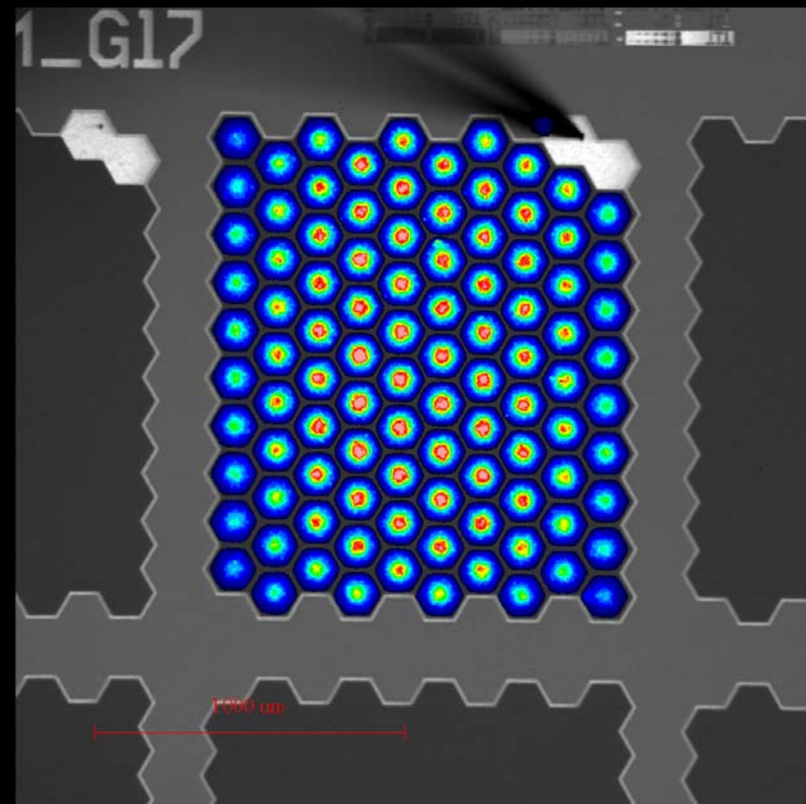


6 arrays placed over more then 5mm distance

2^{nd} production run: Results

- No edge break down





Summary

New detector concept for the silicon photomultiplier array with individual quench resistors, integrated into the silicon bulk is proposed.

- Required flexibility for quench resistor adjustment comes with wafer bonding technique (for small pixels an epitaxial layer is also suitable)
- No polysilicon resistors, contacts and metal necessary at the entrance window
- Geometrical fill factor is given by the need of cross talk suppression only
- Very simple process, relaxed lithography requirements

  -> Cost reduction in mass production

Proof of principle demonstrated – quenching works

Prototype production finished – static measurements very promising

Next: On chip characterization

Thanks