Testing of Manufacturing Faults of CMS RPC Link Boards

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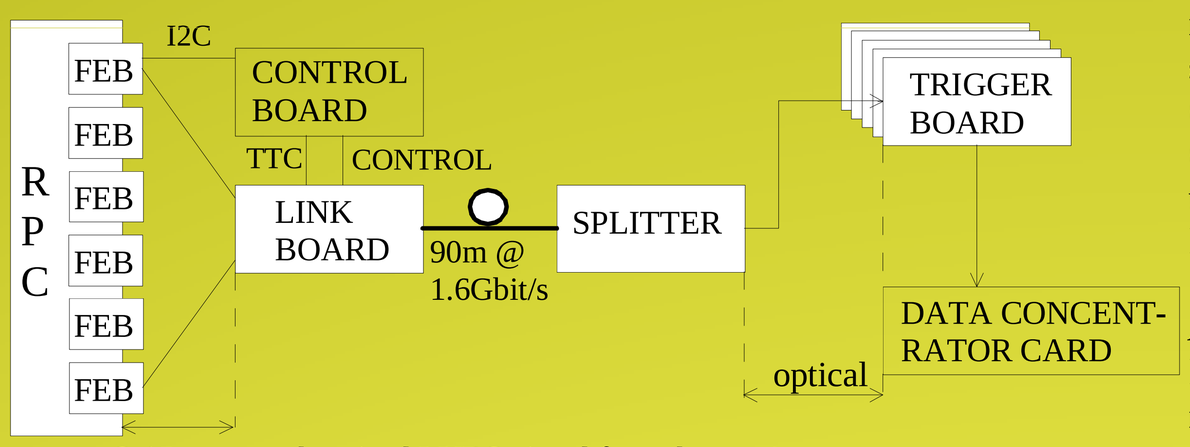
Abstract

A test board suitable for mass testing of the production of CMS RPC link boards has been developed. The test board provides a fast first-level pass of the link boards at the production facility. This ensures that link boards with basic errors are not sent further to the long-term tests at the laboratory. A Field Programmable Gate Array (FPGA) circuit is used to scan connections and shorts of the board traces. The test board functioned well and provided a fast, less than one minute per board, test at the production.

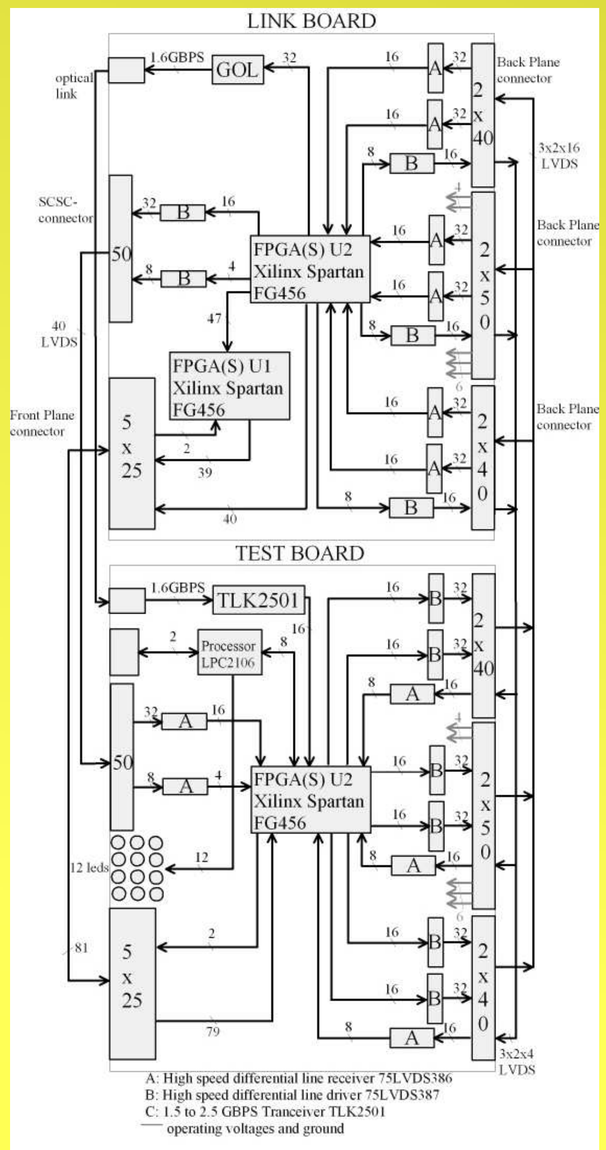
High Energy Physics experiments are entering to an era, where it is not feasible to have hand made electronics. Manufacturing and testing of large number of electronics boards has to be automated. We present here a solution adapted for the CMS experiment at the Large Hadron Collider (LHC). Muon triggering in the CMS is done with Resistive Plate Chambers (RPC), RPC is one of the major subsystems in the CMS. The RPC Muon trigger consists of RPCs, Front End Boards (FEB), Link Boards (LB), Control Boards (CB) , Splitter Boards and Trigger Boards

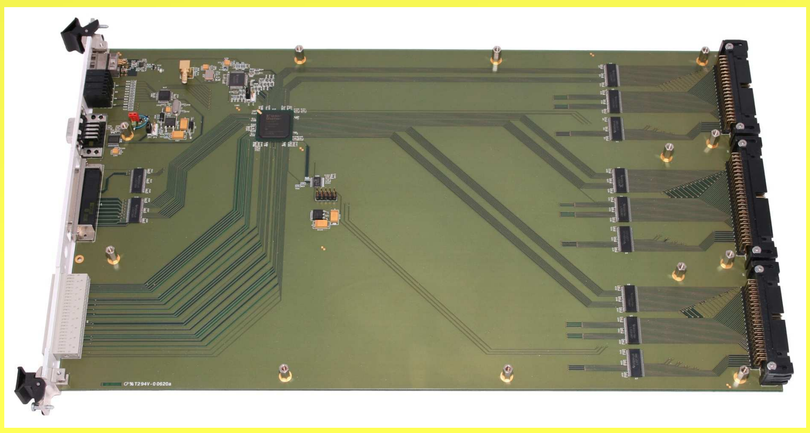


At the first phase, the link system of the CMS contains 560 Master Link Boards (MLB) and 905 Slave Link Boards (SLB). Because there is a large number of the LBs, there has to be an easy and fast way to test them at the production. This test is developed to detect manufacturing faults, like open soldered joints and shorts between traces. These problems are expected to be major concern in the production process. The whole link system is tested separately in our laboratory for all the functions.

The Link Board has parallel inputs from FEBS and test pulse outputs to the FEBS (back plane), optical output to the Splitter Board (optical link), front plane connector to communicate with the Control Board and possible SLBs and a SCSI-connector to combine the data with Cathode Strip Chambers (CSC) [4]. Two Xilinx Spartan 3 FG456 FPGA-circuits U1 and U2 at the link board are used for the testing.

The test is divided into seven subtests: GOL, CSC, FP, QPLL, BP1, BP2, and BP3. GOL tests the optical link. CSC tests the SCSI connector and FP test the Front Plane. The QPLL test tells if the QPLL (Quartz Crystal Phase-Locked Loop) circuit is locked and also if the QPLL can lock to the 80.16 MHz frequency that is used in the Link system. The test for the Back plane connectors is divided into three parts BP1, BP2, and BP3. Each test sends the test vectors first from the tester to the U2, similarly as the FEBs do in the Link system. If these vectors are received correctly and the test is passed, the U2 sends vectors to the tester as test pulses from the FEBS. The final result for this test is given after both the FEB and the test pulses are completed.





Tester board is practically a mirror of the LB. It makes possible to do the testing in the rack. The inputs of the LB are outputs of the Tester and the other way around. There is one Xilinx Spartan 3 FG 456 FPGA on the tester board circuit to perform the testing. Communication to PC and controlling of the test is made with RS323 connector and LPC2106 micro controller. Twelve LEDs on the tester are giving fast information about test results.

Conclusion

A tester board has been developed for production testing. The tester was in use in the production factory for several months, and it performed well. 50 faulty boards (24 MLB, 26 SLB) out of 1465 boards (560 MLB, 905 SLB) were found. 44 boards (19 MLB, 25 SLB) from these faulty ones were repaired. Only 18 (14 MLB, 4 SLB) boards of all the tested LBs have been found faulty in the full functional testing in the laboratory.