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Behcet Alpat¹, Giovanni Ambrosi¹, <u>Mauro Menichelli¹</u>, Andrea Papi¹, Pablo Cirrone², Francesco Ferrera², Pierpaolo Figuera², Paolo Finocchiaro², Marcello Lattuada², Danilo Rifuggiato², Fabrizio Bizzarri³, Sandor Blasko³, Diego Caraffini³, Marco Petasecca³, Francesca Renzi³, HalukDenizli⁴

¹ INFN Sezione di Perugia, Italy ²Laboratori Nazionali del Sud dell'INFN, Catania, Italy ³MAPRAD S.r.I., Perugia, Italy ⁴Abant İzzet Baysal Universitesi, Bolu, Turkey

Abstract

A high-resolution and wide dynamic range data acquisition system has been developed for general purpose applications which involve new generation of radiation detectors. Front-end comprises a hybrid interface which allows the connection of a 1.5 mm thick double-sided silicon microstrip detector as well as thin detectors up to 128 channels per detector head. Readout interface, based on two VA32TA2.2 chips for each detector side, has been developed by MAPRAD for low noise charge sensitive readout of solid state detectors with shaping, triggering, and timestamp generation circuitry. The digital data acquisition interface is based on a dual-FPGA system with a master-slave configuration and a stand-alone HV generator (TCP/IP remote-controlled). A full custom LabView front-panel was developed for the onlinemonitoring of the sensor and biasing parameters as well as for a four dimensional (X-Y-Z, θ) positioning control of the detector. The system performance has been tested at the irradiation facility of LNS-INFN, Catania and preliminary results have been reported.

Description of the acquisition system

DAQ

PC Interface

line analysis.

The DAQ system consists of two boards, one for the S-side and one for the K-side. Both the boards process the analog (pre-amplification by the front-end circuitry) and digital signals after the digital conversion.

The Master FPGA stage (clocked at 48MHz) drives all the controls signal of the hybrid (DAC and thresholds settings) and the ADC timing synchronization. A time tag is also assigned to each triggered signal. A separate "digital board" (slave FPGA) stores the data on buffer memories and transfers to the on-board computer. The data from DAQ is linked to the onboard PC through a USB 2.0 interface. The power supply system is based on a TCP/IP remote controllable unit which provide the low voltage for the data acquisition system and the high voltage to deplete the sensors.

The software for DAQ, the control of the positioning system and the monitoring of slow control parameters is based on LabView. The DAQ uses random trigger sampling for a fast

(few seconds) calibration run in order to determine the noise

and common noise behavior of the silicon detector and

readout electronics system. After the calibration the DAQ

starts and its duration can be set either by maximum number

of events to be reached or by clock time. During DAQ the raw

data are piped out on local storage for further detailed off-





FRONT END ELECTRONICS

The charge collected by silicon detectors are sent to a low power ASIC (VA32TA2.2) with a 32 channels preamplifier and fast triggering stage.

The preamplifier circuitry is 32 channel low noise, low power charge sensitive preamplifier-shaper, Sample & Hold (S&H) circuitry with multiplexed analog readout and calibration capabilities.

Each channel of the time unit circuitry consists of one levelsensitive discriminators with different adjustable thresholds. Only inputs with pulse amplitude above the threshold yield the trigger.

The total dead time of the readout system is about 20 μs which consists of the granularity introduced by the clock speed and additional few μ s of veto as safety margin.





THICK DETECTOR Squared 35.34 mm **Double side** 64 strips/detector Pitch 500um Strip width 300 um Guard-ring 300 um p-side Multiguardring standard with 10 rings n-side

Application: Beam characterization at LNS (Catania) for Space qualification of COTS

Characterization of the thick detector efficiency and preamplification channels by cosmic rays -K side and S side.





Comparison between G4 Montecarlo, Standard Physics, Charge Distributions for ⁴⁰Ar, air2=10,15,20,25 cm and Data set from LNS BAP/I

> Contacts: MAPRAD Srl, Via C.Colombo, 19/I - 06127 Ferro di Cavallo, PERUGIA - ITALY Tel. +39 075 5056317 Fax. +39 075 5156291