The ALICE silicon pixel detector read-out electronics

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Abstract

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracking system [1]. The SPD is built with 120 detector modules (half staves) and contains about 10 million pixels in total. The half-staves are connected to the off-detector electronics, housed in a control room 100 m away, via bidirectional optical links. The stream of data from the front-end electronics is processed in 20 VME readout modules, called Routers, based on FPGAs. Three 2-channel link-receiver daughter cards, also based on FPGAs, are plugged in each Router. Each Link-receiver card receives data via the optical link from two half-staves, applies the zero-suppression and passes them to the Router to be processed and sent to the ALICE-DAQ system through the detector data link (DDL). The SPD control, configuration and data monitoring are performed using the VME interface embedded in the router.

Key words: ALICE; LHC; SPD; VME

I. Introduction

The ALICE silicon pixel detector (SPD) constitutes the two innermost layers of the ALICE inner tracker system which contains 10 million pixels organized in 120 detector modules called half-staves. Each half stave consists of a linear array of 10 ALICE pixel chips bump bonded to two silicon sensors and is read out using a multi-chip module (MCM) [2,3]. The ALICE trigger has three stages (L0, L1, L2) whereas the SPD system uses L1 and L2 triggers only. It has the unique feature among the vertex detectors of the LHC experiments to contribute to the definition of the L0 trigger. The pixel chips provide binary hit information, which is stored in a delay line during the L1 decision time. In case of a positive L1 decision the hit is stored in one out of four multi-event buffers where the data wait for the L2 decision to be read out or discarded. The ALICE trigger scheme foresees a non-pipelined architecture and allows the detector read-out systems to temporarily reject triggers by sending a busy signal to the central trigger processor. The ALICE SPD off-detector electronics controls, configures and reads out the detector via bidirectional optical links. The front-end data streams are processed in 20 readout modules (Router), based on FPGAs, each carrying three 2-channel link-receiver daughter cards. The processed data are sent to the ALICE-DAQ system on the ALICE detector link (DDL) [4] for permanent storage. In Table 1 the SPD main system parameters and running conditions are summarized. The SPD control, configuration and data monitoring are performed using the VME interface of the routers. Configuration and trigger data are sent from the VME based electronics (router and link receiver card) in the control room

Table 1: Main system parameters and running conditions

L1 rate	1 kHz
L1 latency	6.5 μs
L2 rate	40–800Hz
L2 latency	100 – 500 μs
Read-out time	256 μs
Multi-event buffers	4
Total Ionizing Dose (inner layer)	2.5 kGy (10 years)
Fluence (1MeV equivalent)	$3x10^{12}cm^{-2}$(10 years)
Material budget per layer	<1% X_0

to the on-detector electronics via two optical fibers, one carrying the clock and one carrying serial data. On the detector the PIN diodes in the optical package and the RX40chip [5] convert the optical signals to electrical signals. The PILOT2003 chip [6] initiates the read-out of the pixel chips and controls the ANAPIL chip, which provides analog bias voltages to the pixel chips and measures supply, bias voltages and the temperature on the detector. Once read-out has been initiated the nonzero-suppressed data are sent from the pixel chips via the PILOT2003 and an 800 Mbit/s G-link compatible optical link driver chip GOL [7] and an optical fiber to the control room. There the data are zero-suppressed and formatted in the FPGA-based link receiver mezzanine board. The router performs data multiplexing and establishes the interface to the ALICE trigger and data acquisition. In total 20 router cards read out the 120 half staves. Figure 1 shows a block diagram of the full SPD read-out chain.

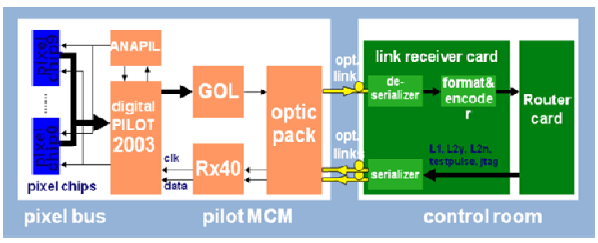

Figure 1: Global readout block diagram

II. Link Receiver and Router

Each of the two link-receiver channels has three optical fibre links; two links for the clock and the serial trigger, control and configuration data and one 800 Mbit/s G-link compatible link to receive data from the detector. On the link

receiver the pixel data stream from the detector is de-serialized, the received data are checked for format errors and stored in a buffer-FIFO before being zero suppressed, encoded, re-formatted and written to a dual port memory, as depicted on Fig.2. When all data from one event are stored in the dual port memory on the link receiver, the link receiver asserts event ready flag to be read out by the Router processor. The G-link receiver deserializes the data stream and recovers the 40 MHz transmission clock using a commercial component (Agilent HDMP1034) [8]. The implementation of the link receiver is also based on a commercial FPGA and dual port memories. The expected occupancy of the detector will not exceed 2%. It is therefore efficient to encode the raw data format after zero suppression. In the raw data format the position of a hit within a pixel row is given by the position of logic '1' within a 32-bit word. The encoder transforms the hit position into a 5-bit word giving the position as a binary number for each single hit and attaches chip and row number to the data entry. The output data from the FIFO are encoded and stored in an event memory.

The Router receives the trigger control signals from the ALICE Central Trigger Processor (CTP) through the on-board TTCrx chip [9] and forwards the trigger commands to the pixel detector. Upon reception of the L1 trigger signal the Router sends trigger signals to the detector and the pixel data are copied into multi-event buffers on the pixel chips. After reception of the positive L2 decision, the Router starts to check the event ready flag in the status register of the link receivers. When the event ready flag appears the router processor reads the data from the link receiver dual port memory. Each Router sequentially reads one event from each of the link receiver channels in order to merge data from the 6 channels and labels them with trigger and status information to build one router sub event. The sub events of each of the routers are sent to the ALICE-DAQ system through the ALICE detector data link (DDL). The read out data stream can also be copied into a dual port memory, where it is accessible for data monitoring and analysis via the VME-interface. The Router architecture including the link receiver is shown on Figure 2. The data access for the SPD control and configuration is performed via the router VME-interface. The router converts the data to JTAG compatible commands which are sent to the detector through the optical links with a maximum data rate of 5 Mbit/s. The Router is a 10-layers Printed Circuit Board with a 1020 pins chip Altera Stratix EP1S30 component as the main processor. The VME interface is inside an Altera APEX EP20K60EQC FPGA with 240 pins. This is shown on Fig. 3.

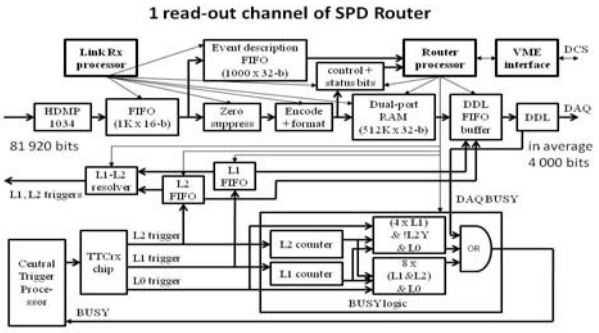

Figure 2: Router architecture

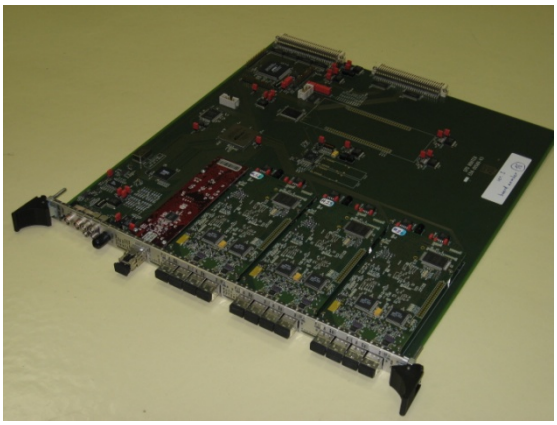

Figure 3: SPD Router

III. Summary

The SPD detector system including the off-detector electronics was tested in the CERN Divisional Silicon Facility (DSF) – a clean room where the full detector system was integrated and commissioned before being moved to the underground area. After tests on the surface, the whole detector system has been installed in the experimental cavern. The integration of the ALICE SPD off-detector electronics and tests with final detector elements have proven to satisfy all specifications. Performance of the system has been qualified during first beam from LHC in September 2008.

IV. References

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