A 3D deep n-well CMOS MAPS for the ILC vertex detector

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Abstract

This work presents the features of a new kind of deep n-well monolithic active pixel sensor (DNW-MAPS), called SDR1 (Sparsified Data Readout), which exploits the capabilities of vertical integration (3D) processing in view of the design of a high granularity detector for vertexing applications at the International Linear Collider (ILC).
SDR1 inherits and extends the functional capabilities of DNW-MAPS fabricated in planar (2D) CMOS technology and is expected to show better collection efficiency with respect to 2D versions. The aim of the paper is to outline the features of analog and digital architecture of the SDR1 chip, together with circuit simulations data. Also some device simulation results concerning detection efficiency will be discussed.

Key words: MAPS, 3D integration technologies, CMOS, front-end electronics

1. Introduction

In the last years, CMOS monolithic active pixel sensors (MAPS) have been proposed as suitable candidates for charged particle trackers at the next generation colliders like ILC and Super B-Factory. MAPS devices, indeed, may comply with the severe constraints set by the future experiments at these colliders, which require highly granular and low mass detectors. CMOS MAPS are adequate in terms of material budget, since their sensing element shares the same substrate with the readout electronics; furthermore, substrate thickness can be reduced to a few tens of microns with no significant signal loss. Resolution constraints can be respected combining the advantages coming from the use of scaled CMOS processes with vertical integration capabilities [1] in MAPS fabrication. Because of the large amount of data produced in the readout of large matrices, an innovative solution of MAPS was proposed a few years ago [2]. This solution relies upon the use of a deep n-well/p-substrate junction, provided by triple-well CMOS technologies, as collecting element. In this way, the sensor can be extended to cover a large area of the pixel cell. These devices, called deep n-well MAPS, allow designers to realize more complex readout circuits, taking advantage of fully CMOS architectures: the effects of charge collection from PMOS n-wells, which acts as competitive electrodes against the main collecting electrode, may be significantly limited. Moreover, such devices can be affected by crosstalk between analog and digital sections. Vertical integration processes, by stacking two or more layer one on the top of the other, make it possible to reduce interaction effects between different sections of the pixel cell. 3D processes may also improve collection efficiency since PMOS wells can be placed in a different layer with respect to the sensor.

2. The SDR1 chip

SDR1 features two vertically integrated layers, each fabricated in a 130 nm CMOS process provided by Chartered Semiconductor, containing the analog and the digital front-end respectively; wafers will be vertically integrated by means of a cost-effective process provided by Tezzaron Semiconductor [3]. SDR1 operation is based on the ILC beam structure. It features

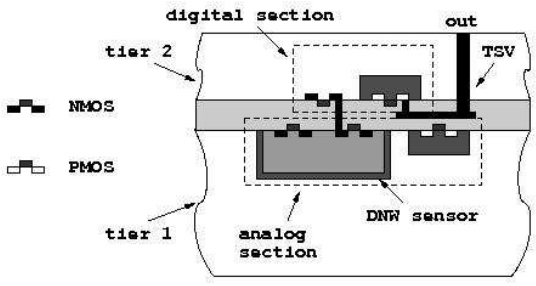

Figure 1: Schematic cross sectional view of the SDR1 cell.

two different processing phases: a detection phase (corresponding to the bunch train period) and a readout phase (corresponding to the intertrain period). SDR1, whose simplified cell sectional view is shown in Fig. 1, consists of a 240x256 MAPS matrix with a pixel pitch of 20 μm. The analog tier (tier 1) includes DNW sensor, a charge sensitive amplifier and the NMOS pair from the threshold discriminator, while digital tier (tier 2) hosts the digital front-end (two latches for hit storage, sparsification logic, two time stamp registers, kill mask blocks), the

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digital back-end (X and Y registers, time stamp line drivers, serializer) and PMOS pair from the discriminator. Logic blocks are able to keep information about two hits during each single bunch train with the relevant time stamps (5 bit resolution), thus providing a high detection efficiency. Tiers interconnections are provided by means of wafers face-to-face bonding, based on thermo-compression techniques, while connections to and from the outer world are obtained by means of through silicon vias (TSV), which are made to emerge on one side of the stack by aggressive back thinning of the silicon wafers.
Fig. 2 shows the analog front-end of SDR1. Charge restora-

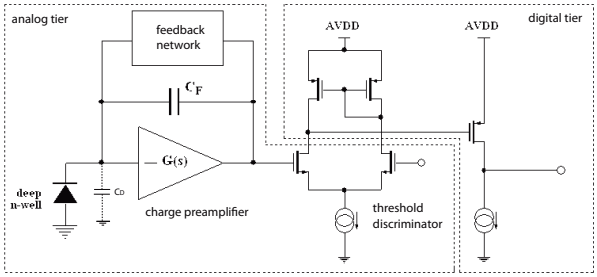

Figure 2: Analog front-end of the pixel cell.

tion in the preamplifier feedback network is obtained through a current mirror stage, providing a linear discharge of the capacitor C_F. Charge sensitivity in the preamplifier is designed to be about 800 mV/fC. In the design of the circuit, the high frequency noise contribution has been reduced by purposely limiting the preamplifier bandwidth. For a detector capacitance C_D of 200 fF an equivalent noise charge (ENC) of 35 e^- was obtained from circuit simulations. An overall input referred threshold dispersion of 36 e^- was computed from Monte-Carlo simulations: main contributions arise from the preamplifier input device (a 20/0.18 NMOS transistor) and from NMOS and PMOS pair in the discriminator. Power consumption of the elementary cell is about 5 μW.
The digital front-end of the SDR1 chip is shown in Fig. 3. During the detection phase a time stamp is sent to all cells: the

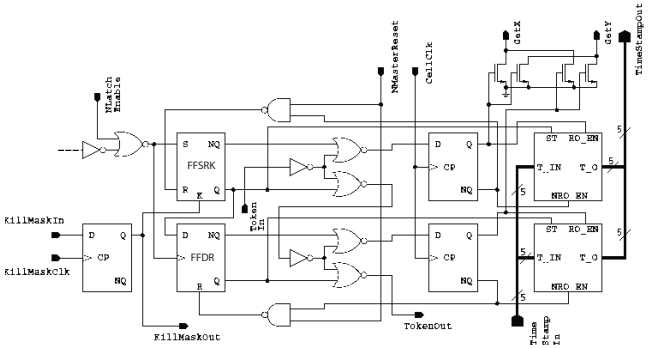

Figure 3: Digital front-end of the pixel cell.

set/reset flip-flop (FFSRK) is set when the pixel is hit the first time. Upon a second hit, the D-type flip-flop (FFDR) is also set. At the same time, the relevant time stamp registers get frozen. At the end of the detection phase a token is launched through the matrix and sparse readout is performed [4]: the hit cells, after the arrival of the token, send both the coordinate and time stamp data to the output serializer at the next cell clock (CellClk) rising edge; data are serialized and transmitted off the chip within a cell clock period (1 CellClk/hit). Output data from the serializer are 24 bit long words: achievable bit rate is in the order of 100 Mbit/s.

3. Monte Carlo Simulations

In order to evaluate the collection efficiency, Monte Carlo simulations have been performed on clusters of 3x3 DNW MAPS featuring the layout of a 2D cell and SDR1 sensors (10000 experiments, 80 μm thick substrate). Fig. 4 shows the layout of the DNW sensors and of n-wells both in a 2D DNW-MAPS and in the SDR1 cell. The results of Monte Carlo

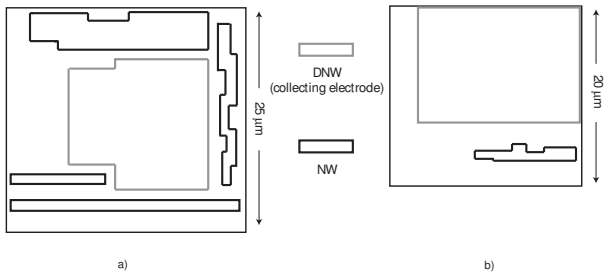

Figure 4: Cell geometries of a 2D DNW-MAPS (a) and SDR1 sensor (b).

simulations are shown in Fig. 5. In the SDR1 collection efficiency turns out to be significantly increased with respect to a 2D MAPS: indeed, large area PMOS devices belonging to the threshold discriminator were laid out on the digital tier of the chip, thus remarkably reducing the competitive n-well areas. Moreover, placing the fully CMOS digital electronics in

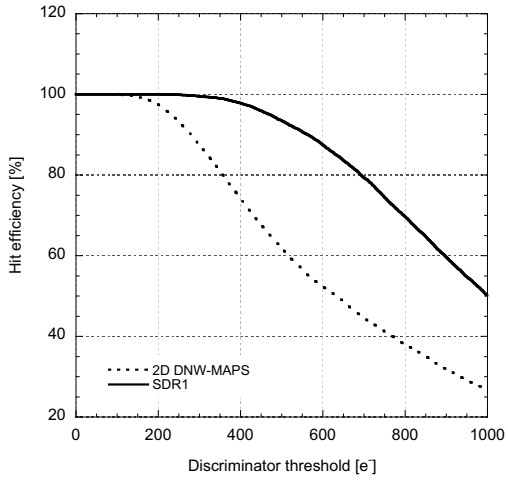

Figure 5: Comparison of the collection efficiency between a 2D DNW-MAPS and SDR1 sensor.

a different tier from the sensor layer, makes it possible to further reduce the area covered by competitive electrodes, therefore providing better collection efficiency than in the case of DNW MAPS in planar technology.

4. Conclusion

We present the design of a 3D DNW-MAPS suitable for vertexing applications at the ILC. This device features a sparsified readout architecture, and is able to store two hits with the relevant time stamps during each bunch train. Collection effciency turns out to be signicantly increased with respect to a 2D MAPS as a consequence of the separation of the analog and digital electronics, reducing the area covered by competitive n-wells in the analog tier.

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