CMOS Analog Front-End Channel for Silicon Photo-Multipliers

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INFN DASiPM Collaboration

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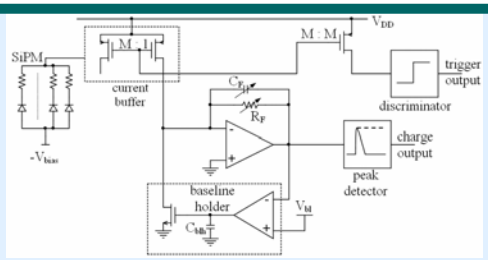
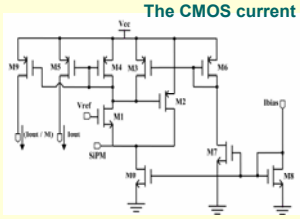
Architecture of the analog channel



- AMS 0.35μm standard CMOS technology – 3.3V power supply;
- Variable gain integrator: Gain: 1V/pC ÷ 0.33V/pC (2 bits); τ_i = 200ns; Output voltage range: 0.3V ÷ 2.7V; Current mirror scaling factor 10:1.
- Current discriminator: Current mirror scaling factor 1:1; Threshold variable from 0 to 40μA (about 50 microcells @ V_{BIAS}=-31.5V).
- Baseline holder (V_{bl}=300mV): Very slow time constant; Non-linearities added to prevent baseline shifts at increasing event rates.

The CMOS current buffer

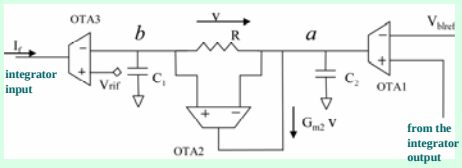


- Common gate configuration (M1)
- Feedback applied to increase bandwidth and decrease input resistance (M2, M4)
- SiPM bias (and gain) fine tuning possible by varying Vref
- Bias point of M2 and M4 set by means of the current source M3

Main specs

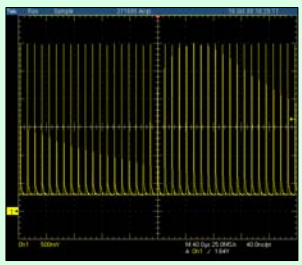
- Open loop poles: $\omega_1=g_{m1}/C_{SiPM}$ (first pole) $\omega_2=g_{m4}/C_A$ (second pole)
- Loop gain T = g_{m2}/g_{m4} set to 10 for stability
- Small signal bandwidth: 250MHz
- Total current consumption: 800μA
- Rise time of the output waveform: 400ps
- Vref variable in the range 1V÷2V
- Input resistance: 17Ω
- Linearity dynamic range: about 50pC

The Baseline holder (BLH) circuit



- OTA_1 is the error amplifier
- OTA_3 delivers the feedback current I_F
- The current i_{TOT} is proportional to the current i_{C1}: $i_{TOT}=i_{C1}(1+G_{m2}R)$
- C_1 is magnified by a factor of $(1+G_{m2}R)$
- Large time constants can be obtained with practical C_1 values

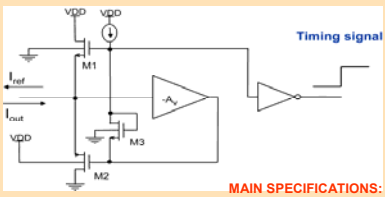
Non-linear intrinsic effects have been exploited to limit the variation of the feedback current I_F due to the increase of the event rate



Response of the integrator to a pulse train (full dynamic range, 100kHz rate)

Observed shift of the baseline ≅ -1mV

The Current discriminator



MAIN SPECIFICATIONS:

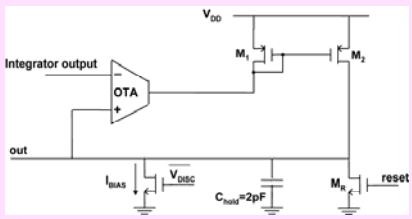
t_{RISE} ≅ 300ps;

Delay ≅ 1.2ns, almost indipendent of the threshold value;

Maximum variation of the delay with Iref ≅ 200ps;

- External threshold setting via I_{REF} control;
- I_{out} is a 1:1 replica of the current buffer output;
- Advantages: high speed (less than 2ns delay).

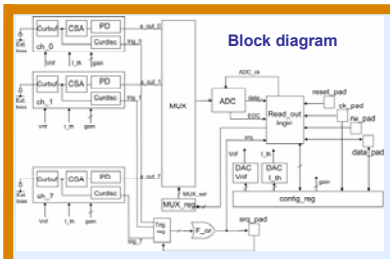
The peak detector

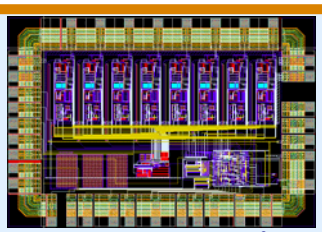


- It is based on a P-MOS current mirror as a rectifying element
- I_{BIAS} added to improve the speed of operation, especially for small signals

Architecture of the 8-channel ASIC (BASIC)

Block diagram



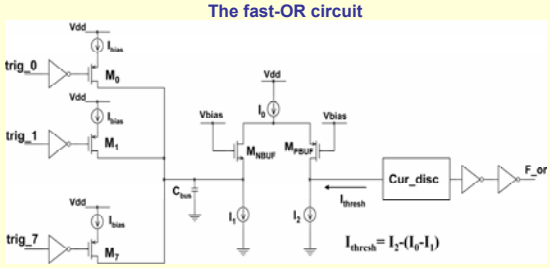


Layout (size ≅ 3.2 x 2.2 mm²)

Main features

- Three operating modes: write configuration, read configuration and acquisition
- Two acquisition modes: "sparse read-out" and "serial read-out"
- Standard cell read-out logic
- All the channels share the same Vbias e I_th
- 8 bit successive approximation ADC from a library
- Fast-OR circuit operating in current mode, to improve the speed of operation

The fast-OR circuit

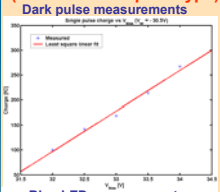


- Current-mode approach (large capacitive loads)
- Current buffer added to drive the current discriminator
- Current discriminator with fixed threshold

Measurements

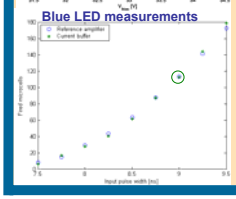
Preliminary measurements (current buffer prototype)

Dark pulse measurements



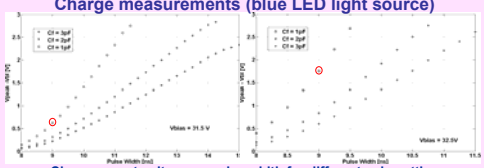
Single dark pulse charge as a function of V_{bias}

Blue LED measurements



Average number of fired microcells as a function of the input pulse width

Single channel measurements
Charge measurements (blue LED light source)



Charge-ouput voltage vs pulse width for different gain settings

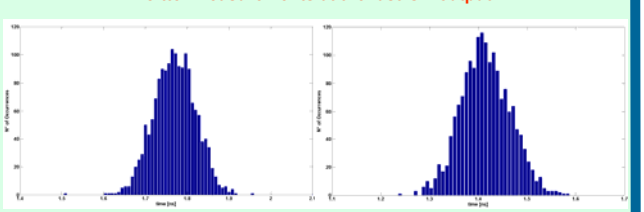
From the preliminary measurements, for pulse width = 9ns, we have n=115 fired μcells and:

Vbias	31.5V	32.5V
$Q_T = Q_{1cell}(Vbias)*n$ (total injected charge)	6.9pC	17.3pC

Vbias	31.5V	32.5V
expected $Q_T/(M*C_f)$	690mV	1.73V
measured V_{peak}-V_{bl}	630mV	1.76V

Measurement are in good agreement with the expected results

Jitter measurements at the fast-OR output



One excited channel: slowest case
Average delay μ_S = 1.77ns
Standard deviation σ_S = 50 ps

Two excited channels: fastest case
Average delay μ_S = 1.42ns
Standard deviation σ_S = 50.5 ps

Worst case dispersion ≅ ($\mu_S + 3\sigma_S$) - ($\mu_D - 3\sigma_D$) ≅ 652 ps

Target design value ≅ 1ns