The ATLAS “Insertable B-Layer”

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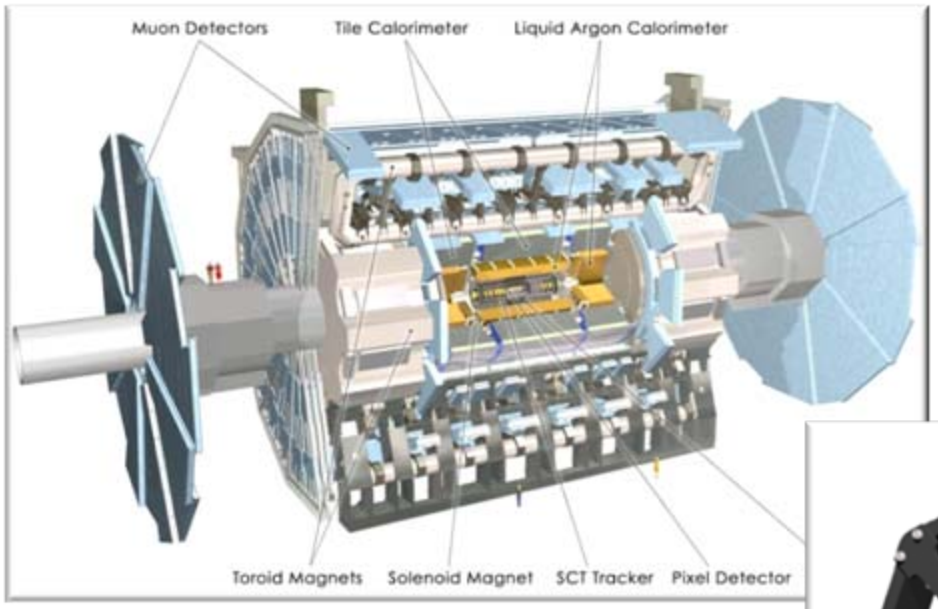
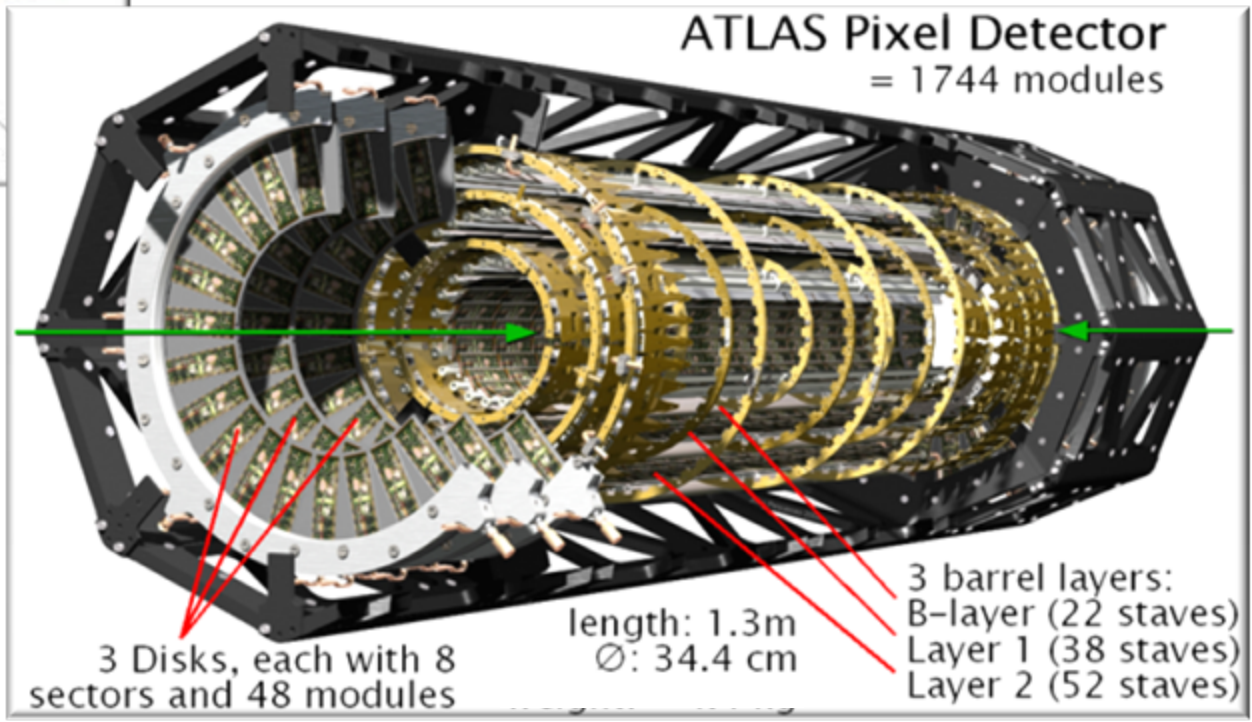
D. Giugni / INFN Milano

The present ATLAS Pixel Detector



- 1744 separate pixel modules
- 80 mio. readout channels
- 3 track points down to |h|=2.5

- 50x400 um² pixels
- spatial resolution:
  10 um in R-f, 115 um in z
- radiation hardness
  Specs 500kGy ; tested to
  >1000kGy and 2e15 n_{eq}

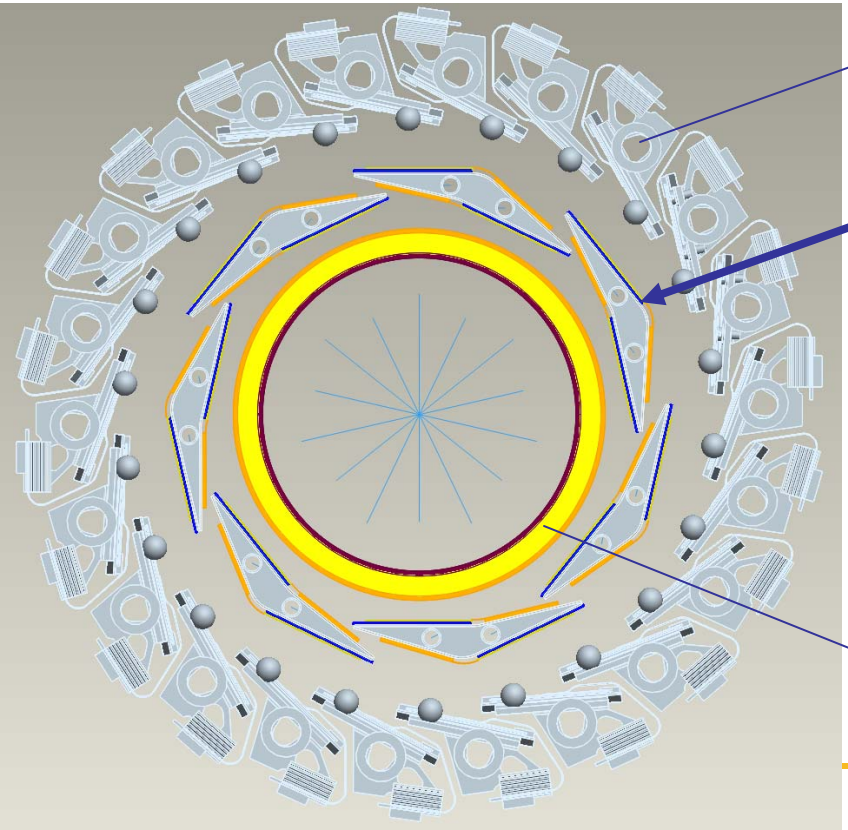


The 4th Pixel Layer: Insertable B-Layer

- The present ATLAS Pixel Detector has 3 Layers, the innermost is called “B-Layer”
  - The B-Layer will gradually loose efficiency due to radiation damage to sensors and chips
  - It needs to be replaced in the “LHC Phase 1 upgrade” shutdown (~2013/14)
- Removing the present B-Layer was studied in detail and was found to be not feasible because
  - Time required is significantly longer than winter shutdown 2013/14
  - Risks to Layer 1 and 2, which stay in place, are significant
- Solution: Add a 4th Pixel Layer inside the present B-Layer: **The Insertable B-Layer**
  - Existing Pixel detector stays installed and a 4th layer is inserted inside the existing pixel detector together with new beam pipe . (Requires new, smaller radius beam pipe to make space)
- It serves also as a “**technology step**” from now to sLHC
  - This is the first project of the ATLAS Upgrade program
  - The IBL project will be the first to use much of the **new technologies** currently under development **for sLHC** (FEI4 chip, new sensors, …)

Layouts under study☐

- 14 (15) staves, each with 32 FEI4 Frontend chips
- Sensor surface ~ only 0.2m^2
- 16 degree tilt angle
- ~35 mm sensor radius
- ~33 Inner Radius, 41.5 Outer Radius
- Beam pipe ID 25mm (To be confirmed)
- Uses newly developped FE chip: FEI4
- Pad size 50x250μm
- Chip size 20.1x19.6mm
- Radiation hardness >200Mrad

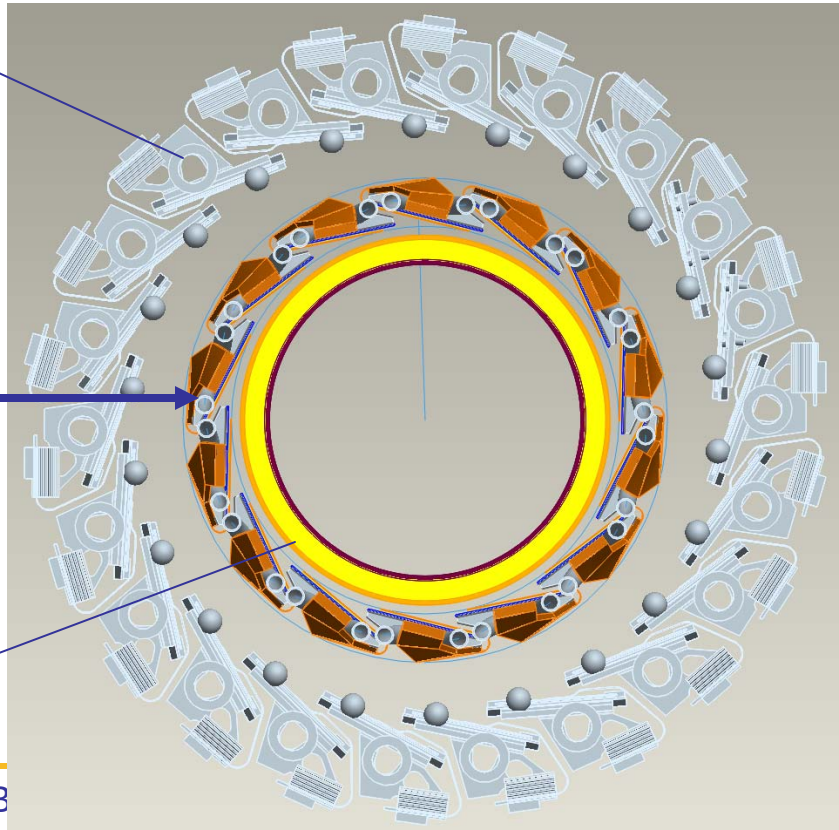


Present B-Layer

IBL with 2 sensor Rows per stave ("bi-stave")

IBL with single Sensor row

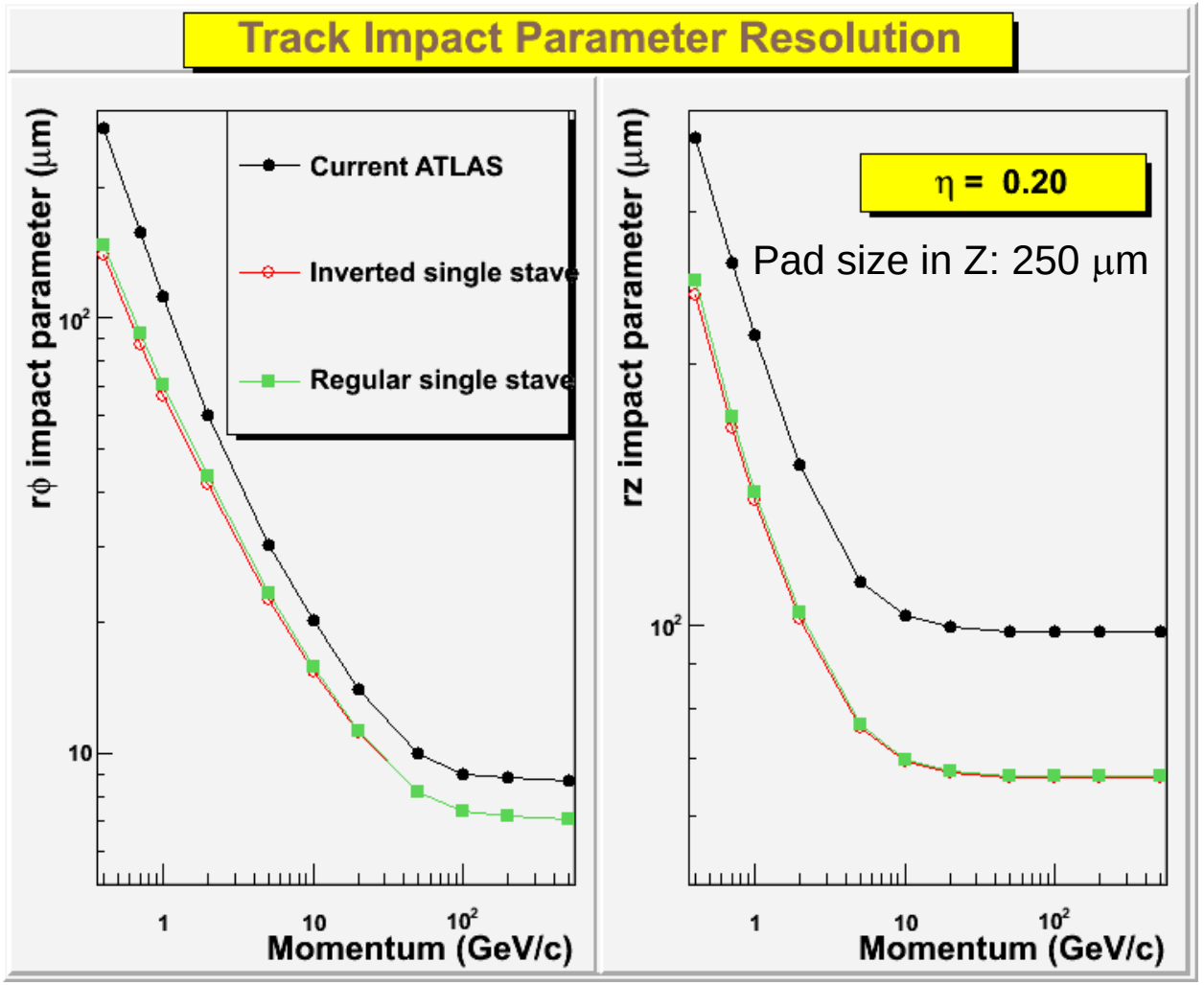
Beam Pipe with Insulation and Heater pads For backout



IBL Performance

- IP res Z: 100μm->~60μm
- IP res RΦ : 10μm -> 7μm
- B-tagging: Light Jet rejection factor improves by factor ~2
- To maintain Pixel Detector performance with inserted layer, material budget is critical.

Component	% X_0
beam-pipe	0.6
New-BL @ R=3.5 cm	1.5
Old BL @ R=5 cm	2.7
L1 @ R=8 cm	2.7
L2 + Serv. @ R=12 cm	3.5
Total	*11.0*



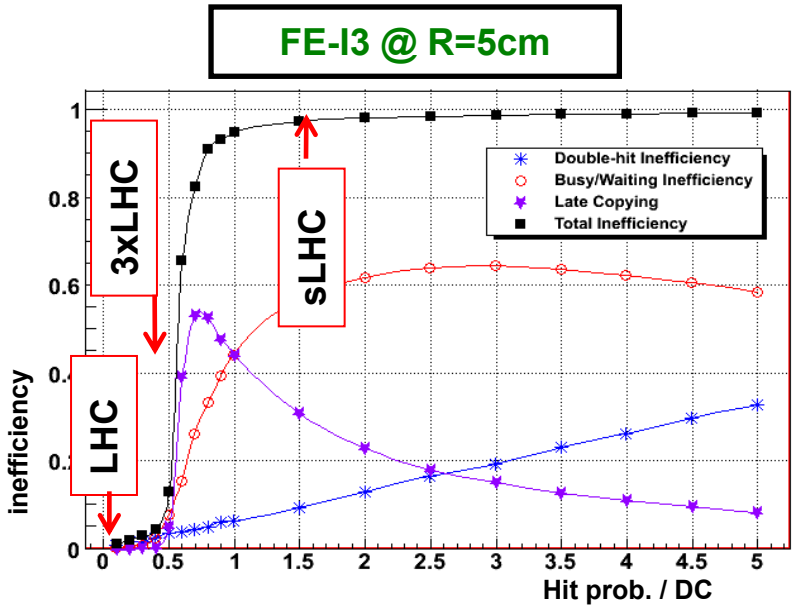
IBL and sLHC

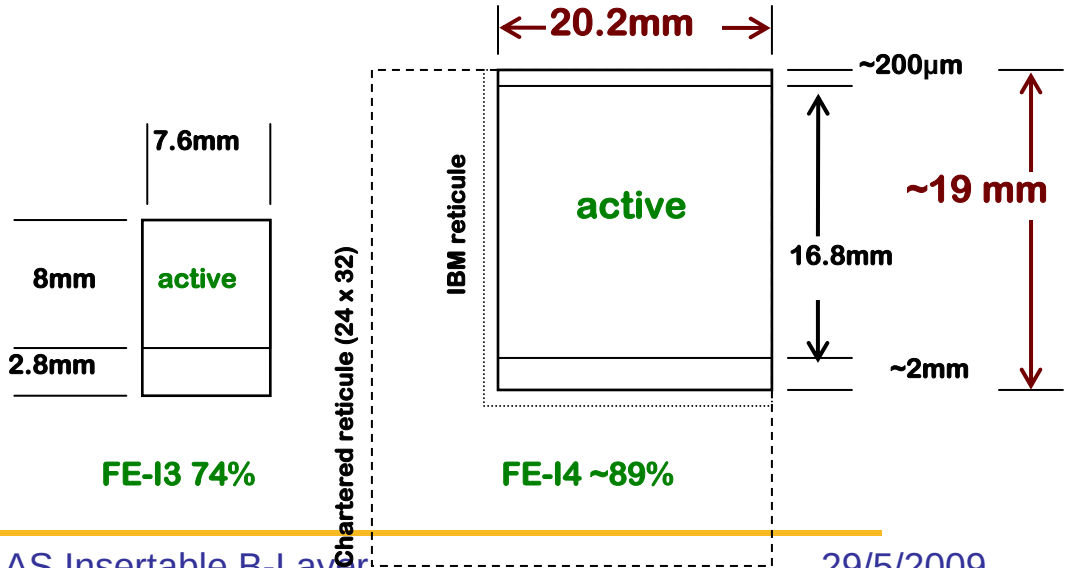
- The IBL will be the **B-Layer for the LHC high luminosity running**
  - We plan to minimize the changes to the minimum necessary from the present system and integrate it completely into the present Pixel detector
  - The IBL is also **a bridge to sLHC**: Its requirements (radiation hardness approximately 3x present system) require us to develop new technologies for it
- With IBL we will make the **technology step to sLHC**
  - Radiation hardness ~ 3 to 5 x 10^{15} n_{eq}/cm^2 (sLHC ~ 10^{16} in inner layers)
  - Timescale: IBL ~4-5 years from, sLHC ~10 years from now
  - **Frontend IC4**: go to IBM 130nm process and improve readout architecture to minimize inefficiency at high hit rates and radiation hardness
  - **Sensors**: investigate 3D silicon sensors, new planar sensors and CVD diamond sensors as possible options for radhard detectors
  - **Readout system & optolink**: improve data through-put and redundancy. Will go to 160MHz from present 40MHz clk for data upling of IBL
  - **Cooling system & Mechanics**: investigate more efficient cooling of sensors+chips with significant **reduction in X0** on staves. Investigate CO2 evaporative cooling in parallel to existing C3F8 cooling and new cooling pipe technologies (CF pipes, Ti pipes)
  - **Installation in existing ATLAS Detector**: All installation will be developed with constraints of existing detector and work requirements for radiation zones

New Pixel Front-End Chip: FEI4

- Reasons for a new FE design:
  - Increased radiation hardness
  - New architecture to reduce inefficiencies ($\mathcal{L}$=3xLHC)
- New FE-I4
  - Pixel size = 250 x 50 μm^2
  - Pixels = 80 x 336
  - Technology = 0.13μm
  - Power = 0.5 W/cm^2 (max) , 0.25 W/cm^2 (nominal)
- FE-I4 Design Status
  - Contribution from 5 laboratories: Bonn, CPPM, INFN Genova, LBNL, Nikhef
  - Main blocks MPW submitted in Spring 2008 and under test now
  - Working on Full-Size FE-I4 ready for submission to build IBL prototype modules next year

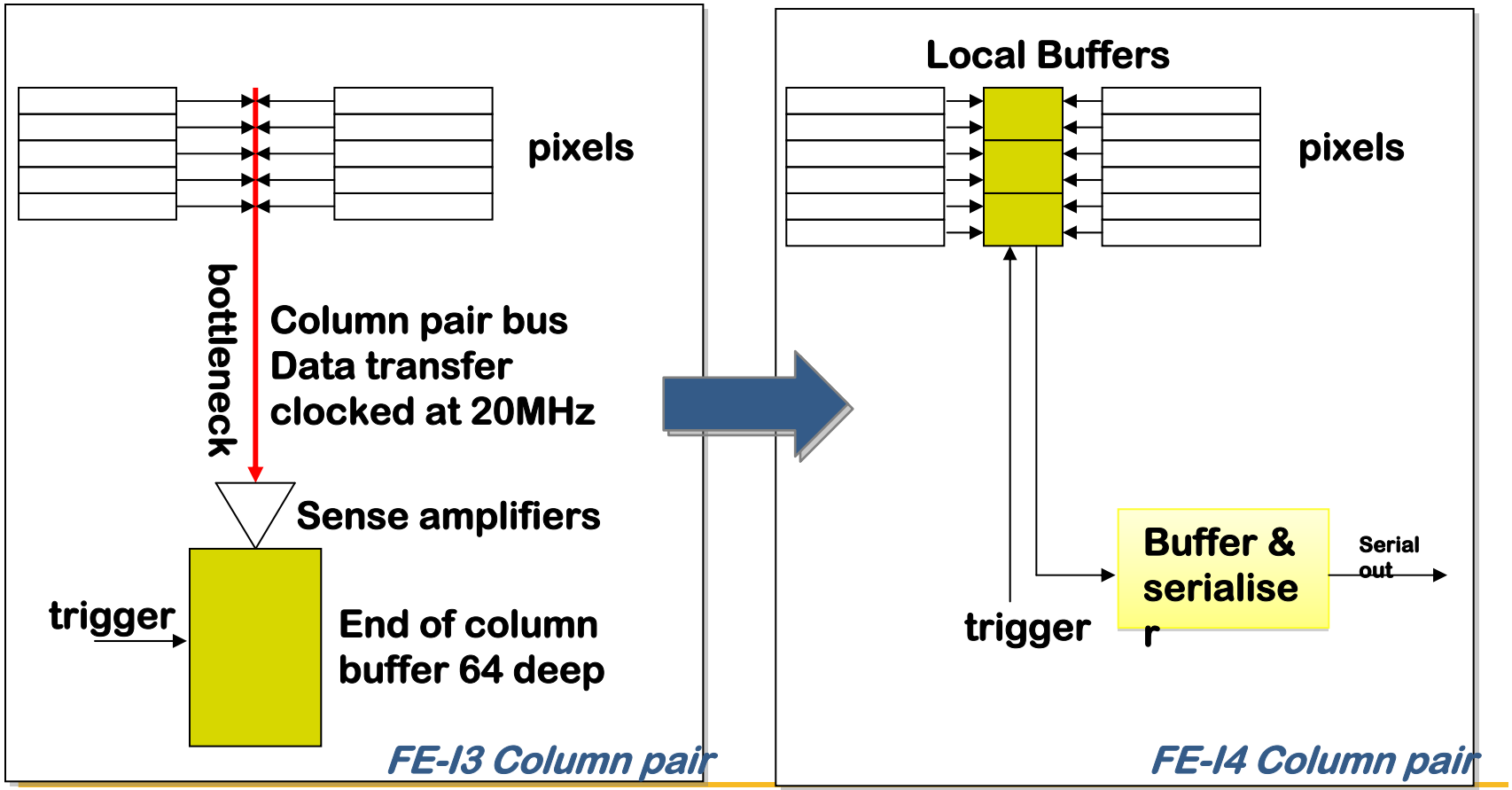
"Busy" inefficiency: with FEI3 at LHC = 0.08% but with IBL 3%!



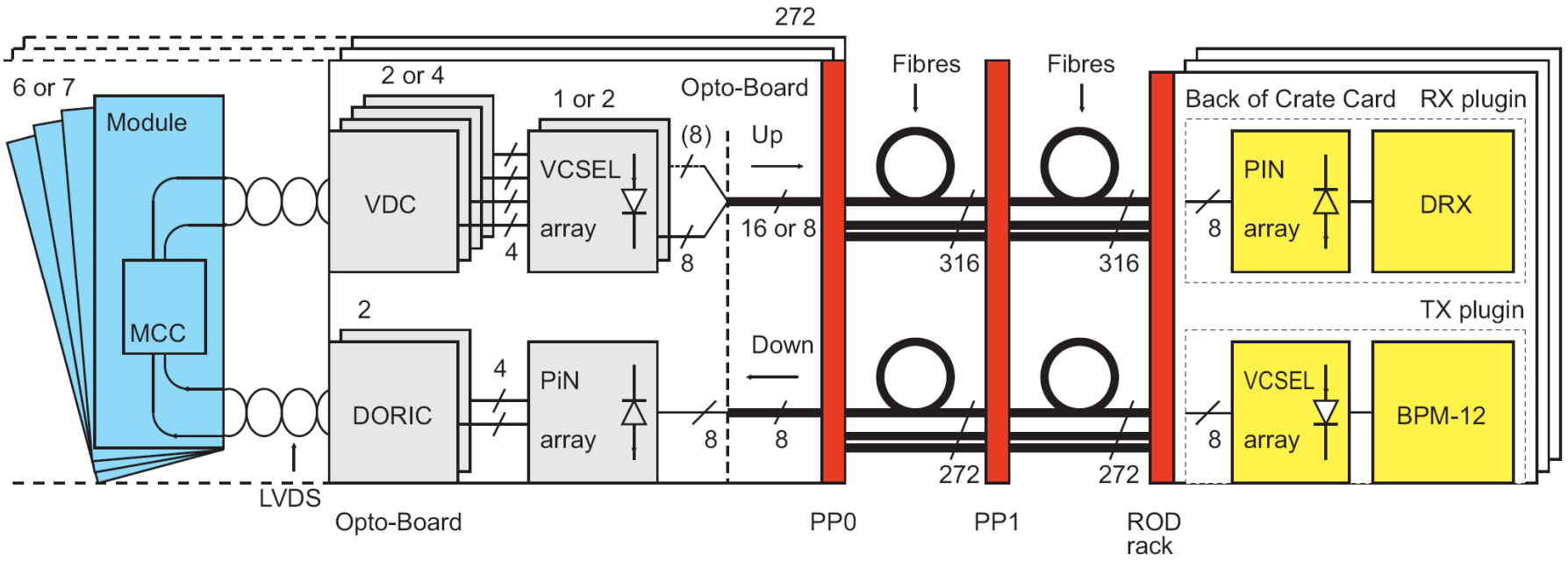


FE-I4 Architecture: Obvious Solution to Bottleneck

- >99% of hits will not leave the chip (not triggered)
  - So don't move them around inside the chip! (this will also save digital power!)
- This requires local storage and processing in the pixel array
  - Possible with smaller feature size technology (130nm)



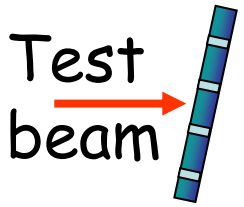
Readout Links

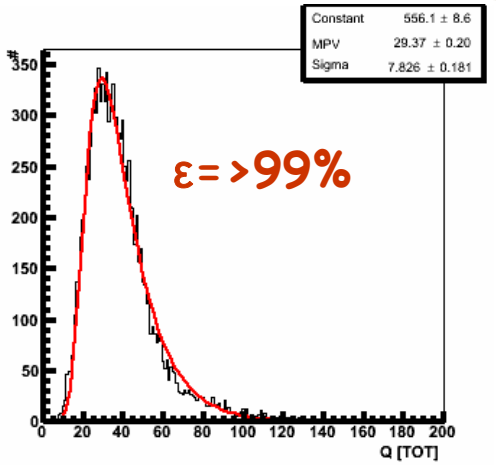


- Try to minimize changes from present system:
  - Down link (TTC) stay the same 40Mb/s
  - Uplink use 160 Mb/s data+clock (8b/10b encode) – Single FE-I4
  - Need new BOC design
  - Use GRIN fibers (under rad-test for SLHC, or new Ericsson)
  - Opto-board at PP1 – need test of reliable electrical signal transmission (~4-6m)

Sensors: 3D silicon

- Approved ATLAS upgrade R&D
- pro's:
  - Good charge collection but more power in the FE for same time-walk
  - Active edge
  - Lower voltage (<150 V), power after irradiation lower than planar
- Con's:
  - column Inefficiency at 90º
  - Higher C_{det}
  - Need to establish yield in "scale" production
- See Poster by Andrea Zoboli/Trento on FBK 3D-DDTC sensors and Cinzia DaVia on 3D detectors for LHC upgrade

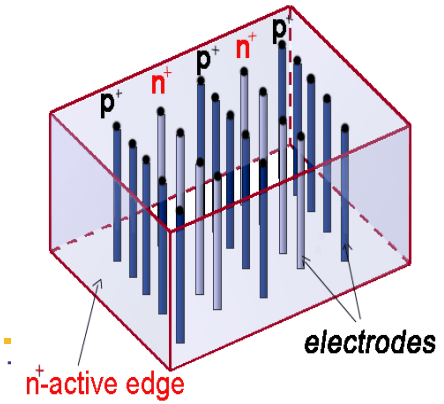


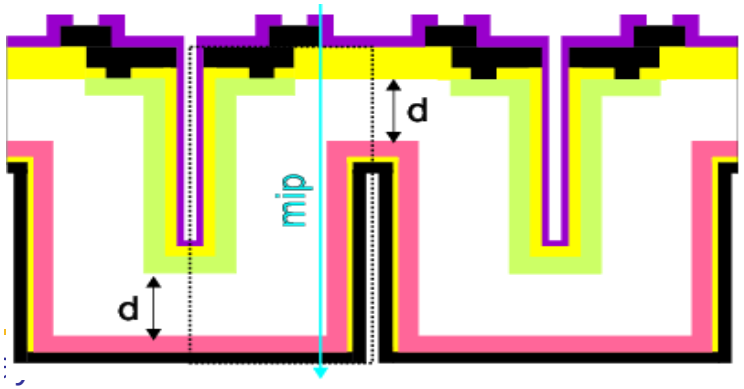


IRST - FBK Trento
Run n-on-p completed FE-I3 bump-bonded. Active edge being included in layout
CNM
n-on-p completed and FE-I3 waiting for bump-bonding

Double column design

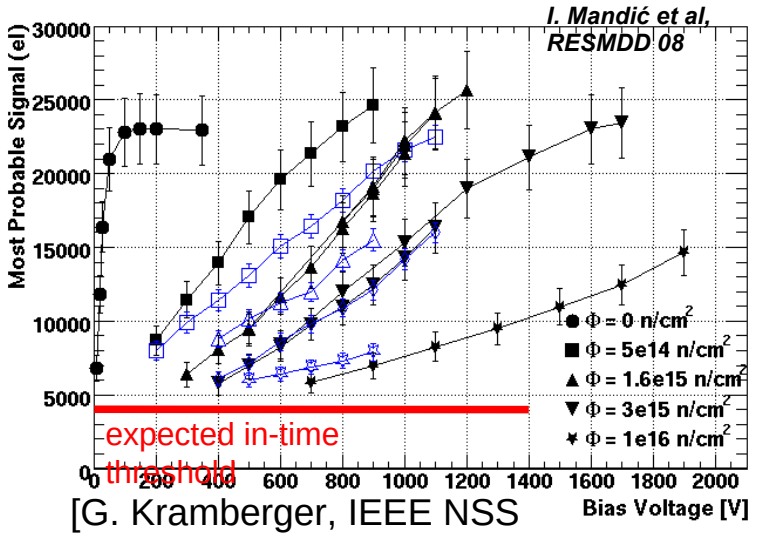
3DC Fabricated at Stanford
and tested with Atlas pixel and SLHC fluences
3DC SINTEF
FE-I3 n-on-n Bum-bonded. n-on-p with FE-I4 run started. Should be ready by spring 09



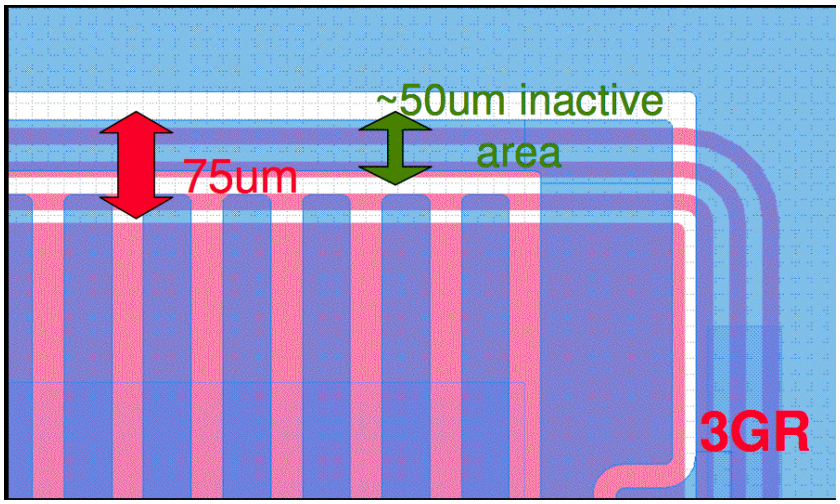


Sensors: New planar silicon

- Approved ATLAS upgrade R&D
- Pro's
  - n-on-n is a proven technology with minor changes for IBL (pad size)
  - n-on-p single sided process (costs) is being studied
  - Lower C_{det} -> lower noise, lower in-time threshold for same power settings in the FE.
  - Partially depleted sensors collect charge
- Con's
  - Need for slim edges -> reduce dead area in Z
  - Need high bias voltage (~1000V_{bias}?)
  - N-on-p need high voltage insulation on chip side



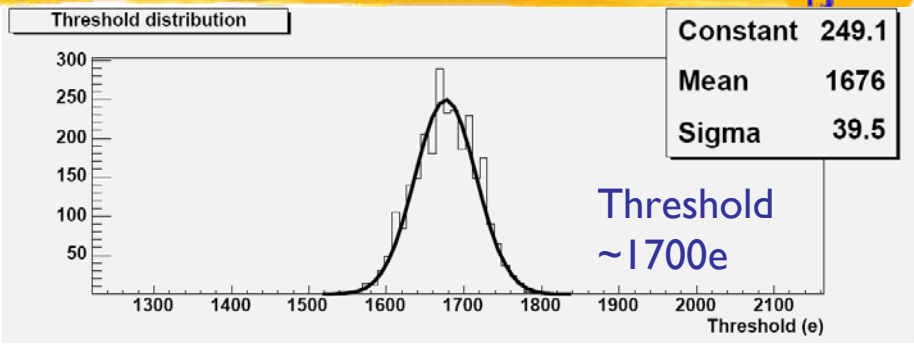
[G. Kramberger, IEEE NSS 2008, Dresden]

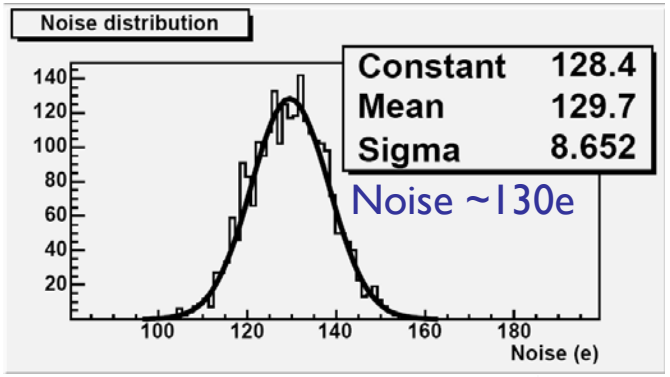


- Study n-in-n and n-in-p structures with DOFZ and MCz wafers
- Develop "slim" edges (reduce guard ring width)
- Submitted prototype run at CiS (Erfurt)

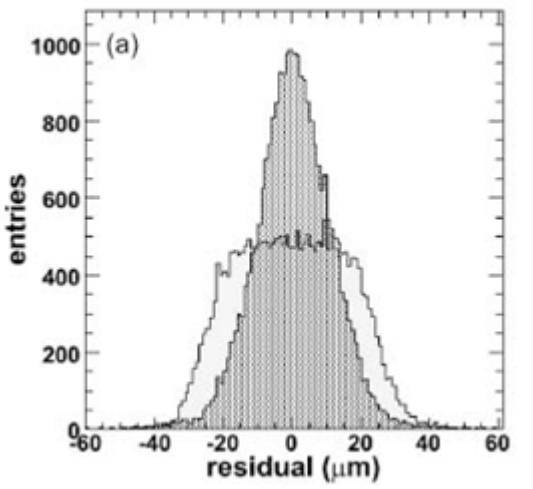
Sensors: CVD diamond

- Approved ATLAS upgrade R&D
- pro's:
  - No leakage current increase with radiation
  - Lower capacitance, therefore less threshold required for in-time efficiency
  - Can operate at any temperature, no cooling issues
- Con's:
  - Smaller signal (with poly-crystal CVD)
  - Need to establish yield in "scale" production
  - Higher cost & number of vendors (?)





QuickTime™ and a
TIFF (LZW) decompressor
are needed to see this picture.



Spatial resolution with TOT informatio:

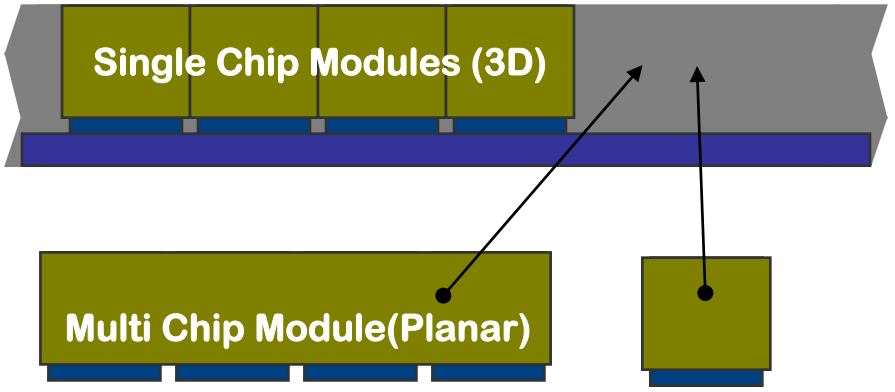
8.9μm

e B

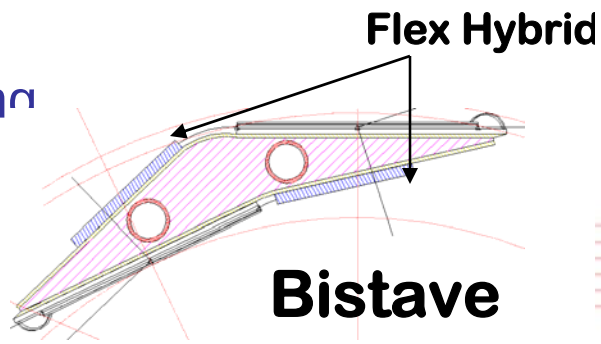
IBL Stave

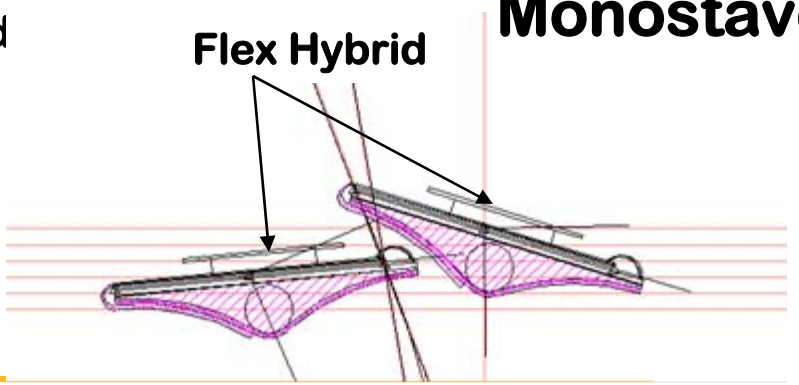
- Function
  - Support for single or multi chip modules
  - Separate readout to each chip
  - Chips connected through flex cable to end of stave
- Main challenges
  - Minimize material (!!!)
  - Low temperature gradient in stave to allow lower silicon temperature at given cooling temperature
  - Minimize CTE
- 2 Types in prototyping
  - Monostave
  - Bi-stave

Pre-tested stave structure with integrated bus and cooling, SMD and burned-in power adapters



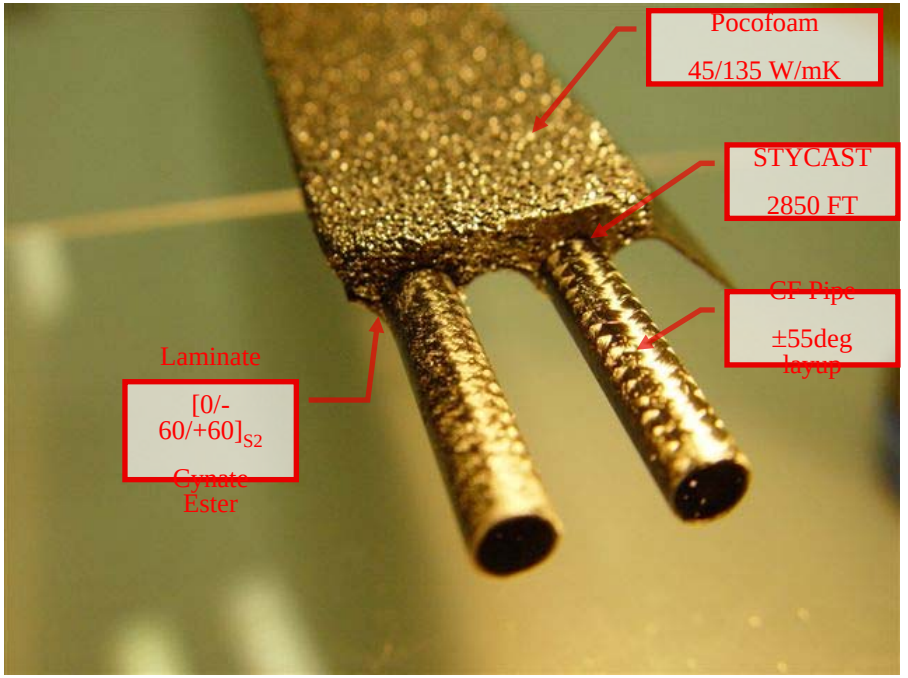
Robotically placed, fully tested 1-chip or multi-chip modules. Wire bond to stave after placement.





Stave R&D

- Aim to minimize and unify material (“homogeneous stave”)
  - Staves currently being prototyped by INFN Milano, CPPM, Wuppertal
- Stiffness provided by CF shell
  - Fiber YS-80A; resin EX-1515
- Carbon foam provides heat transfer from modules to cooling pipe
  - Poco Foam or Kopers KFOAM L1-250
- Prototypes build with 2 types of pipes:
- **Carbon fibre pipe**
  - Less X0
  - match CTE with rest of stave
  - No corrosion
- **Titanium pipe**
  - Less temperature gradient in pipe
  - Smaller pipe ID achievable
  - Welding possible
  - Low CTE (compared to other metals)



Cooling: CO_2 or C_3F_8

- IBL cooling parameters:
  - 15 staves with ~100W each ← P_{total} =1.5kW
- Options (limited by main constraint: develop time & working experience):
  - CO_2: copy of the LHCb VELO system, similar in cooling power.
  - FC: present Pixel+SCT C_3F_8 system (after modifications).
- Prototyping CO_2 and C_3F_8 cooling system in cooperation with ATLAS CERN cooling groups and NIKHEF

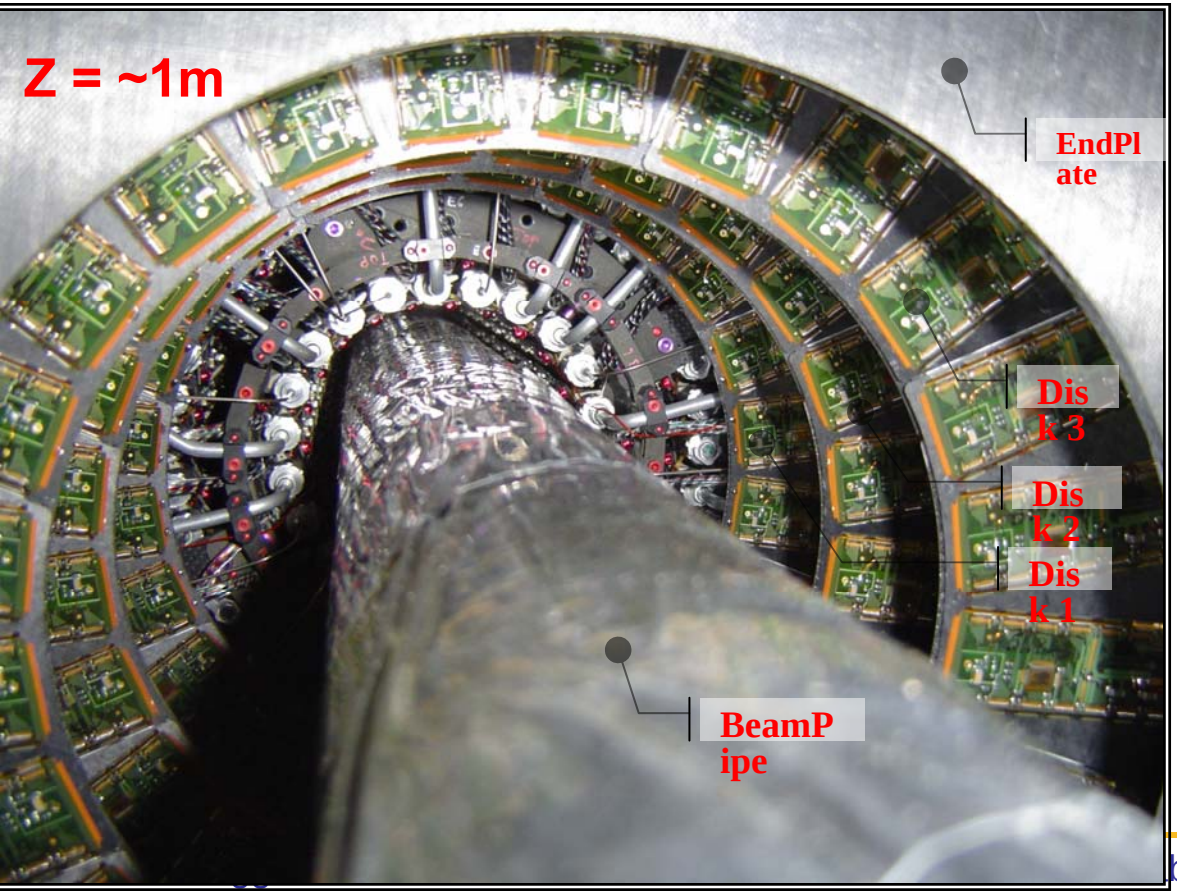
- Pipe material plays important role in **thermal gradient:** figure of merit is between 16.5 °C.cm²/W (CF) and 2.4 °C.cm²/W (Ti), Ti therefore allows for higher sensor power before thermal run-away
- Choice of coolant influences **pipe diameter** (CO2: ~1.6mm, C3F8 ~3mm) and minimal **evaporation temperature** (C3F8 min T_{evap}=-30°C, CO2 min T_{evap}= -45°C)
- Want redundancy (2 pipes) to avoid this significant “single point failure” in case of leak/blockage of one pipe

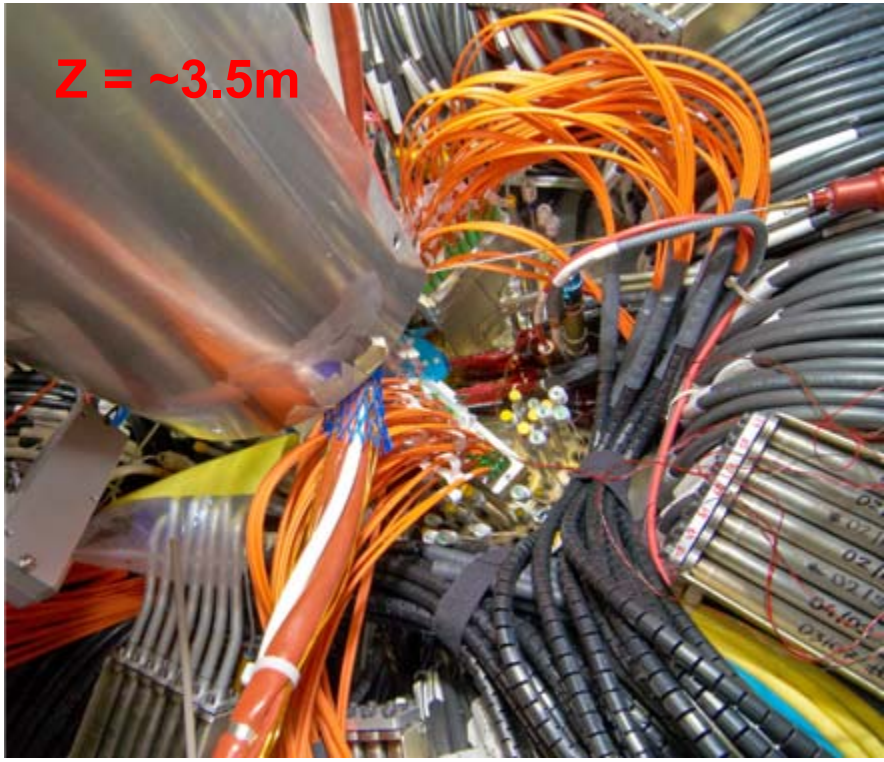
Very preliminary material breakdown for different options:

"Invariant Contributions"	X0 [%]	
Silicon sensor (250um)	0.27	
FE chip	0.33	
Flex circuit	0.2	
Stave foam (4mm with X0=426cm)	0.09	
Carbon facings (2x200um)	0.13	
Total invariant	***1.02***	
"Cooling contribution"		
CO2 pipe 1.5mm ID		
C3F8 pipe 3.0mm ID	C02	C3F8
Coolant fluid (liquide 80/60%)	0.03	0.13
Cooling pipe CF (300um)	0.04	0.07
Cooling pipe Ti (120um)	0.12	0.22

IBL Installation and access to present Pixel

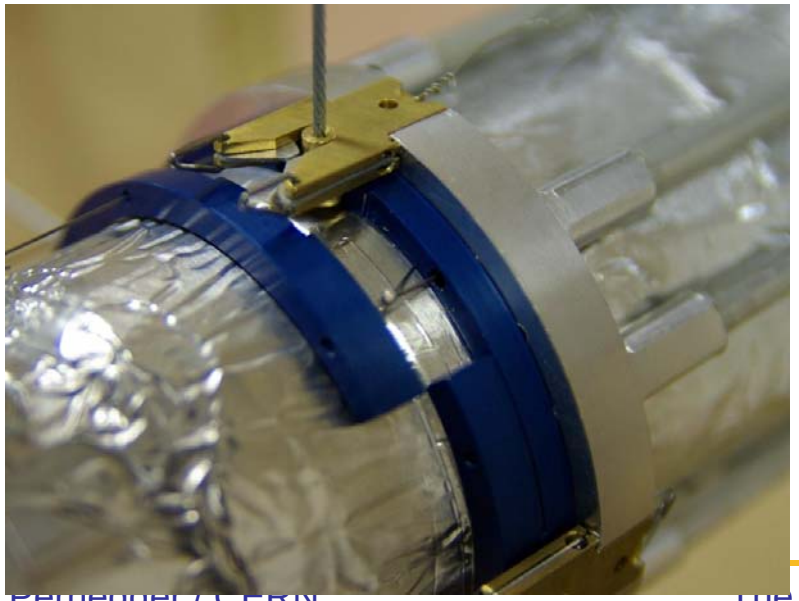
- Beam Pipe extraction & Installation complicated by
  - Activation of surrounding area
  - Very little access to beam pipe and long lever arm (access is at z~3.5m)
  - Minimize any risk to present Pixel Detector

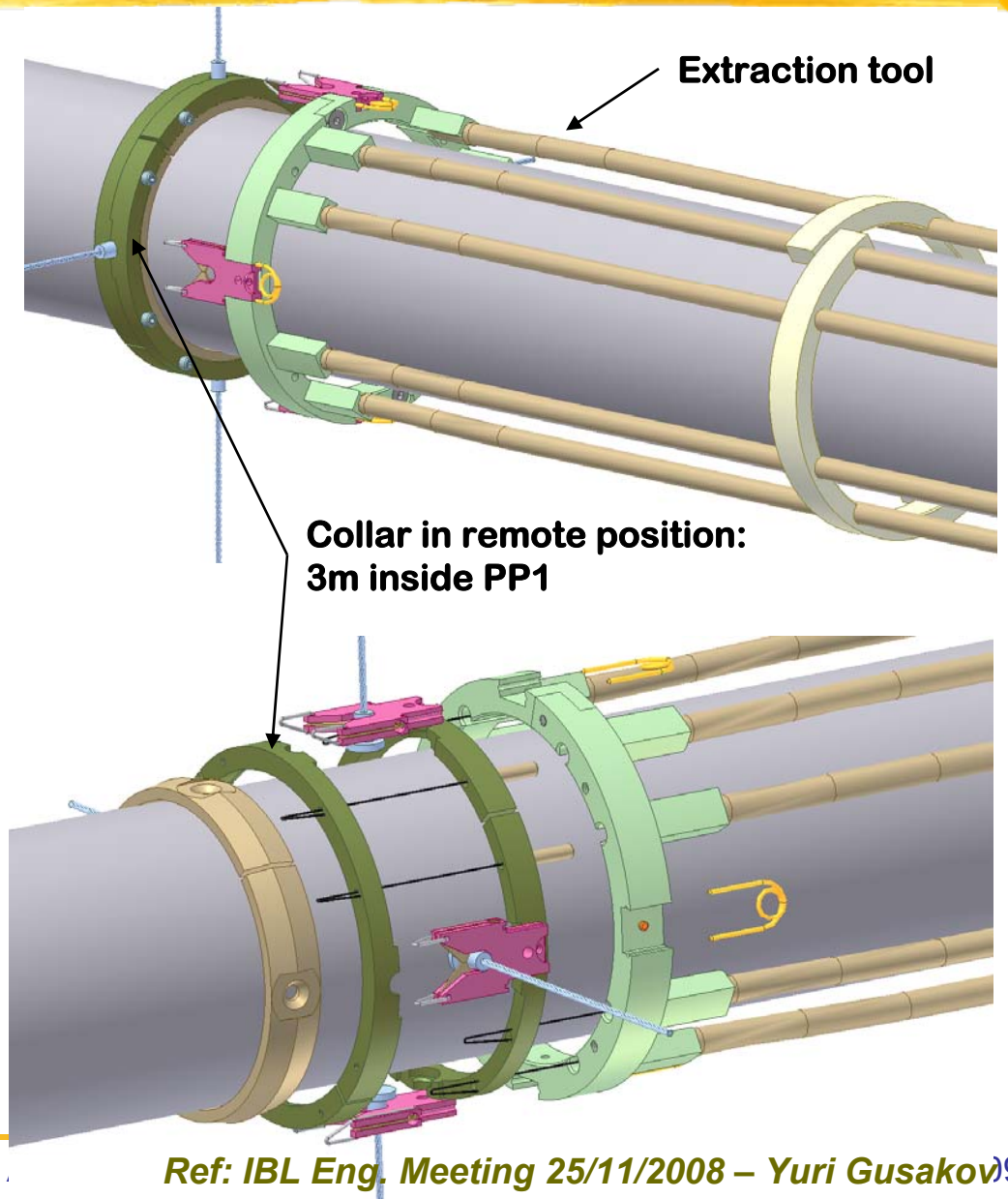




Beam Pipe extraction

- Tools to dismount Beam Pipe support collars:
  - Remote access >3 m inside
  - Activated material – fast operation
- Beam pipe must been supported from inside.
  - Tool has to compensate gravity bow (7m long pipe).

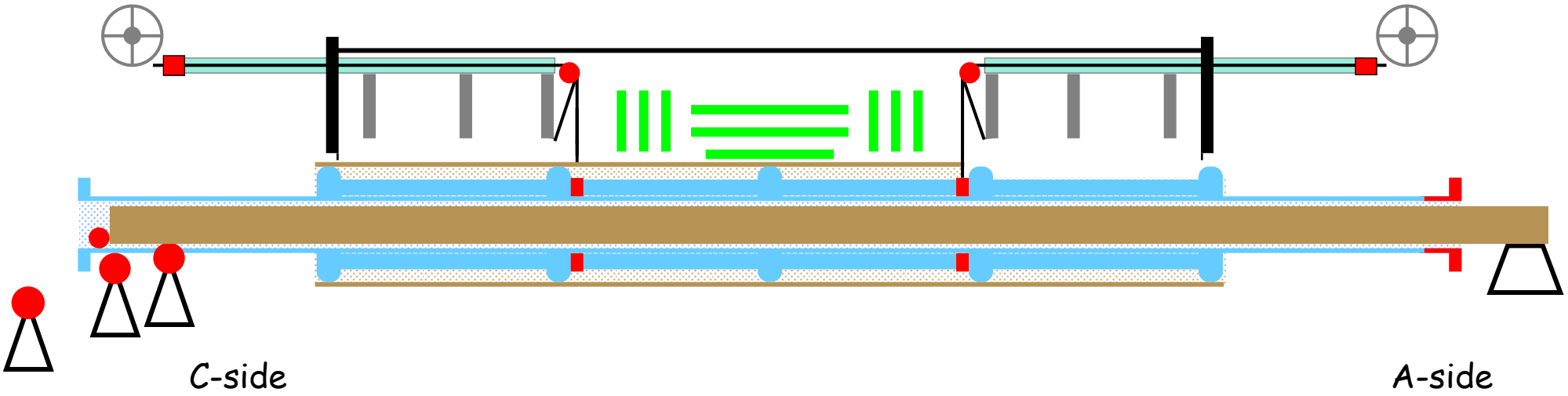




Ref: IBL Eng. Meeting 25/11/2008 – Yuri Gusakov

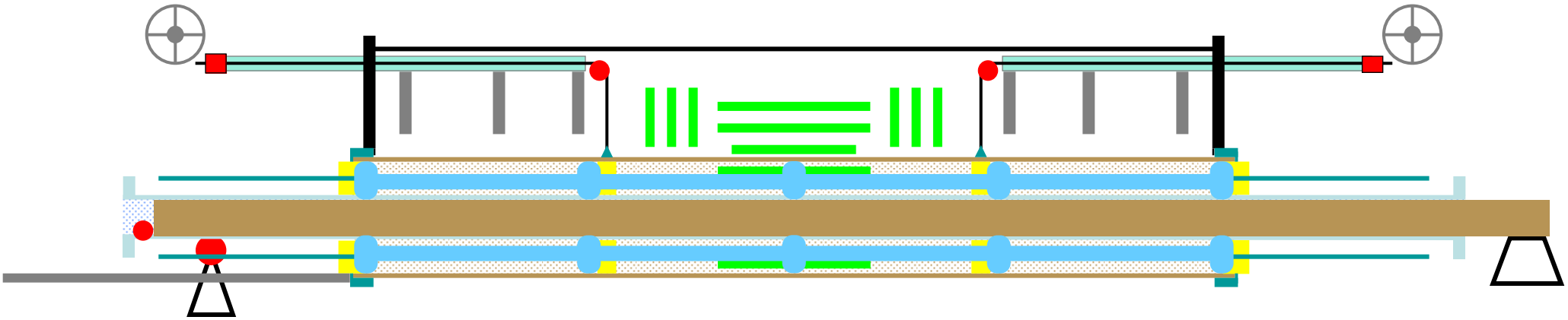
Extraction sequence

- **The beam pipe flange on A-side is to close to the B-layer envelope . Need to be cut on the aluminum section**
- A structural pipe is inserted inside the Beam Pipe and supported at both sides.
- The support collar at PP0 A-side is disassembled and extracted with wires at PP1.
- Beam pipe is extracted from the C-side and it pulls the wire at PP1
- New cable supports are inserted inside PST at PP0.
- A support carbon tube is pushed inside the PST along the structural pipe.



IBL installation scenario

- Different scenarios under study now
- The support carbon tube is fixed in 2 point of PP0 and on PP1 walls on side C and A.
- The structural pipe with a support system is moved out from the support carbon tube.
- The new beam pipe (in any configuration with OD up to 82,5 mm) is inserted from C-side. It has 2 supports at PP0 area and 2 floating wall at PP1 on side A and C.

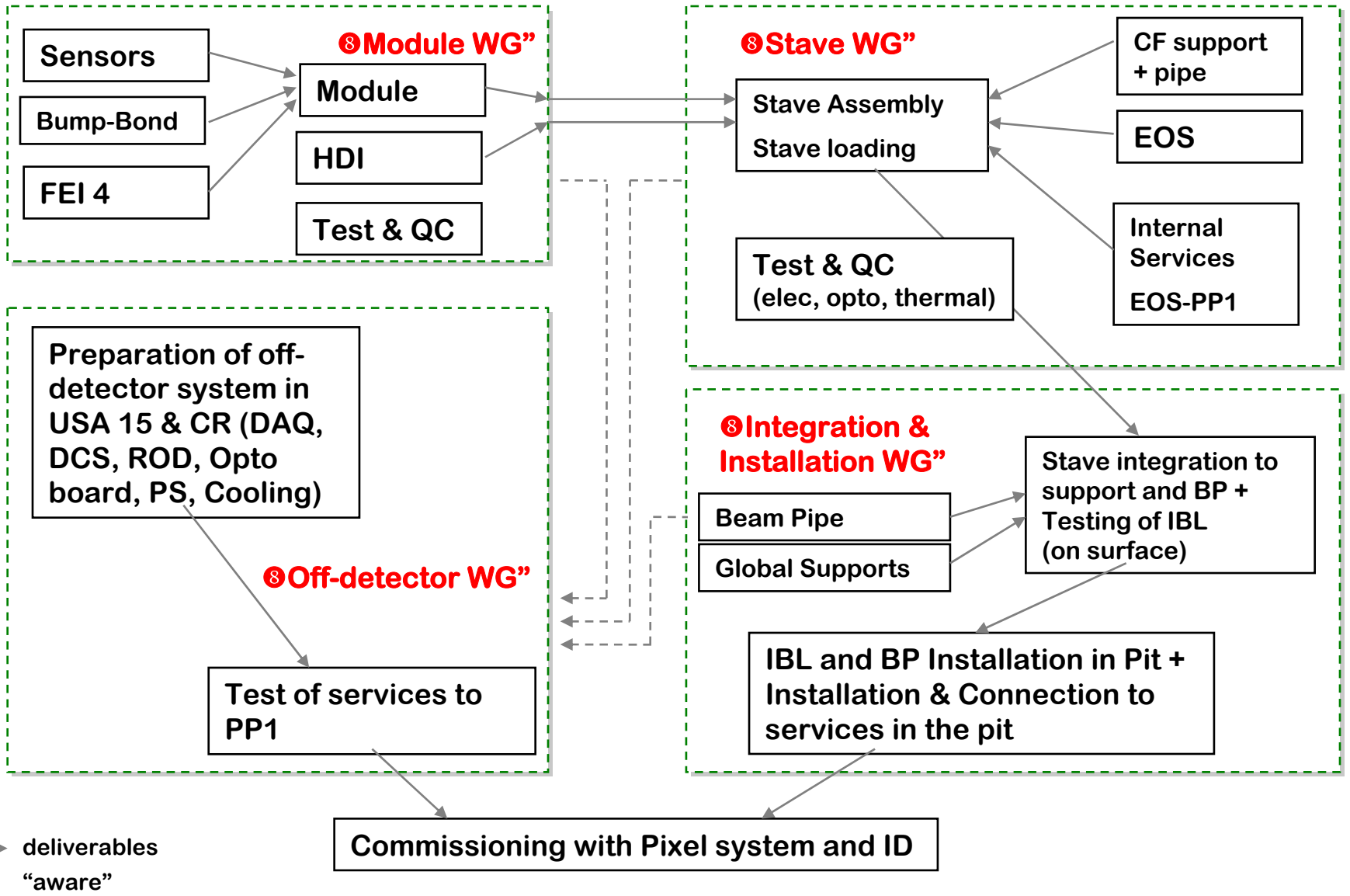


Summary

- The Insertable B-Layer will be a new, **4th pixel layer** to be added for the high-luminosity in the present ATLAS Pixel system
  - Smaller radius and lighter to further improve pixel performance
  - Compensate for gradual inefficiency of existing B-Layer
- The IBL is the **"technology" bridge to sLHC**
  - Its specification requires us to develop and use new technologies, which are directly relevant for sLHC
  - Construct a full detector system with those technologies on the time scale of 4-5 years
  - Development of Radiation hard **sensors**
  - New architecture and process for **Pixel Front-End** Chip
  - **Lighter Support** structures to minimize X0
  - More efficient **cooling**

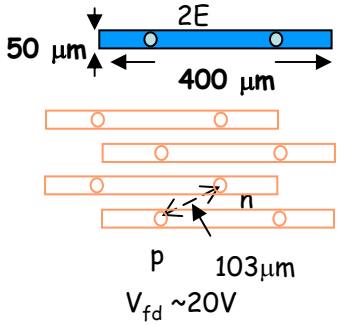
Backup slides

IBL assembly flow chart

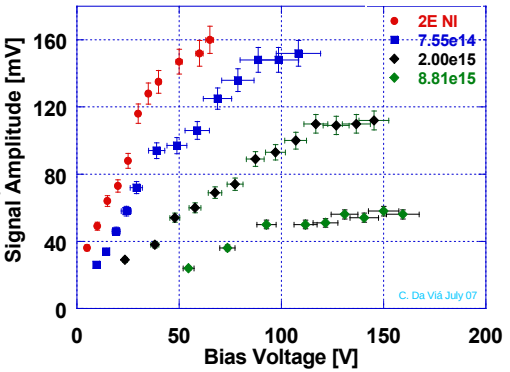


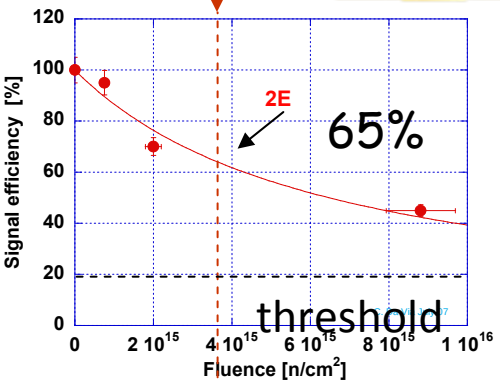
3D Radiation tolerance for the IBL

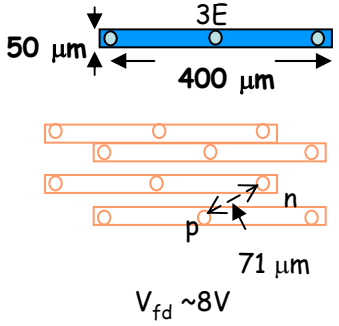
Irradiation and measurements performed in Prague
C. Da Viá, T. Slaviceck, V. Linhart, P. Bem, S. Parker,
S. Pospisil, S. Watts (process J. Hasi, C. Kenney)



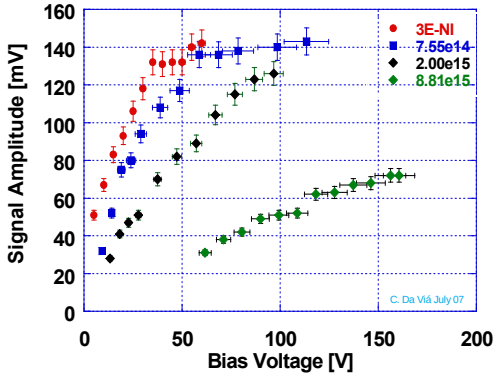
2E
13000e⁻
V_b~110V

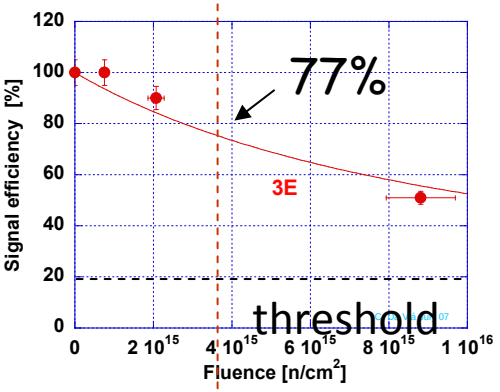


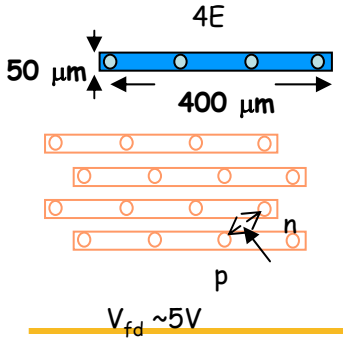




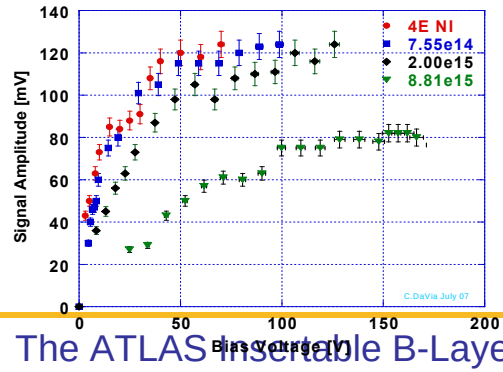
3E
15400e⁻
V_b~50V

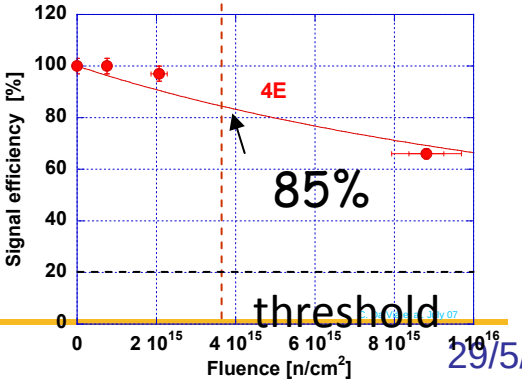






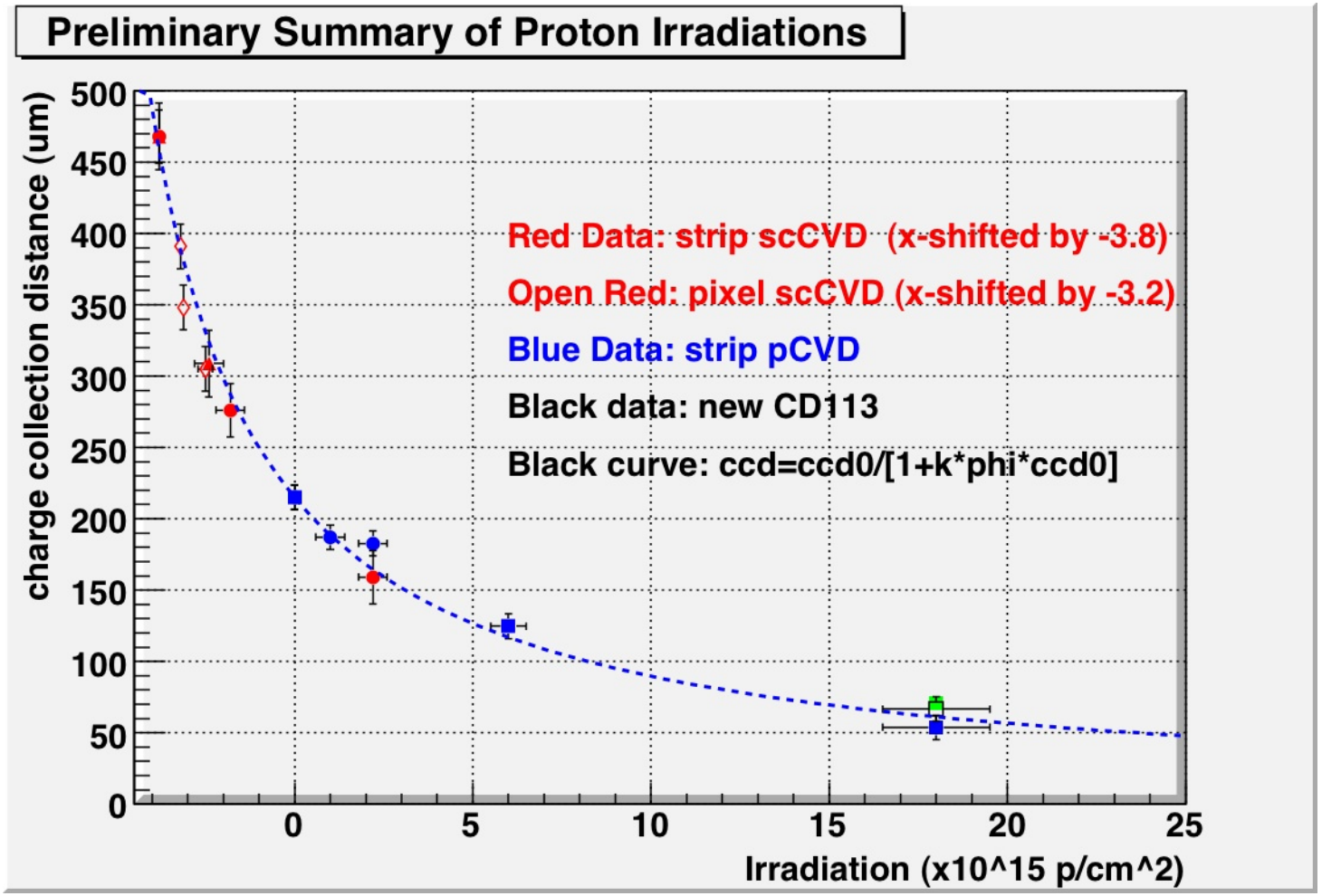
4E
17000e⁻
V_b~50V





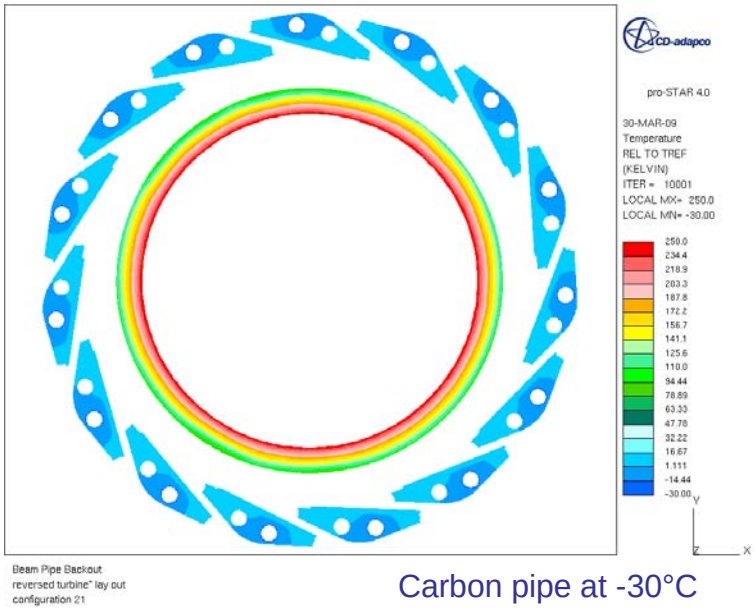
Proton Irradiation of Diamond

- From RD42 collaboration, H. Kagan



Beam Pipe Bakeout

- Beam pipe surface is heated up to 250C during backout
- Cooling failure during bakeout can pose serious risk to IBL modules
  - Investigate redundancy in stave cooling (I.e. 2 pipes supplied independently)



Carbon pipe at -30°C

	Tmax	Tmin
PIPE	8.2°C	-30°C
FOAM	9.4°C	-13.3°C
BUMP-BOUNDING	10°C	4.5°C
FE-CHIP	10.1°C	3.4°C
ADESIVE LAYER	10°C	0.4°C
SENSOR	9.9°C	4.6°C
AIR-GEL	250°C	77°C
NIDROGEN	121°C	-9.9°C