Silicon Vertex Detector Upgrade for the Belle II Experiment

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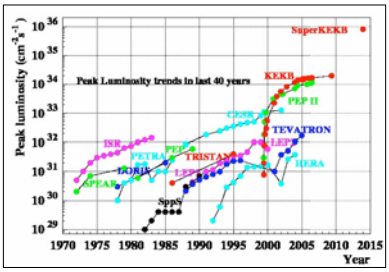
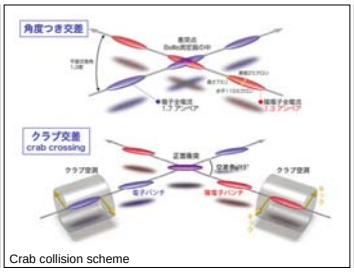
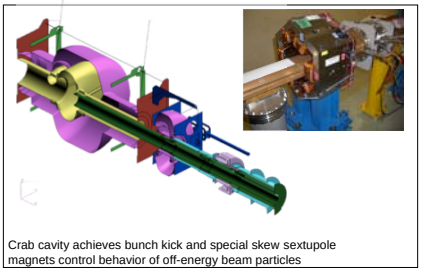
for the Belle SVD Group

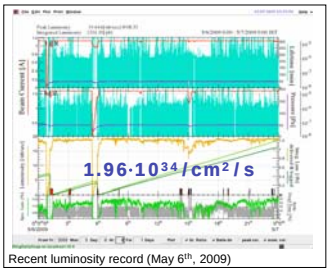
Extreme Luminosity Experiment at Υ(4S) Resonance: End of 2008 the international **Belle II Collaboration** was inaugurated with the purpose to extend the physics reach of the present Belle experiment. The improvement is based on the SuperKEKB accelerator upgrade with a target luminosity of $\mathbf{8{\cdot}10^{35}/cm^2/s}$. Belle detector will be upgraded accordingly so that efficient measurements will be possible at the highest luminosity. Thanks to functional crab crossing scheme in KEKB, which allows for head-on collisions, a record breaking $\mathbf{1.96{\cdot}10^{34}/cm^2/s}$ was already achieved in May 2008 (a factor of two higher than KEKB design).





Crab collision scheme


Crab cavity achieves bunch kick and special skew sextupole magnets control behavior of off-energy beam particles



Recent luminosity record (May 6th, 2009)

Physics at a Super B factory:
- **Precision measurements of CPV** in B decays
- Study of **time dependence of B^0 - anti-B^0 decays**
- Study of **rare decay modes** of beauty and charm hadrons and τ

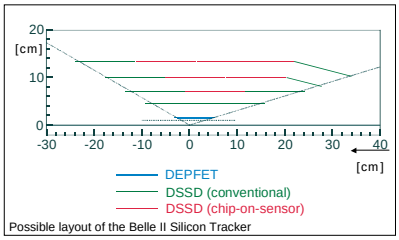
⇒

Design requirements for the Silicon Vertex Detector:
- Good resolution in the beam direction
- Small amount of material inside the acceptance region
- Operation at high radiation background rates and high track density (40 x present)

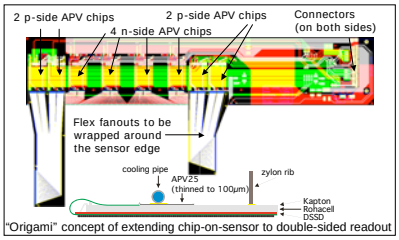
Two beam-beam collision variants under investigation: **High beam current** and **nano-beam size** at IP. Silicon tracker details will depend upon that choice.

Silicon tracker upgrade plan:
- **PXD - Pixel** Detector (2 inner layers) - high precision
- **SVD - Strip** Detector (4 outer layers) - larger acceptance

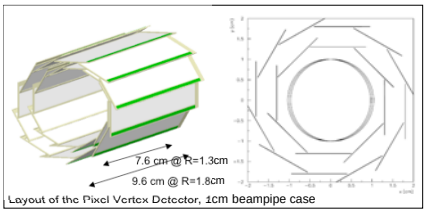
PXD Layout (based on DEPFET):
- Small radius, as close as possible to the beampipe (for 1.0cm BP case 1.3cm IL [8 modules] and 1.8cm OL [10 modules]) depending on IR
- High granularity sensors, pixel size about 50x75μm²
- Detector should be small, 20-24 single sensor modules in two layers
- Total of ~6Mpixel, frame readout rate <10μs
- Possibility of variable pixel in z pitch to optimize charge sharing at large z and improve resolution in the central part
- Sensor R&D (**DEPFET**, CAP, SOI), all technologically promising



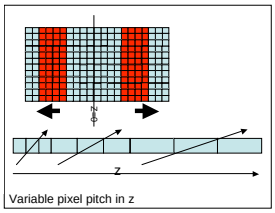
Possible layout of the Belle II Silicon Tracker



"Origami" concept of extending chip-on-sensor to double-sided readout



Layout of the Pixel Vertex Detector, 1cm beampipe case



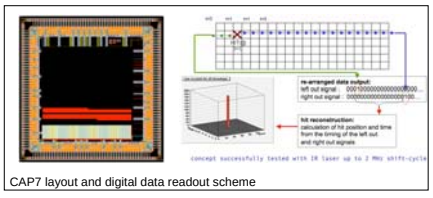
Variable pixel pitch in z

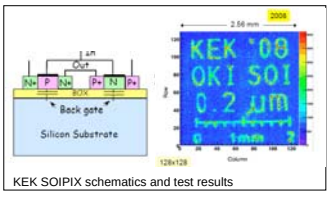
SVD Layout:
- System size 3-4 of the present Belle SVD2 (4 layers from ~3.8 to 14cm)
- Use of **DSSD sensors** from 6" wafer, well established technology
- Additional use of alternative "chip-on-sensor" sensor types (Lower number of readout chips, less material and power dissipation in acceptance region)
- Readout with **APV25** (~ 50ns shaping time, sensitive window ~160ns)+ FADC+COPPER (Full DAQ chain already successfully tested in a beam test at KEK)

Conceptually proven, after finalizing the geometry ready for production.

PXD Sensor R&D Status - 3 variants pursued:
- **CAP** (Continuous Acquisition Pixels) V1-7
  - -From basic technology studies to working pixel arrays
  - -Testing of digital readout CAP7 in 0.2μm OKI SOI (35x50 μm² pixel cell, 60k pixels, 3x3mm² active area)
- **KEK SOIPIX**
  - -Latest prototype in 0.2μm OKI SOI, successful tests with x-rays
  - -Works, but problems due to back-gate-effect, plans to reduce it
  - -LBNL beam tests - best S/N (15) at U=10V, gets worse at higher U (no full depletion)

Both offer very promising concepts for the future, however still at basic R&D

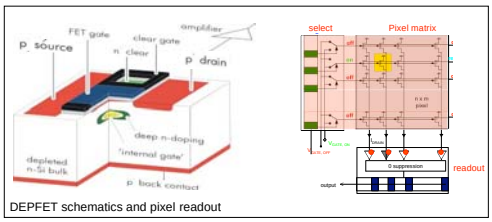

CAP7 layout and digital data readout scheme



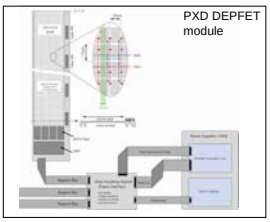
KEK SOIPIX schematics and test results

- **DEPFET**
  - -Each pixel is a p-channel FET on a completely depleted bulk, deep n-implant creates a potential minimum for electrons under the gate; 50 x (75-115) mm² pixels
  - -Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e⁻), accumulated charge removed by a clear contact ("reset")
  - -Frame readout time <10μs, sequential readout of pixels or rows (line readout time 80ns, 2x4 lines per readout step)
  - -Low power (only few pixels active), ASICs at the periphery

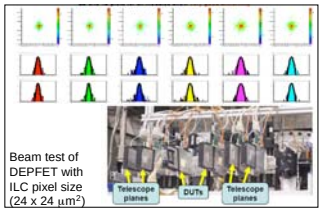
Most promising candidate - Evolving from basic R&D to production for Belle II !



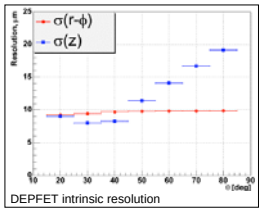
DEPFET schematics and pixel readout



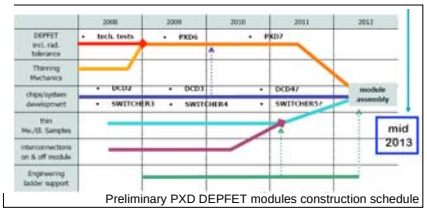
DEPFET testing, plans and open questions:
-Beam tests at DESY (<6 GeV) and CERN (180 GeV)
-Latest setup: 6 DEPFET array acting as telescope & DUT (20 M events taken)
-Radiation hardness:DEPFET works after 80kGy with low noise, large (operation mode dependent) threshold voltage shift & dispersion, annealing helps
-GEANT4 simulation started, tuned to beam test data
-Solve radiation related issues (try thinner oxides, optimization of nitride/oxide thicknesses)
-Start considering mechanics/cooling design, which strongly depends on IR design (fixed at latest mid 2010)
-DAQ interface (PXD may deliver up to 70Gbit/s)



Beam test of DEPFET with ILC pixel size (24 x 24 μm²)



DEPFET intrinsic resolution



Preliminary PXD DEPFET modules construction schedule