Silicon Vertex Detector Upgrade for the Belle II Experiment

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for the Belle SVD Group

Extreme Luminosity Experiment at Y(4S) Resonance: End of 2008 the international Belle II Collaboration was inaugurated with the purpose to extend the physics reach of the present Belle experiment. The improvement is based on the SuperKEKB accelerator upgrade with a target luminosity of 8x10^{33}/cm^2/s. Belle detector will be upgraded accordingly so that efficient measurements will be possible at the highest luminosity. Thanks to functional crab crossing scheme in KEKB, which allows for head-on collisions, a record breaking 1.96x10^{34}/cm^2/s was already achieved in May 2008 (a factor of two higher than KEKB design).

Physics at a Super B factory:
- Precision measurements of CPV in B decays
- Study of rare decay modes of beauty and charm hadrons and τ
design requirements for the Silicon Vertex Detector:
- Good resolution in the beam direction
- Small amount of material inside the acceptance region
- Operation at high radiation background rates and high track density (40 x present)

Two beam-beam collision variants under investigation: High beam current and nano-beam size at IP. Silicon tracker details will depend upon that choice.

SVD Layout:
- System size 3-4 of the present Belle SVD2 (4 layers from ~3.8 to 14cm)
- Use of DSSD sensors from 6” wafer, well established technology
- Additional use of alternative “chip-on-sensor” sensor types (Lower number of readout chips, less material and power dissipation in acceptance region)
- Readout with APV25 (~ 50ns shaping time, sensitive window ~160ns), FADC+COPPER
- Full DAQ chain already successfully tested in a beam test at KEK

Conceptually proven, after finalizing the geometry ready for production.

Most promising candidate: Evolving from basic R&D to production for Belle II !

PXD Sensor R&D Status - 3 variants pursued:
- CAP (Continuous Acquisition Pixels) V1-7
- DEPFET schematics and pixel readout
- DSSD (conventional)
- DSSD (chip-on-sensor)

Possible layout of the Belle II Silicon Tracker

Silicon tracker upgrade plan:
- PXD - Pixel Detector (2 inner layers) - high precision
- SVD - Strip Detector (4 outer layers) - larger acceptance

PXD Layout (based on DEPFET):
- Small radius, as close as possible to the beampipe (for 1.0cm BP case 1.3cm IL [8 modules] and 1.8cm OL [10 modules]) depending on IR
- High granularity sensors, pixel size about 50x75μm
- Detector should be small, 20-24 single sensor modules in two layers
- Total of ~6Mpixel, frame readout rate <10^10 events/s
- Detector should be small, 20-24 single sensor modules in two layers
- Sensor R&D (DEPFET, CAP, SOI), all technologically promising

DEPFET schematics and pixel readout

APV25

Variable pixel pitch in z

APV25

Flex fanouts to be wrapped around the sensor edge

CAP layout and digital data readout scheme

DEPFET testing, plans and open questions:
- Beam tests at DESY (<=6 GeV) and CERN (180 GeV)
- Latest setup: 6 DEPFET array acting as telescope & DUT (20 M events taken)
- Radiation hardness:DEPFET works after 80Gy with low noise, large (operation mode dependent) threshold voltage shift & dispersion, annealing helps
- GINTRA simulation started, tuned to beam test data
- Solve radiation related issues (try thinner oxides, optimization of nitride/oxide thicknesses)
- Start considering mechanics/cooling design, which strongly depends on IR design (fixed at latest mid 2010)
- DAQ interface (PXD may deliver up to 70Gb/s)

Layout of the Pixel Vertex Detector, 1cm beampipe case

High granularity sensors, pixel size about 50x75μm

7.6 cm @ R=1.3cm

1.3 cm IL [8 modules] and 1.8cm OL [10 modules]) depending on IR

9.6 cm @ R=1.8cm

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