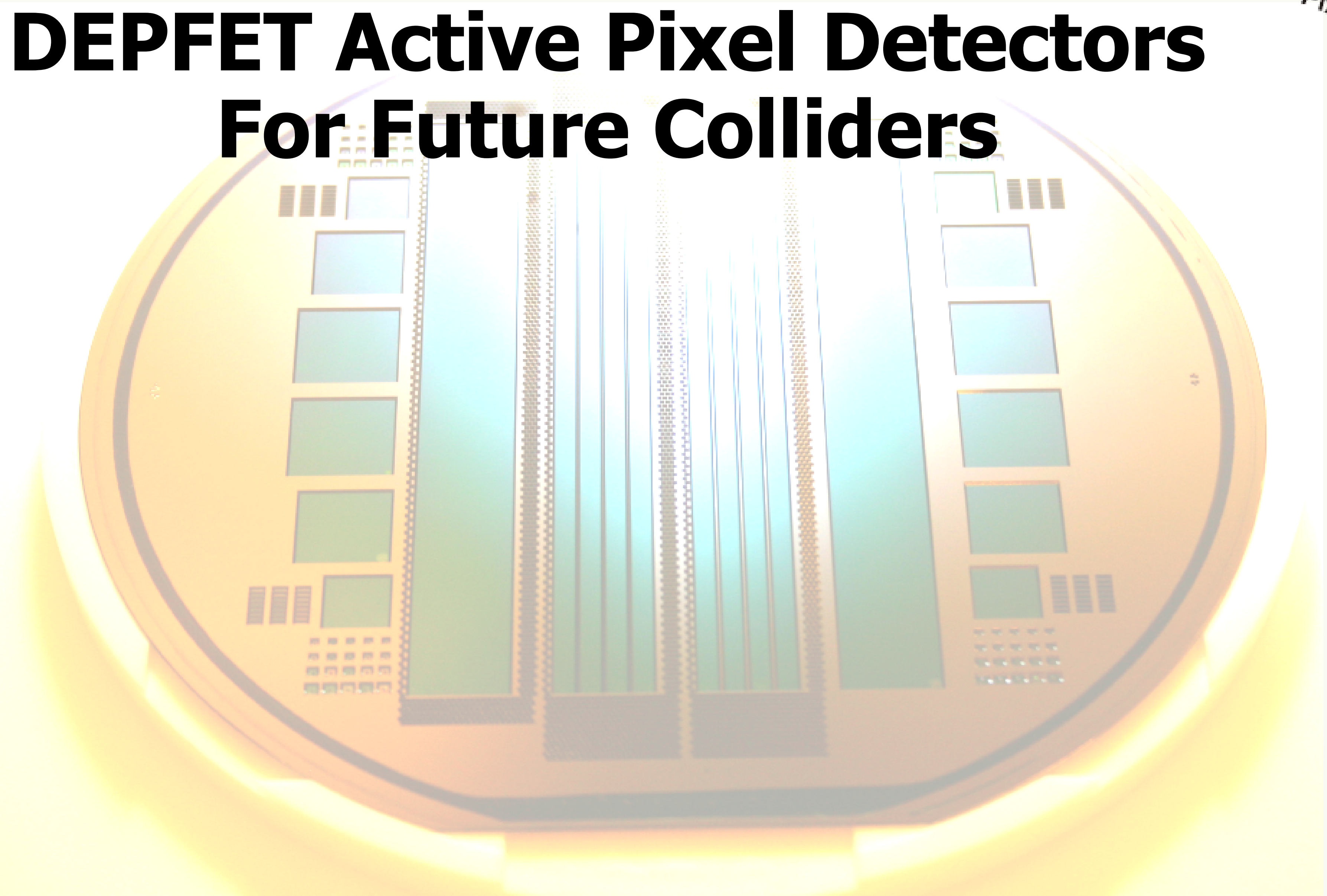
DEPFET Active Pixel Detectors For Future Colliders



DEPFET is also a collaboration

(www.depfet.org)

- ✔ DEPFET is also an international collaboration.
- ✔ 12 research institutes and universities
- ✔ Working to build with the DEPFET sensors developed at the HLL MPI a system suitable for the vertex detectors in the coming e^+e^- colliders.

Universität Karlsruhe (TH)
Research University • founded 1825

MAX-PLANCK-GESELLSCHAFT

mpi halbleiterlabor

UNIVERSITAT DE BARCELONA

The Henryk Niewodniczański Institute of Nuclear Physics Polish Academy of Sciences

GEORG-AUGUST-UNIVERSITÄT GÖTTINGEN

universitätbonn

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Heidelberg University

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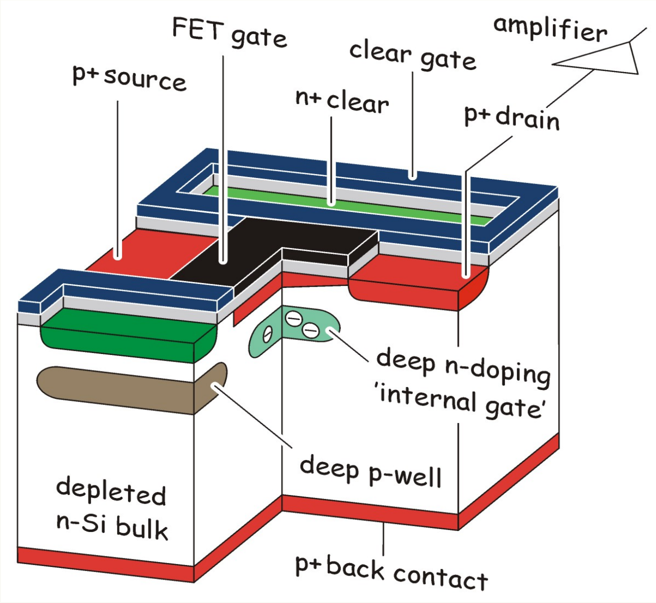
Introduction

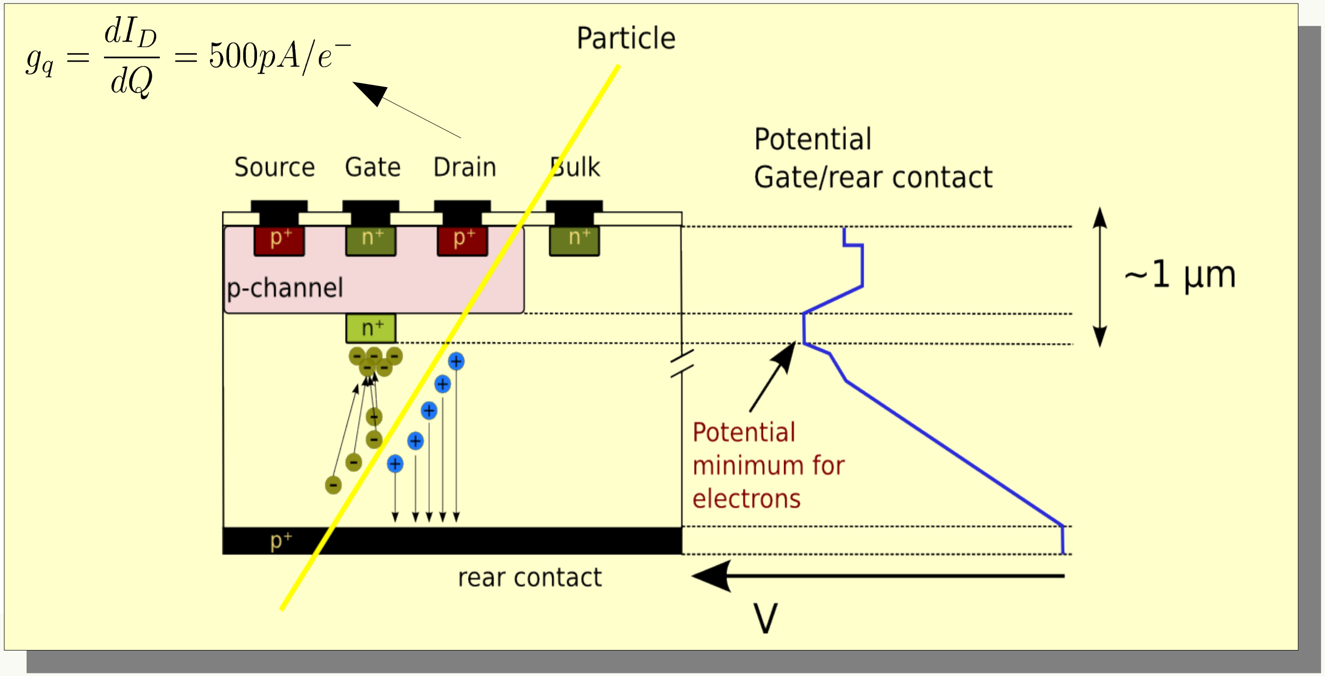
- ✔ Next generation of e^+e^- colliders require new pixel detector concepts that
  - ➔ Provide very good spatial resolution,
  - ➔ Can cope with a considerable amount of background and
  - ➔ Keep the material budget as low as possible to minimize the effect of multiple scattering.
    - ➘ Active cooling "forbidden" in sensitive area
- ✔ DEPFET (DEPleted Field Effect Transistor) is a very good candidate technology
  - ➔ DEPFET is the baseline technology for Belle II upgrade and
  - ➔ Competes with other technologies for the Future Linear Collider

	ILC	**Belle II**
Occupancy	0.13 hits/μm²/sec	0.4 hits/μm²/sec
Radiation	<100 kRad/year	> 1Mrad/year
Power Duty Factor	1/200	1
Frame time	25-100 μs	10 μs
	Large momemtum range Required IP res. 3-5 μm Small pixels: 25x25 μm2 Low material budget: 0.1X0 -> Thickness: 50 μm	Low (<1GeV/c) mom. tracks IP res. dominated by MS (~9μm) Pixels can be larger: 50x70 μm2 Low material budget: 0.15 X0 -> Thickness: 50 μm

The DEPFET concept

- The key concept: the integration of amplifying transistors in a fully depleted bulk
  - Charge carriers drift due to the electric field (fast)
  - Large signal
- By means of sidewards depletion and an n-implant a potential minimum for electrons (the internal gate) is created under the transistor channel
  - Electrons drift to the internal gate where they are stored
  - Readout on demand
- The charge in the internal gate modulates the channel current in the transistor
  - When a voltage is applied to the gate, the current change in the drain is proportional to the charge (g_q – internal amplification)
  - When the ***transistor is off***, there is no current (no power consumption) but ***the detector is still sensitive***





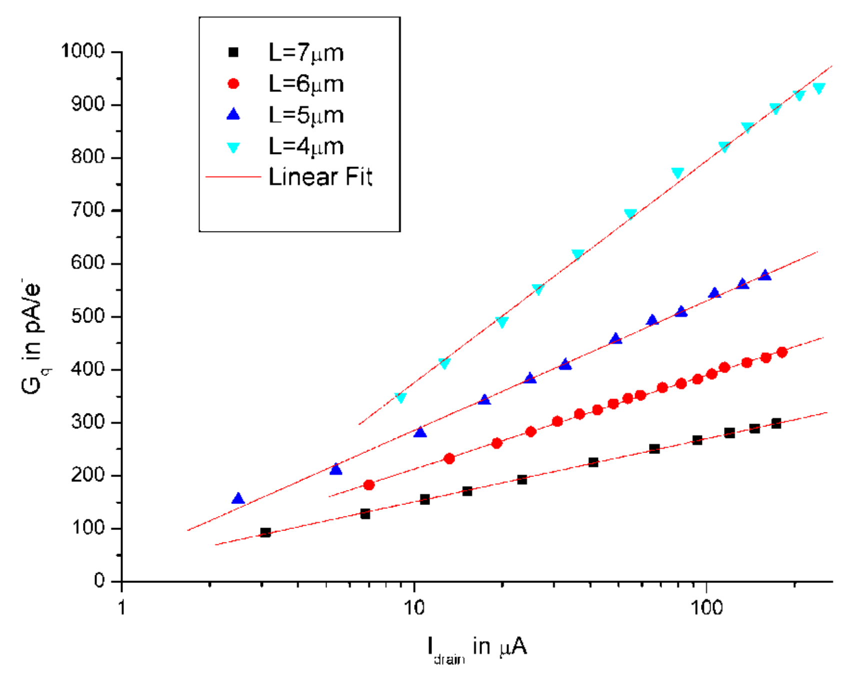
$$g_q = \frac{dI_D}{dQ} = 500pA/e^-$$

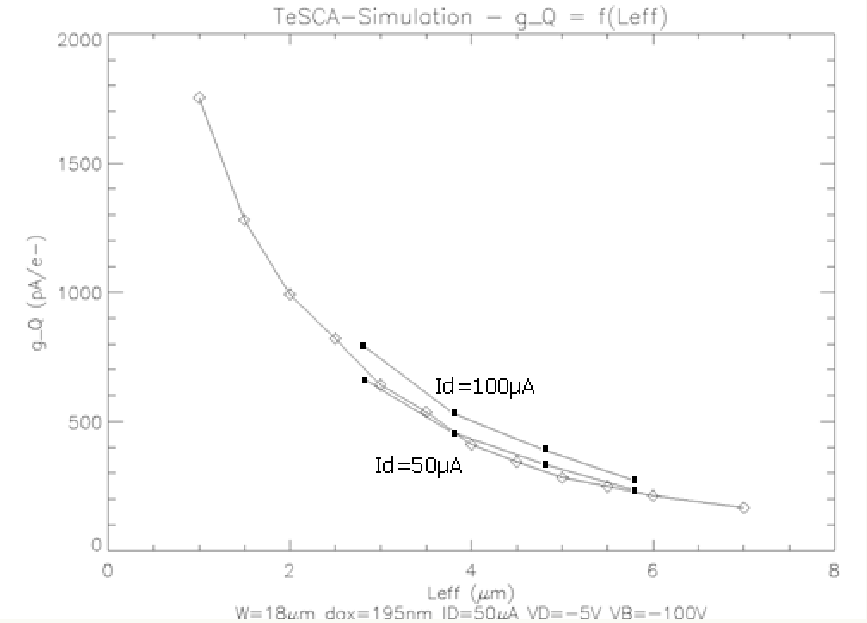
Internal Amplification

- ✔ The internal amplification measures the change in drain current in the presence of charge in the internal gate:

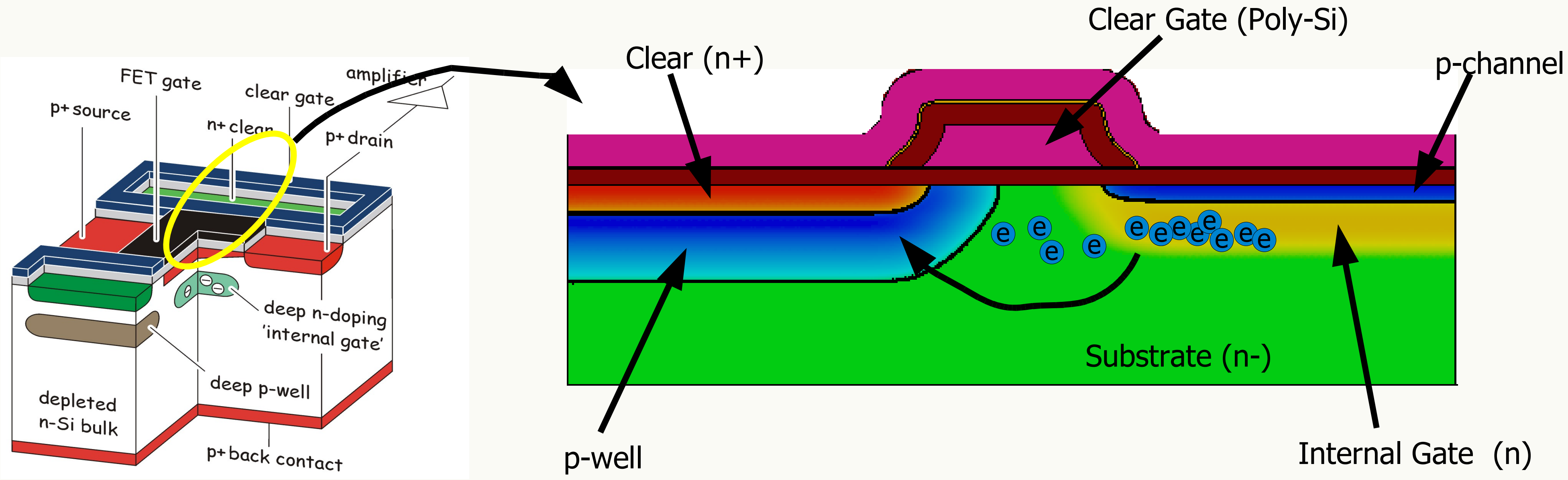
$$g_q = \frac{dI_{ds}}{dQ_{int}} \sim \frac{\sqrt{I_{ds}}}{\sqrt{W L^{\frac{3}{2}}}}$$

- ✔ For an input noise with an equivalent current noise of σ the contribution to the ENC is σ / q_q
  - ➔ Increasing g_q increases SNR, if the electronics is the dominant noise
- ✔ Playing with channel length we can achieve up to g_q ~ 1 nA/e^-



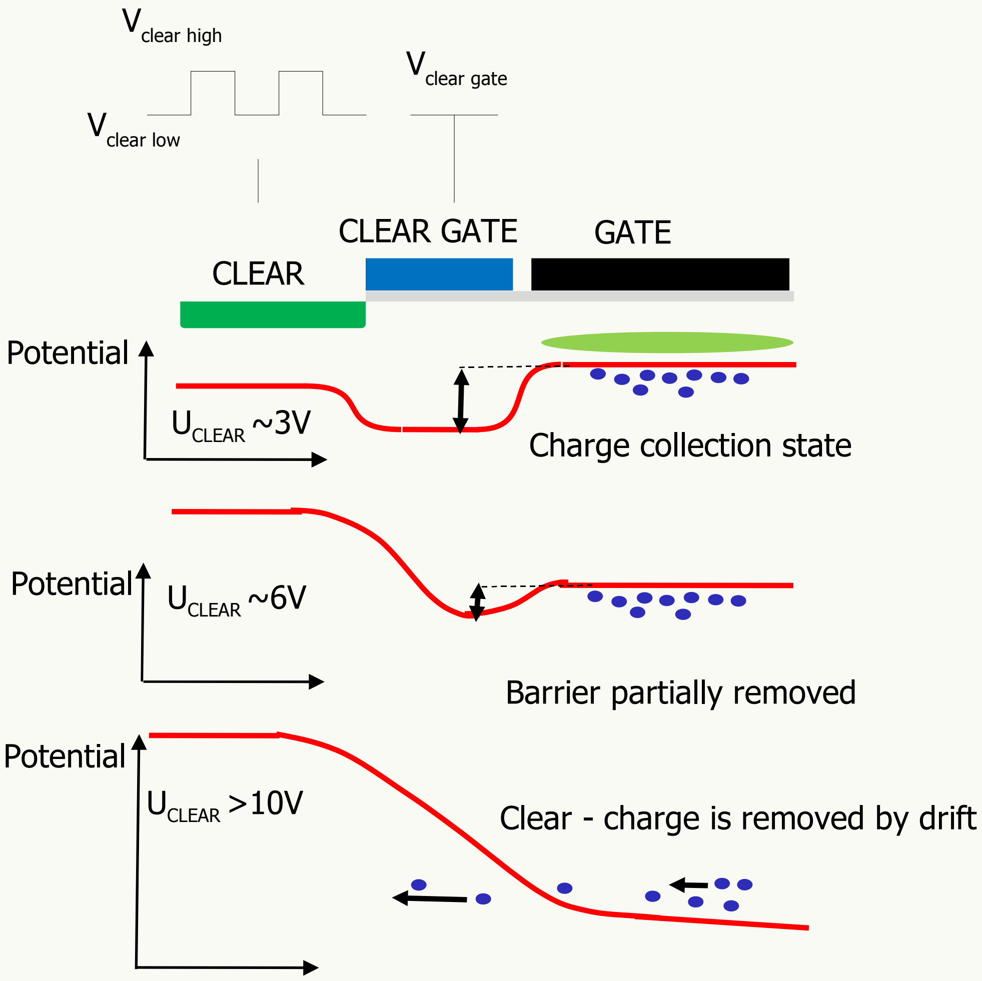


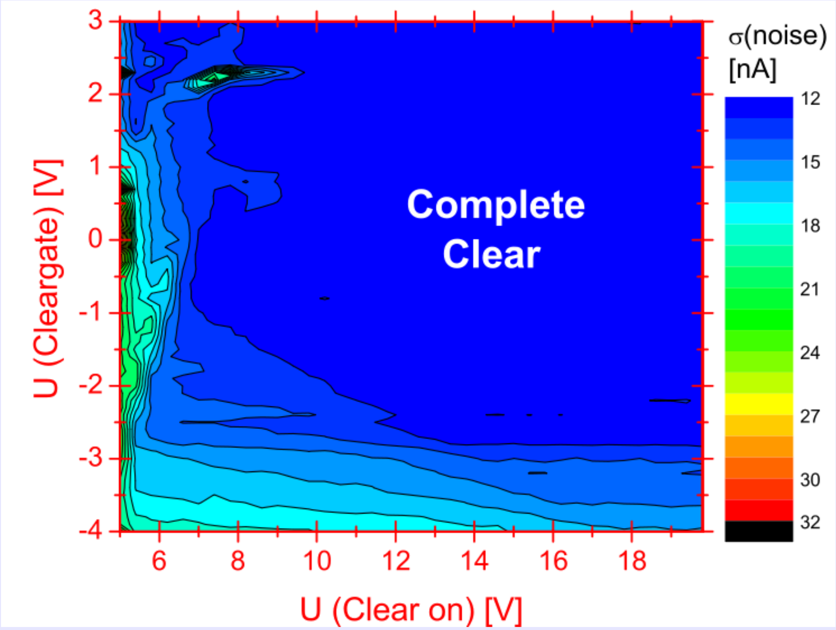
The Clear Mechanism



- ✔ Charge is stored in the internal gate until we remove it
- ✔ Charge removal is done by means of a lateral field that makes the charges drift away from the internal gate to the clear.
- ✔ Clear is shielded by a p-well to avoid charge looses
  - ➔ This creates a potential barrier than hinders the clear process
- ✔ A Clear Gate structure added to overcome this barrier as well as the potential of the substrate around the internal gate

The Clear Mechanism





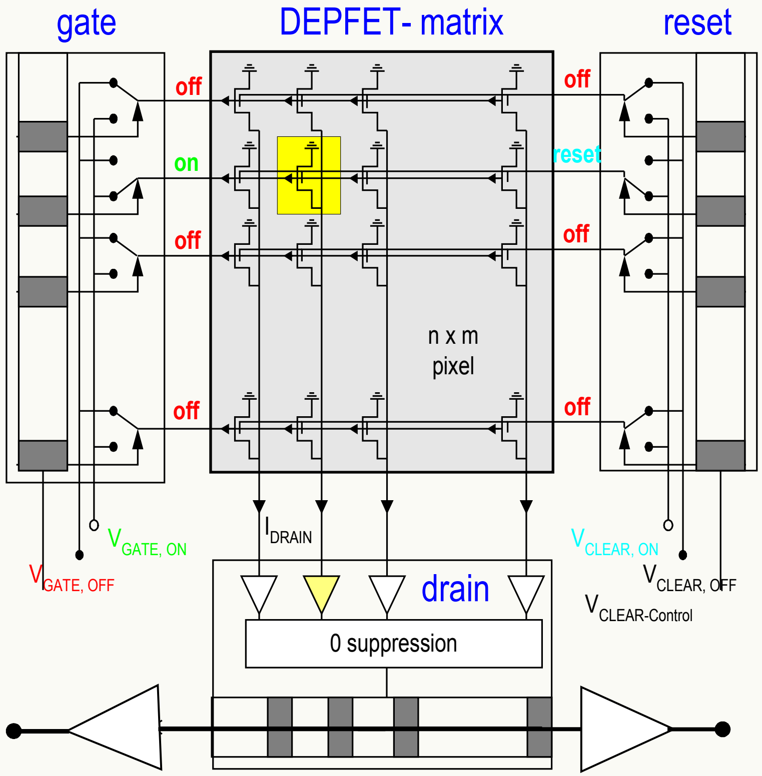
If clear is not complete we have reset noise in the pedestal current

When clear is complete, the reset noise vanishes and the measured pedestal current spread is minimal.

We can achieve a complete clear with V_{clear} ~ 10V and a wide range of $V_{clear\ gate}$ values.

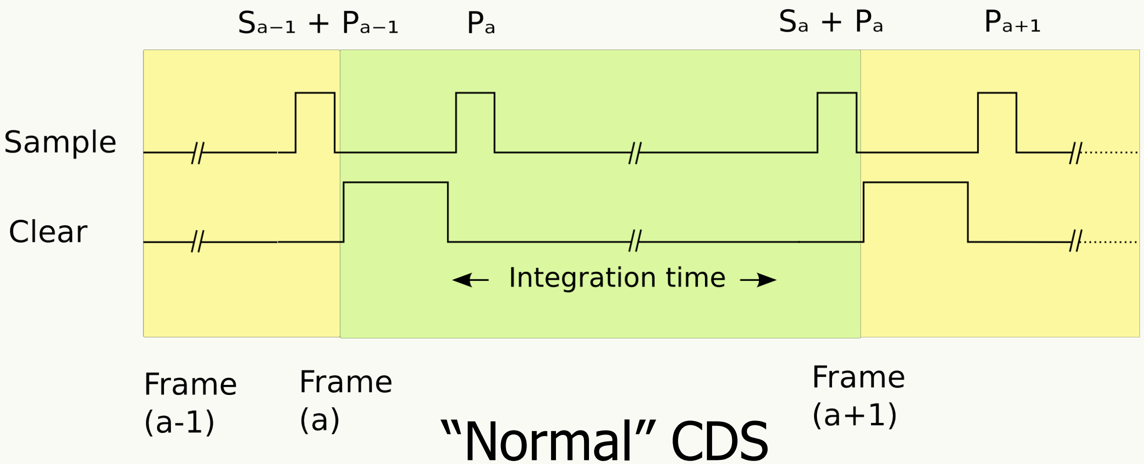
Pixel array for Future e^+e^- colliders

- We read a DEPFET pixel array in “rolling shutter” mode.
  - Select row with external gate
  - Read out data
  - Select next row and repeat
- Besides the readout chip, we need two additional steering chips to provide
  - the Gate voltage to activate the pixels to be readout in the active row
  - The Clear voltage to remove the charge from the internal gate on those pixels
- We read the current from the drain.
  - Drain is kept at a constant potential by an input cascode
  - Faster
- While reading one row all the other pixels are in “OFF” state
  - No power consumption
  - Still collecting charge

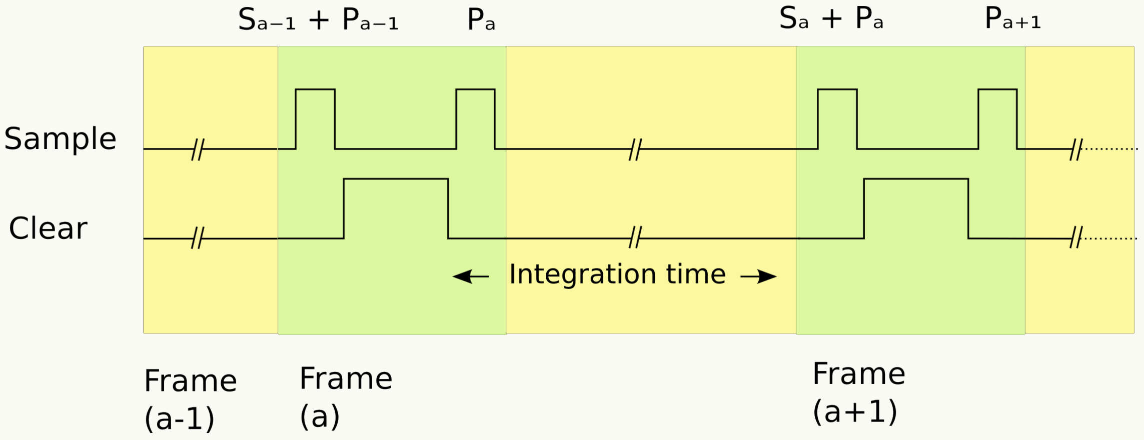


See H. Krüger talk for details on the electronics

The readout sequence



“Normal” CDS



DEPFET CDS

- CDS (Correlated Double Sampling)
- Usually: Signal = $(S_a + P_a) - P_a$
- If there is complete clear and, therefore, no reset noise then ($P_{a-1} = P_a$)
- DEPFET: Signal = $(S_{a-1} + P_{a-1}) - P_a$
- We do not need to store the “pedestal frame” during the CDS

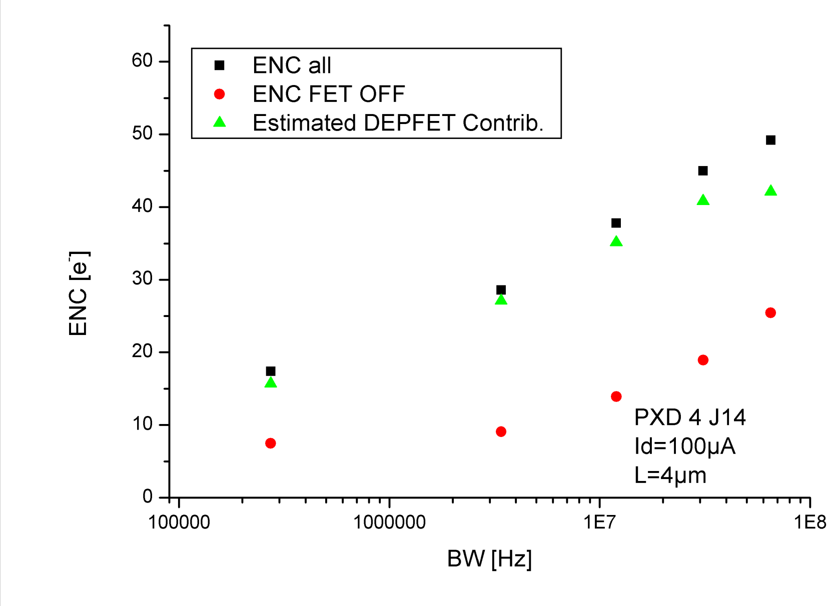
High Speed Operation Performance

High Speed readout

High bandwidth
Short shaping times
Thermal Noise ~ $\tau^{-1/2}$

Measurement of a single pixel shown below
Intrinsinc DEPFET noise small enough

ENC ~40-50 e^- @ τ=20ns (50 MHz)
Signal (50 µm) : 4000 e^- -> S/N ~ 80-100

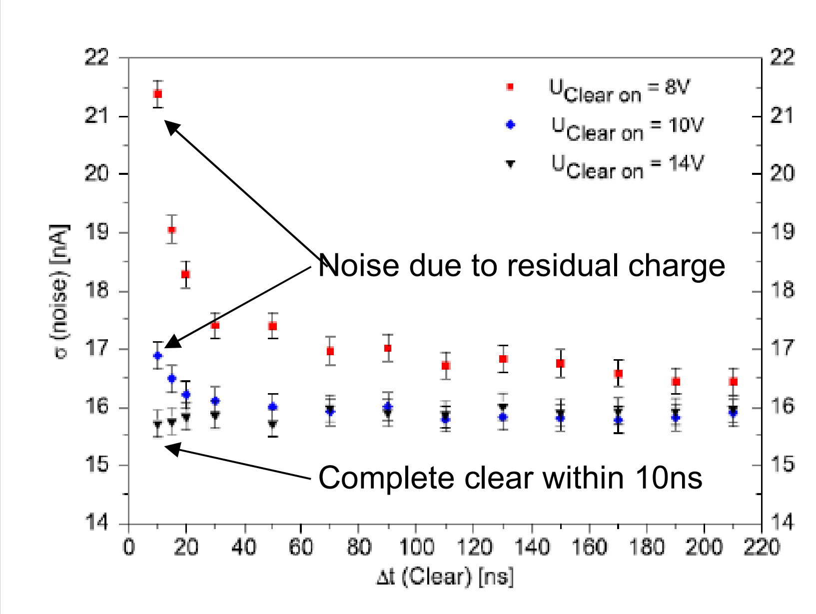


Fast Clear

Needed for high speed operation
Complete clear achievable in ~10ns

Again, pedestal current spread shown as a function of time.

Full clear happens when the spread is minimal.



“Timing”

Pixel row
n -1 active

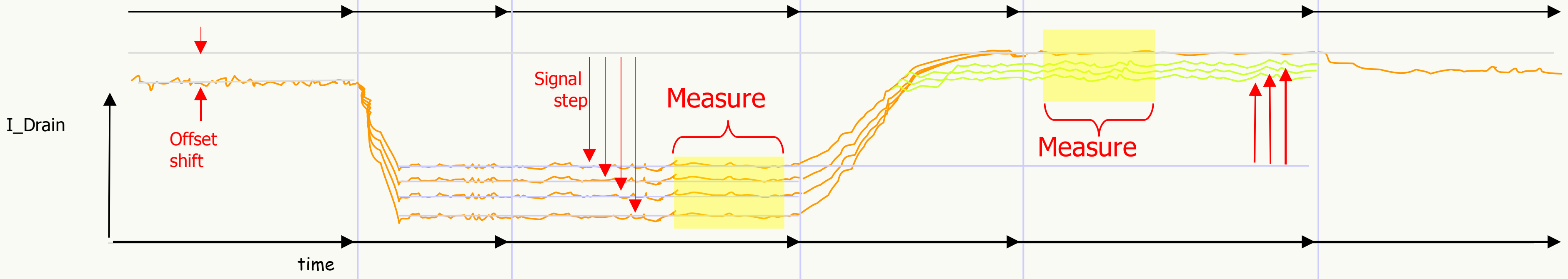
Switch to
row # n

„Signal“ sampling
in row # n

Clear process

„Baseline“ sampling
in row # n

Switch to
row # n +1



„empty“ level
pixel row # n -1

settling
process

„signal“ level
pixel row # n
depends on integrated
charge

pixel returns
to empty level
= reference level

„empty“ level
pixel row # n -1
stable reference if clear
complete

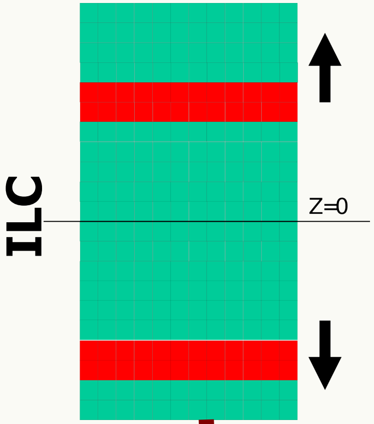
incomplete clear
introduces additional noise

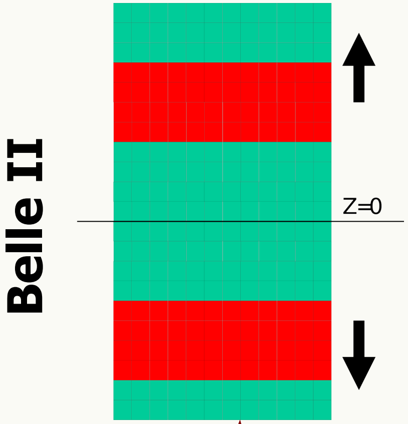
~80-100 ns

The sample-clear-sample cycle can be accomplished in ~80-100ns.
The time to read one frame (all rows in the array) depends on the number of cycles needed

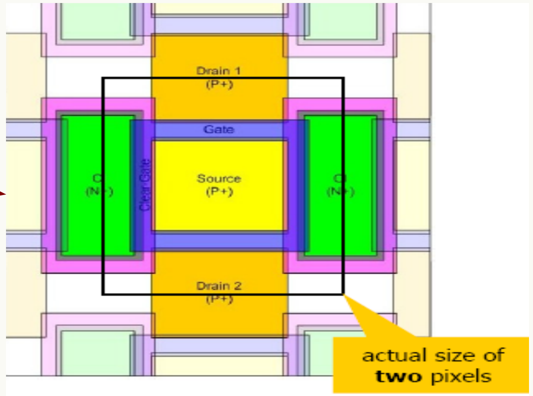
“Timing”

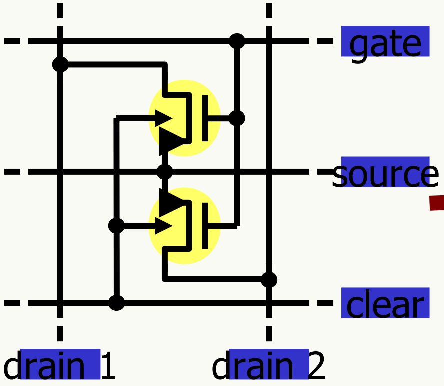
- To minimize the frame time we should reduce the number of sample-clear-sample cycles
  - Split the frame readout in 2 sides
  - Activate more than one row at a time
    - This increases the number of readout channels
    - ILC module activates 2 rows at a time
    - Belle II module activate 4 rows at a time





Pixel size:
25x25 µm



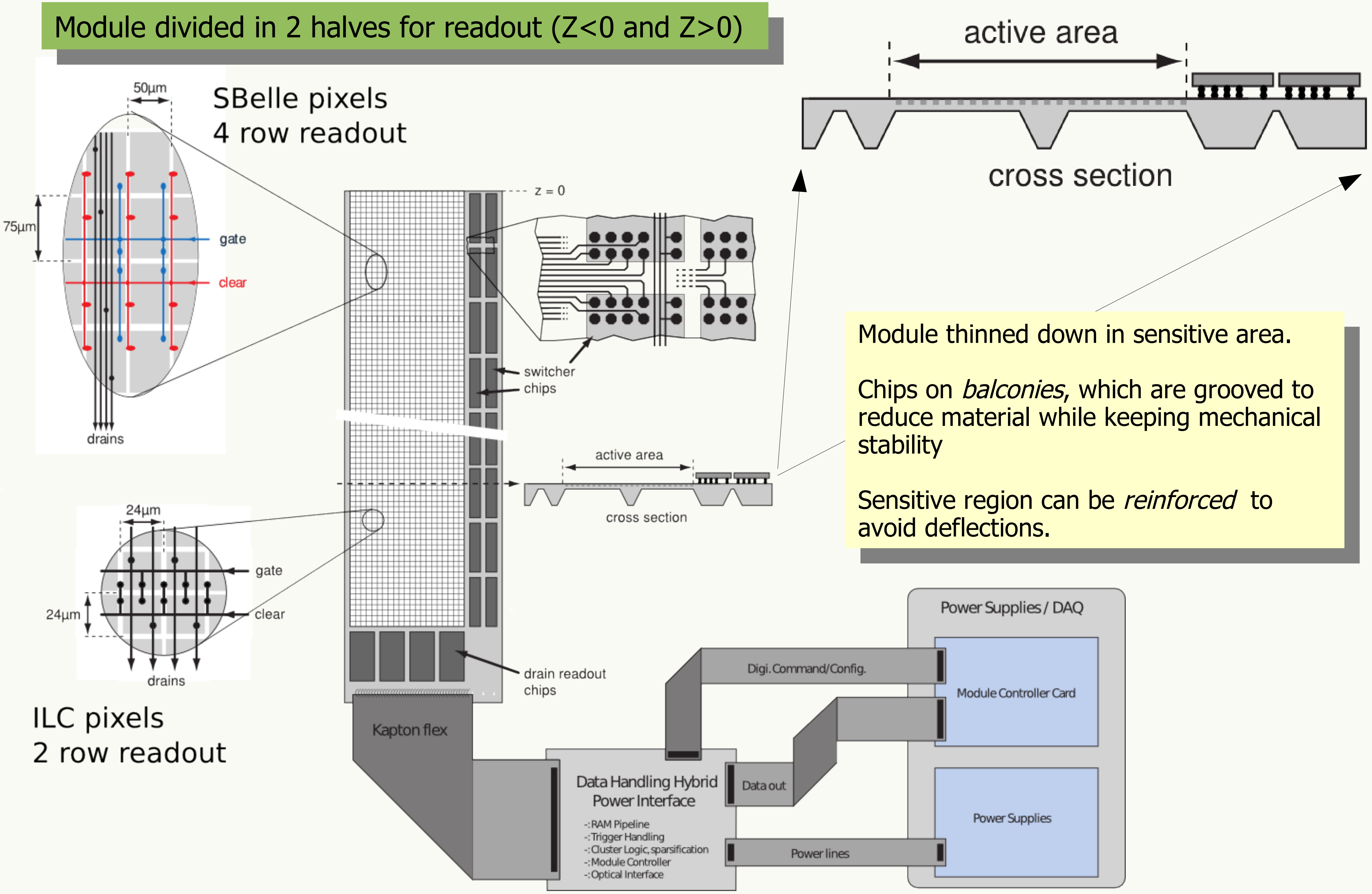


Pixel size:
50x70 µm

Can accommodate
More column lines

The module

Module divided in 2 halves for readout (Z<0 and Z>0)



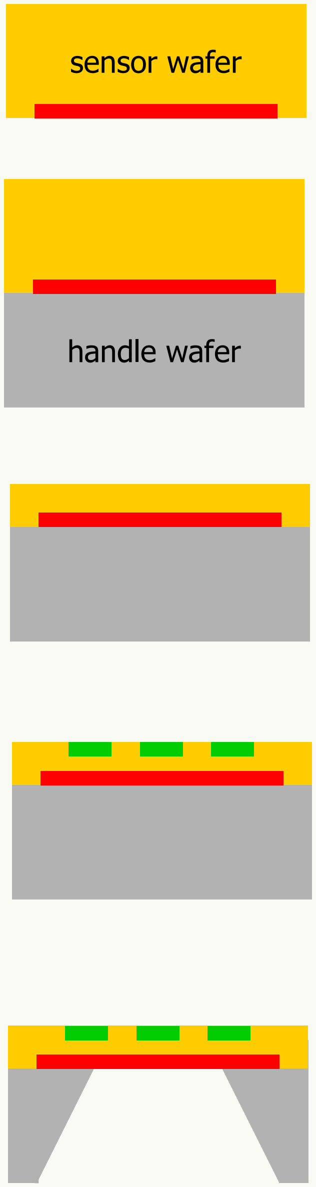
Module thinned down in sensitive area.

Chips on *balconies*, which are grooved to reduce material while keeping mechanical stability

Sensitive region can be *reinforced* to avoid deflections.

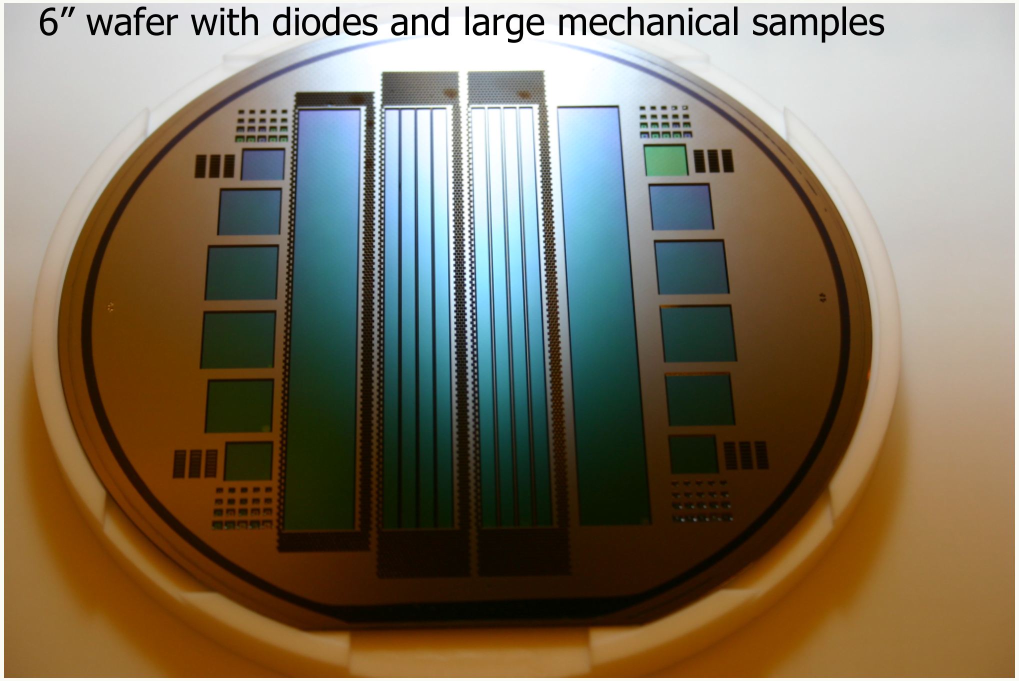
Wafer thinning

1) Process backside of thick detector wafer (structured) implant.
2) Bond detector wafer on handle wafer.
3) Thin detector wafer to desired thickness (grinding & etching).
4) Process front side of the detector wafer in a standard (single sided) process line.
5) Etch handle wafer.
   If necessary: add Al-contacts
   Leave frame for stiffening and handling

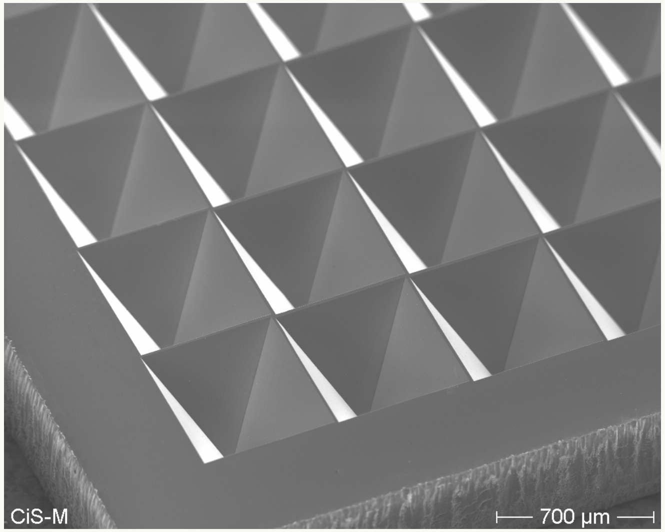


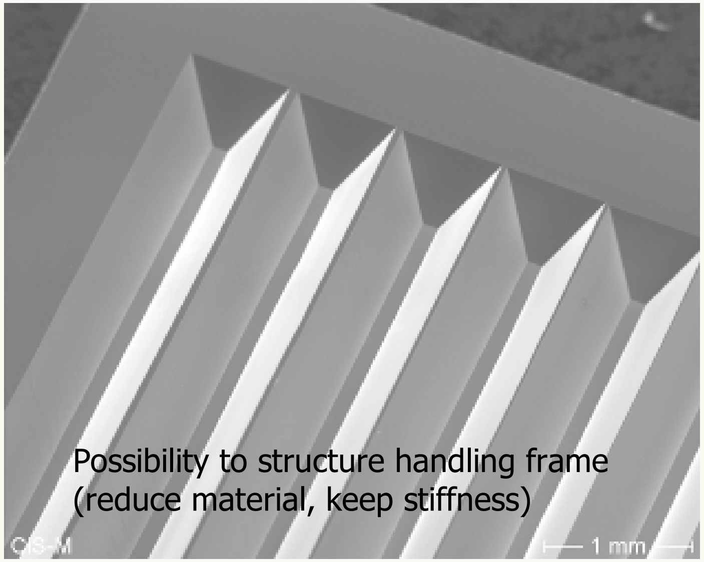
All Silicon module

Wafer Thinning

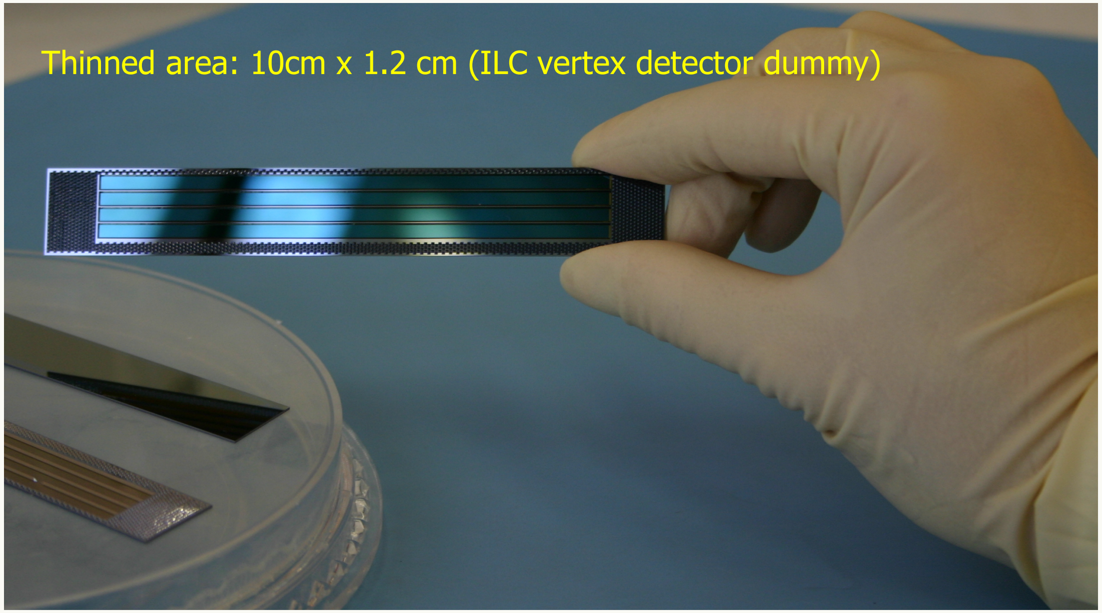


6” wafer with diodes and large mechanical samples





Possibility to structure handling frame (reduce material, keep stiffness)

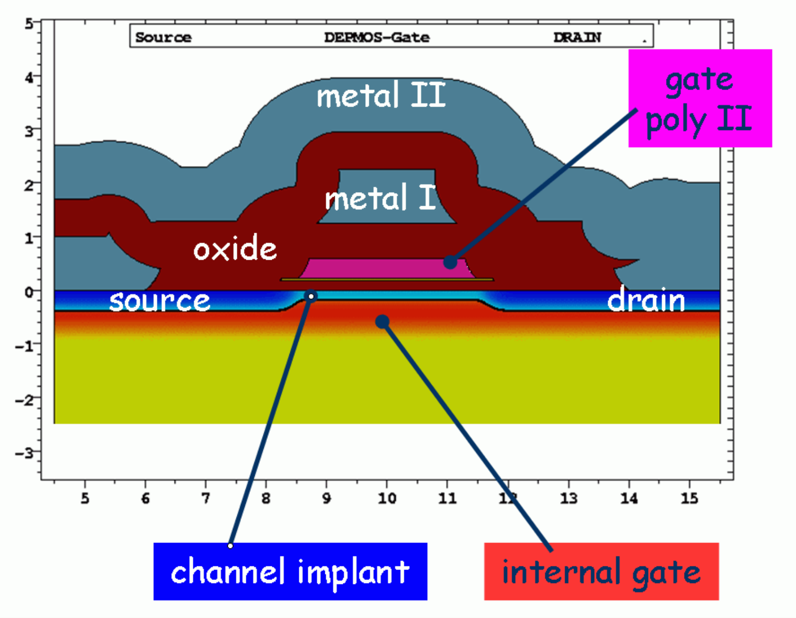


Thinned area: 10cm x 1.2 cm (ILC vertex detector dummy)

Irradiations

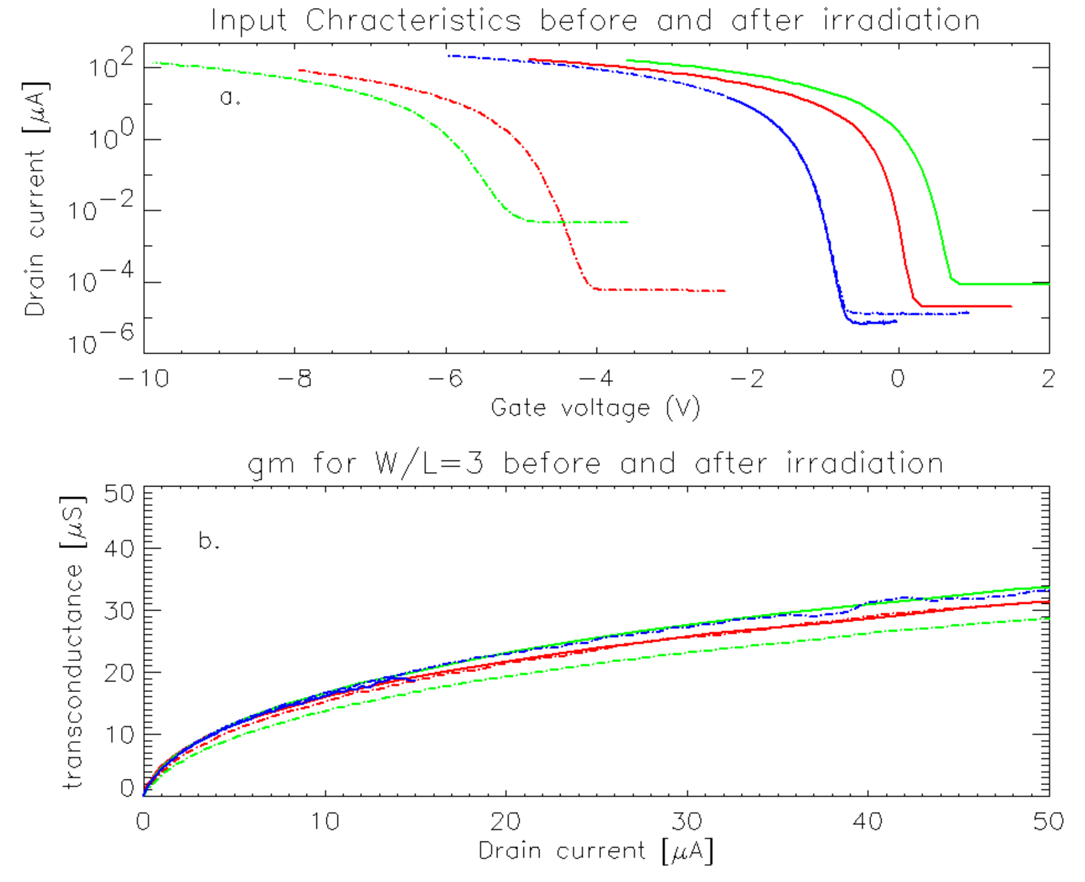
- ✔ Non ionizing Energy Loss (NIEL)
  - ➔ Leakage current increase -> shot noise
  - ➔ Trapping not critical for the expected doses
- ✔ Ionizing radiation – Total Ionizing dose (TID)
  - ➔ 2 MOS gates (Gate, Clear Gate)...
  - ➔ Fixed oxide positive charge -> ΔV_T
  - ➔ Interface trap density
    - ➘ Reduced mobility (g_m)
    - ➘ Higher 1/f noise

Gate Dielectrics: ~ 200nm



	PXD4-10 MO2	PXD4-5 M05	PXD4-2 J14
Type	Protons, 30MeV	Neutrons, 1-20MeV	Gammas - ^{60}Co
Fluence / Dose	$1.2 \cdot 10^{12}$ p/cm²	$1.6 \cdot 10^{11}$ n/cm²	913kRad
1MeV n equivalent	$3 \cdot 10^{12}$ n_{eq}/cm²	$2.4 \cdot 10^{11}$ n_{eq}/cm²	n/a

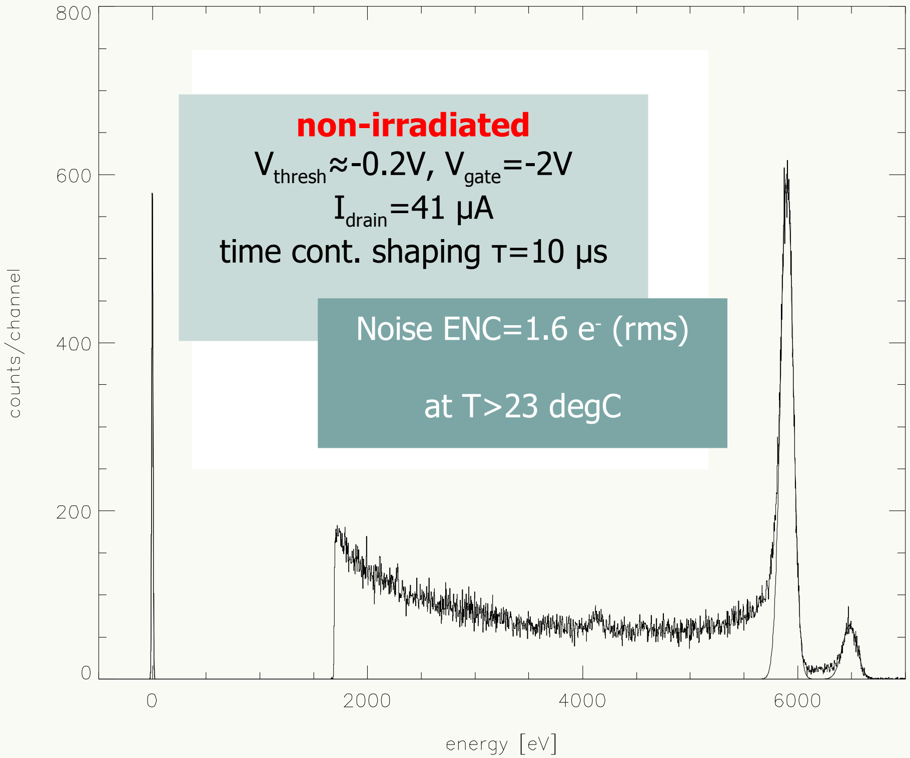
Basic par.: ΔV_T, g_m, I_{leak}



irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4x10^{11} n/cm^2	~ 0	unchanged	1.4 pA
proton	283krad / 3x10^{12} n/cm^2	~-5V	~ -15%	26 pA

(*) 5..22 fA non irrad.

Spectroscopic performance



non-irradiated

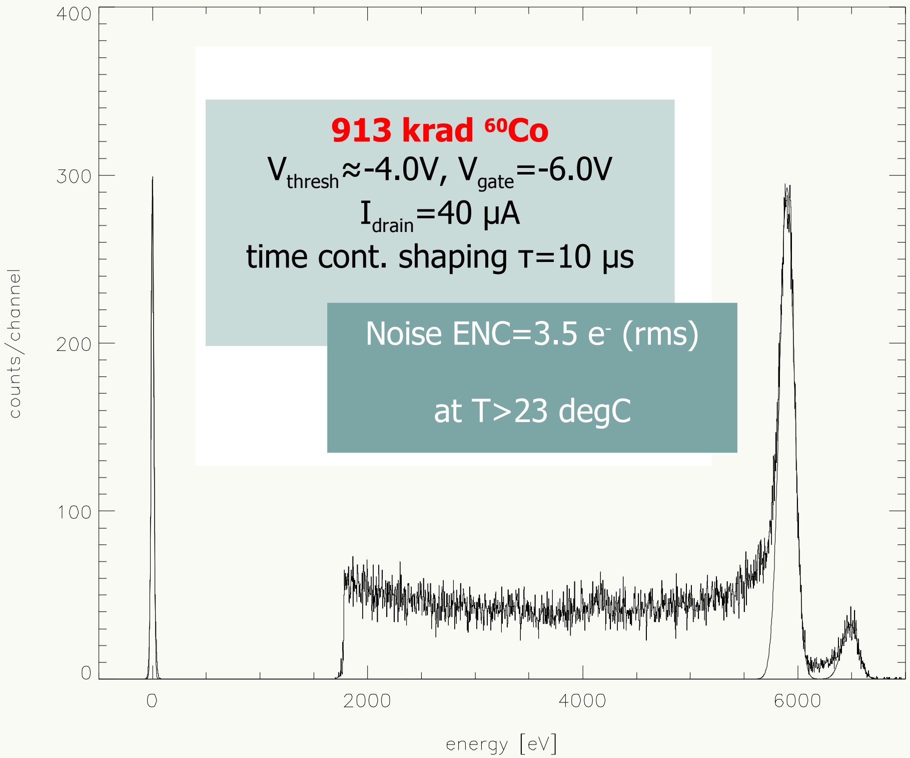
V_{thresh}≈-0.2V, V_{gate}=-2V

I_{drain}=41 μA

time cont. shaping τ=10 μs

Noise ENC=1.6 e^- (rms)

at T>23 degC



913 krad ^{60}Co

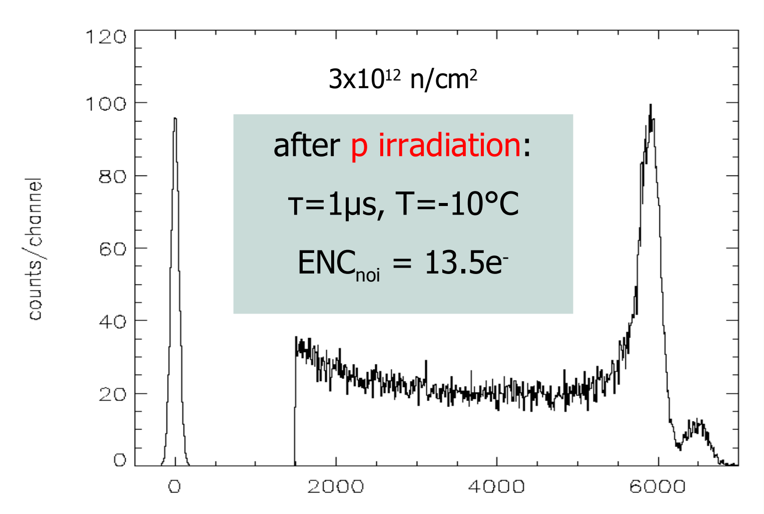
V_{thresh}≈-4.0V, V_{gate}=-6.0V

I_{drain}=40 μA

time cont. shaping τ=10 μs

Noise ENC=3.5 e^- (rms)

at T>23 degC

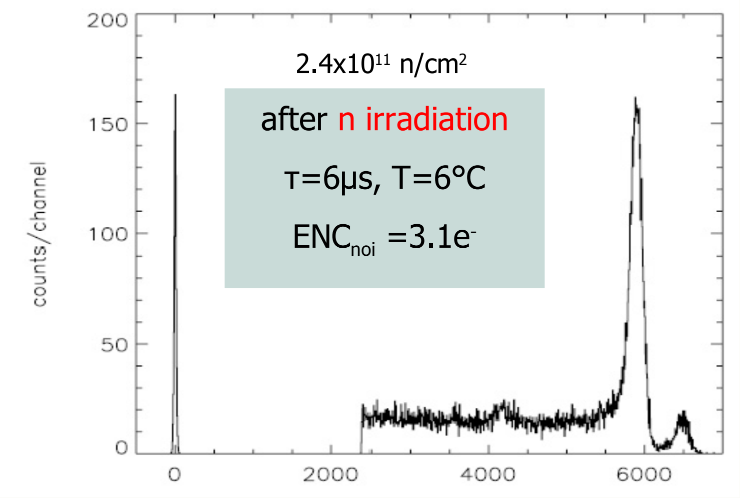


$3x10^{12}$ n/cm^2

after p irradiation:

τ=1μs, T=-10°C

ENC_{noi} = 13.5e^-



$2.4x10^{11}$ n/cm^2

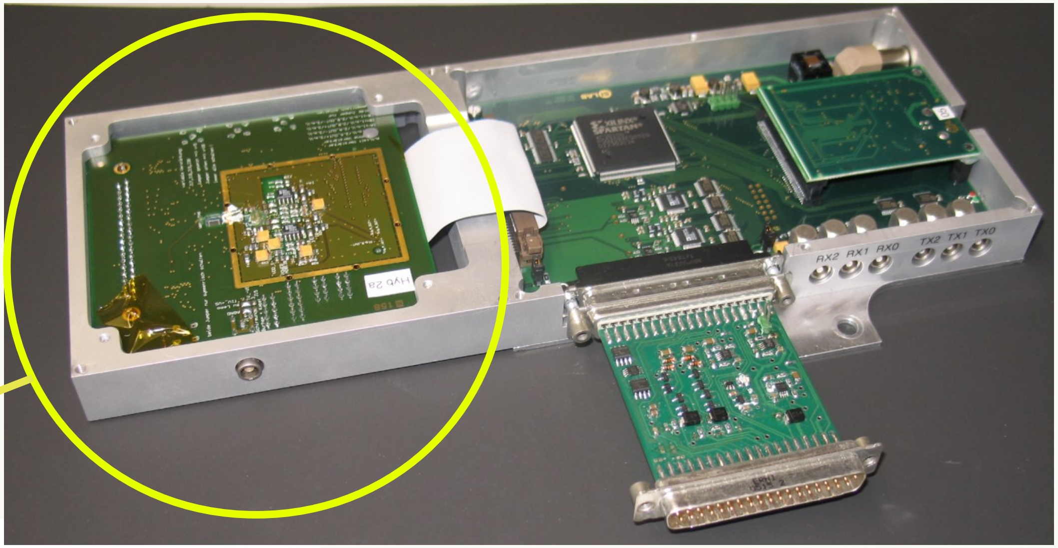
after n irradiation

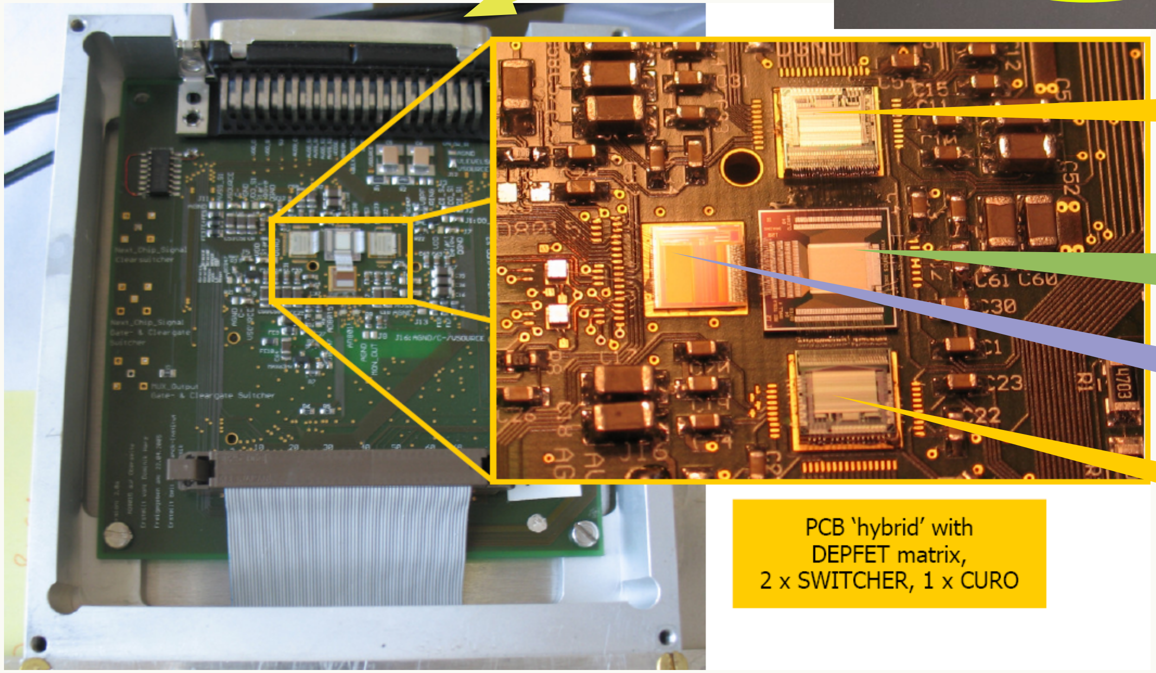
τ=6μs, T=6°C

ENC_{noi} =3.1e^-

Module Testing

- ✔ Hybrid:
  - ➔ Small DEPFET matrix
  - ➔ Steering chip: SWITCHER
  - ➔ Readout chip: CURO
- ✔ S3A Board:
  - ➔ FPGA to control the DAQ
  - ➔ USB interface with PC





PCB ‘hybrid’ with DEPFET matrix, 2 x SWITCHER, 1 x CURO

Switcher chip provides gate voltages

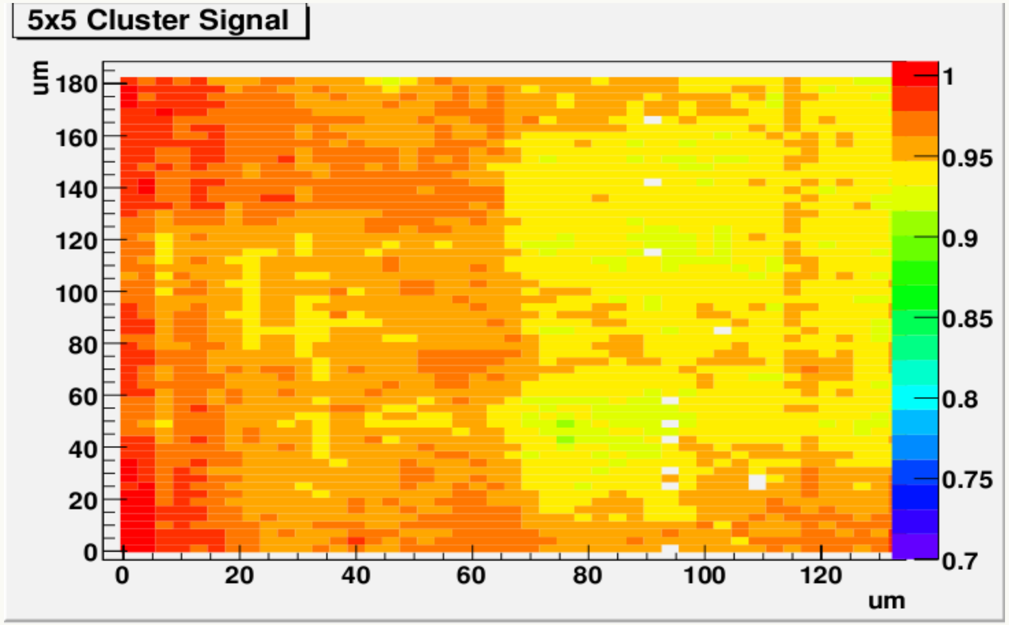
DEPFET Matrix
64x128 pixels
36 x 28.5μm^2

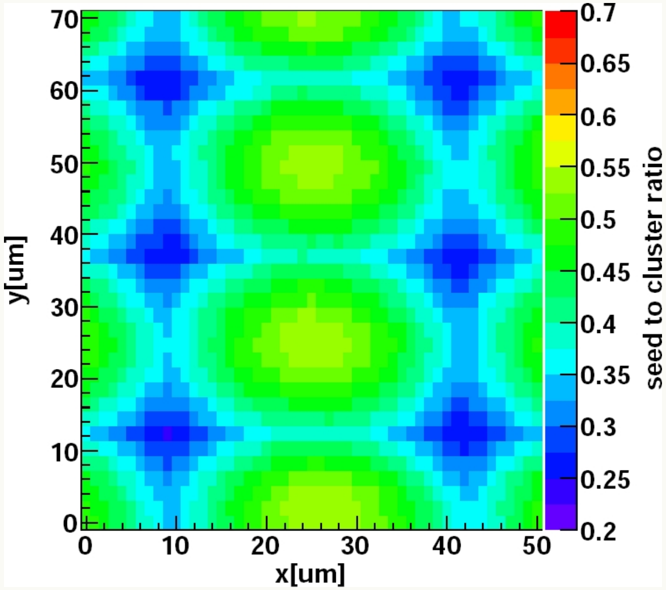
CURO chip

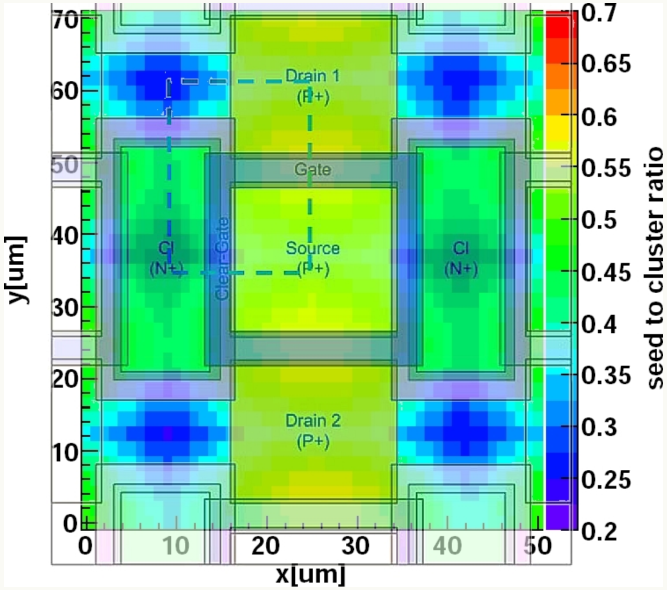
Switcher chip provides clear voltages

Laser tests

- ✔ Use an infrared laser and scan an ILC pixel structure with the help of an XY-stage.
- ✔ We have 100% fill factor, with small variations of the signal.



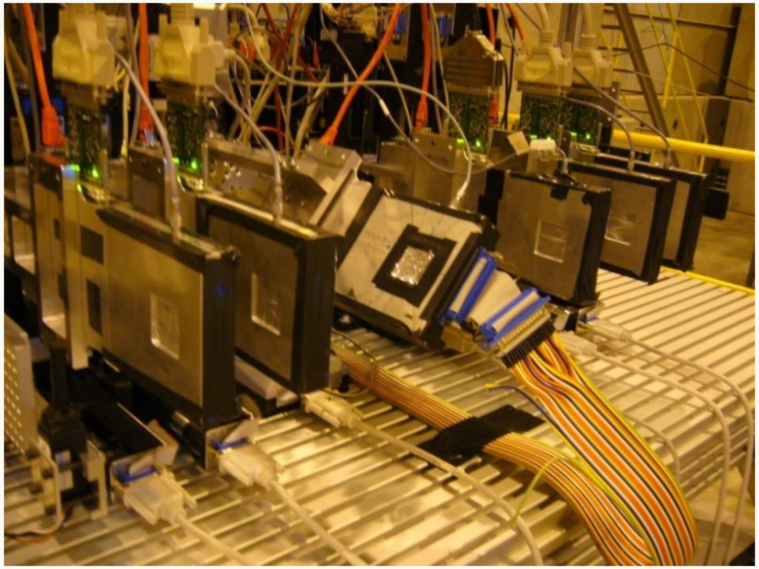




The seed/cluster signal ratio shows how the charge is shared among neighboring pixels.

Even with a hit under the gate, the seed represents only 60% of the cluster signal.

Beam Test



- ✔ Beam test at CERN SPS using a DEPFET only telescope with 4 planes + 2 DUTs
- ✔ Sensor thickness: 400 μm
- ✔ SNR ~ 120
- ✔ Noise ~ 300 e^- ENC (mainly due to CURO chip)
- ✔ Resolution given by residuals (No MS nor tracking error correction) is ~2-3 μm in both coordinates

	D0 (32x24)	D1 (32x24)	D2 (24x24)	d3(32x24)	D4 (32x24)	D5 (32x24)
Sig 3x3 (ADU)	1339	1497	1704	1715	1508	1654
Noise (ADU)	12.7	13.4	12.7	13.4	12.8	13.2
SNR	105	112	134	128	118	125
ENC (e^-)	345	326	286	284	309	290
G_q (pA/e_-)	283	316	360	363	319	350
Res X (μm)	2.9	2.2	2.1	2.1	3.0	3.4
Res Y (μm)	2.6	2.0	1.7	2.0	2.4	3.1

Summary

- ✔ DEPFET technology is a good candidate for the vertex detector in the coming e^+e^- colliders
  - ➔ A firm candidate for the Future Linear collider
  - ➔ Baseline technology for the Belle upgrade (Belle II)
- ✔ A high level of maturity.
- ✔ Provides a low power, low noise, monolithic pixel detector technology.
- ✔ Charge is collected in a fully depleted bulk, providing the maximum charge for a given thickness.
- ✔ There is a smart thinning technology that allows to deliver a 50 μm thick detector with sufficient mechanical stability.
- ✔ Radiation tolerant up to ~1 Mrad (with today's measurements).