DEPFET Active Pixel Detectors For Future Colliders
DEPFET is also a collaboration

(www.depfet.org)

✔ DEPFET is also an international collaboration.
✔ 12 research institutes and universities
✔ Working to build with the DEPFET sensors developed at the HLL MPI a system suitable for the vertex detectors in the coming e⁺e⁻ colliders.
Introduction

- Next generation of e+e- colliders require new pixel detector concepts that
  - Provide very good spatial resolution,
  - Can cope with a considerable amount of background and
  - Keep the material budget as low as possible to minimize the effect of multiple scattering.
    - Active cooling “forbidden” in sensitive area

- DEPFET (DEPleted Field Effect Transistor) is a very good candidate technology
  - DEPFET is the baseline technology for Belle II upgrade and
  - Competes with other technologies for the Future Linear Collider

<table>
<thead>
<tr>
<th></th>
<th>ILC</th>
<th>Belle II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Occupancy</td>
<td>0.13 hits/μm²/sec</td>
<td>0.4 hits/μm²/sec</td>
</tr>
<tr>
<td>Radiation</td>
<td>&lt;100 kRad/year</td>
<td>&gt; 1 Mrad/year</td>
</tr>
<tr>
<td>Power Duty Factor</td>
<td>1/200</td>
<td>1</td>
</tr>
<tr>
<td>Frame time</td>
<td>25-100 μs</td>
<td>10 μs</td>
</tr>
<tr>
<td></td>
<td>Large momentum range</td>
<td>Low (&lt;1 GeV/c) mom. tracks</td>
</tr>
<tr>
<td></td>
<td>Required IP res. 3-5 μm</td>
<td>IP res. dominated by MS (~9 μm)</td>
</tr>
<tr>
<td></td>
<td>Small pixels: 25x25 μm²</td>
<td>Pixels can be larger: 50x70 μm²</td>
</tr>
<tr>
<td></td>
<td>Low material budget: 0.1X0</td>
<td>Low material budget: 0.15 X0</td>
</tr>
<tr>
<td></td>
<td>-&gt; Thickness: 50 μm</td>
<td>-&gt; Thickness: 50 μm</td>
</tr>
</tbody>
</table>
The key concept: the integration of amplifying transistors in a fully depleted bulk

- Charge carriers drift due to the electric field (fast)
- Large signal

By means of sidewards depletion and an n-implant a potential minimum for electrons (the internal gate) is created under the transistor channel

- Electrons drift to the internal gate where they are stored
- Readout on demand

The charge in the internal gate modulates the channel current in the transistor

- When a voltage is applied to the gate, the current change in the drain is proportional to the charge \( g_q \) – internal amplification
- When the transistor is off, there is no current (no power consumption) but the detector is still sensitive
Internal Amplification

- The internal amplification measures the change in drain current in the presence of charge in the internal gate:

\[ g_q = \frac{dI_{ds}}{dQ_{int}} \sim \frac{\sqrt{I_{ds}}}{\sqrt{WL}^{\frac{3}{2}}} \]

- For an input noise with an equivalent current noise of \( \sigma \) the contribution to the ENC is

\[ \sigma / q_q \]

- Increasing \( g_q \) increases SNR, if the electronics is the dominant noise.

- Playing with channel length we can achieve up to \( g_q \sim 1 \text{nA/e}^- \)
The Clear Mechanism

- Charge is stored in the internal gate until we remove it.
- Charge removal is done by means of a lateral field that makes the charges drift away from the internal gate to the clear.
- Clear is shielded by a p-well to avoid charge losses.
  - This creates a potential barrier that hinders the clear process.
- A Clear Gate structure added to overcome this barrier as well as the potential of the substrate around the internal gate.
The Clear Mechanism

Potential $U_{\text{CLEAR}} \sim 3V$

Charge collection state

Potential $U_{\text{CLEAR}} \sim 6V$

Barrier partially removed

Potential $U_{\text{CLEAR}} > 10V$

Clear - charge is removed by drift

If clear is not complete we have reset noise in the pedestal current.

When clear is complete, the reset noise vanishes and the measured pedestal current spread is minimal.

We can achieve a complete clear with $V_{\text{clear}} \sim 10V$ and a wide range of $V_{\text{clear gate}}$ values.
Pixe clamp for Future e⁺e⁻ colliders

✔ We read a DEPFET pixel array in "rolling shutter" mode.
   ➔ Select row with external gate
   ➔ Read out data
   ➔ Select next row and repeat

✔ Besides the readout chip, we need two additional steering chips to provide
   ➔ the Gate voltage to activate the pixels to be readout in the active row
   ➔ The Clear voltage to remove the charge from the internal gate on those pixels

✔ We read the current from the drain.
   ➔ Drain is kept at a constant potential by an input cascode
   ➔ Faster

✔ While reading one row all the other pixels are in "OFF" state
   ➔ No power consumption
   ➔ Still collecting charge

See H. Krüger talk for details on the electronics
The readout sequence

- **CDS (Correlated Double Sampling)**
- Usually: \( \text{Signal} = (S_a + P_a) - P_a \)
- If there is complete clear and, therefore, no reset noise then \( P_{a-1} = P_a \)
- **DEPFET:** \( \text{Signal} = (S_{a-1} + P_{a-1}) - P_a \)
- We do not need to store the “pedestal frame” during the CDS
High Speed Operation Performance

**High Speed readout**

High bandwidth  
Short shaping times  
Thermal Noise $\sim \tau^{-1/2}$

Measurement of a single pixel shown below  
Intrinsic DEPFET noise small enough

ENC $\sim 40$-$50$ e$^-$ @ $\tau=20$ns (50 MHz)  
Signal (50 $\mu$m) : 4000 e$^-$ -> S/N $\sim$ 80-100

**Fast Clear**

Needed for high speed operation  
Complete clear achievable in $\sim$10ns

Again, pedestal current spread shown as a function of time.

Full clear happens when the spread is minimal.
The sample-clear-sample cycle can be accomplished in ~80-100 ns. The time to read one frame (all rows in the array) depends on the number of cycles needed.
To minimize the frame time we should reduce the number of sample-clear-sample cycles:

- Split the frame readout in 2 sides
- Activate more than one row at a time
  - This increases the number of readout channels
  - ILC module activates 2 rows at a time
  - Belle II module activate 4 rows at a time

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**Pixel size:**
- ILC: 25x25 μm
- Belle II: 50x70 μm

Can accommodate more column lines.
The module

Module divided in 2 halves for readout (Z<0 and Z>0)

SBelle pixels
4 row readout

Module thinned down in sensitive area.

Chips on *balconies*, which are grooved to reduce material while keeping mechanical stability

Sensitive region can be *reinforced* to avoid deflections.

ILC pixels
2 row readout
Wafer thinning

1) Process backside of thick detector wafer (structured) implant.

2) Bond detector wafer on handle wafer.

3) Thin detector wafer to desired thickness (grinding & etching).

4) Process front side of the detector wafer in a standard (single sided) process line.

5) Etch handle wafer.
   If necessary: add Al-contacts
   Leave frame for stiffening and handling

Industry: TraciT, Grenoble
Wafer Thinning

6” wafer with diodes and large mechanical samples

Possibility to structure handling frame (reduce material, keep stiffness)

Thinned area: 10cm x 1.2 cm (ILC vertex detector dummy)
Irradiations

- Non ionizing Energy Loss (NIEL)
  - Leakage current increase \(\rightarrow\) shot noise
  - Trapping not critical for the expected doses

- Ionizing radiation – Total Ionizing dose (TID)
  - 2 MOS gates (Gate, Clear Gate)...
  - Fixed oxide positive charge \(\rightarrow\) \(\Delta V_T\)
  - Interface trap density
    - Reduced mobility \(g_m\)
    - Higher 1/f noise

<table>
<thead>
<tr>
<th>Type</th>
<th>PXD4-10 MO2</th>
<th>PXD4-5 MO5</th>
<th>PXD4-2 J14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Protons, 30MeV</td>
<td>Neutrons, 1-20MeV</td>
<td>Gammas - (^{60})Co</td>
</tr>
<tr>
<td>Fluence / Dose</td>
<td>(1.2 \cdot 10^{12}) p/cm(^2)</td>
<td>(1.6 \cdot 10^{11}) n/cm(^2)</td>
<td>913kRad</td>
</tr>
<tr>
<td>1MeV n equivalent</td>
<td>(3 \cdot 10^{12}) n(_{eq})/cm(^2)</td>
<td>(2.4 \cdot 10^{11}) n(_{eq})/cm(^2)</td>
<td>n/a</td>
</tr>
</tbody>
</table>
Basic par.: $\Delta V_T$, $g_m$, $I_{\text{leak}}$

<table>
<thead>
<tr>
<th>Irradiation</th>
<th>TID / NIEL fluence</th>
<th>$\Delta V_{\text{th}}$</th>
<th>$g_m$</th>
<th>$I_{\text{leak}}$ in int. gate at RT(*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gamma $^{60}$Co</td>
<td>913 krad / ~ 0</td>
<td>~ -4V</td>
<td>unchanged</td>
<td>156 fA</td>
</tr>
<tr>
<td>Neutron</td>
<td>~ 0 / 2.4x10$^{11}$ n/cm$^2$</td>
<td>~ 0</td>
<td>unchanged</td>
<td>1.4 pA</td>
</tr>
<tr>
<td>Proton</td>
<td>283 krad / 3x10$^{12}$ n/cm$^2$</td>
<td>~ -5V</td>
<td>~ -15%</td>
<td>26 pA</td>
</tr>
</tbody>
</table>

(*) 5..22 fA non irrad.
Spectroscopic performance

**non-irradiated**

- $V_{\text{thresh}} \approx 0.2\,\text{V}$, $V_{\text{gate}} = -2\,\text{V}$
- $I_{\text{drain}} = 41\,\mu\text{A}$
- Time cont. shaping $\tau = 10\,\mu\text{s}$

Noise ENC=$1.6\times 10^{-9}$ e$^-$ (rms)

at $T > 23\,\text{degC}$

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**913 krad $^{60}\text{Co}$**

- $V_{\text{thresh}} \approx -4.0\,\text{V}$, $V_{\text{gate}} = -6.0\,\text{V}$
- $I_{\text{drain}} = 40\,\mu\text{A}$
- Time cont. shaping $\tau = 10\,\mu\text{s}$

Noise ENC=$3.5\times 10^{-9}$ e$^-$ (rms)

at $T > 23\,\text{degC}$

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**after $p$ irradiation:**

- $\tau = 1\mu\text{s}$, $T = -10^\circ\text{C}$
- ENC$_{\text{noi}} = 13.5e^-$

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**after $n$ irradiation**

- $\tau = 6\mu\text{s}$, $T = 6^\circ\text{C}$
- ENC$_{\text{noi}} = 3.1e^-$

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$3 \times 10^{12}$ n/cm$^2$

$2.4 \times 10^{11}$ n/cm$^2$
Module Testing

✓ Hybrid:
  ➔ Small DEPFET matrix
  ➔ Steering chip: SWITCHER
  ➔ Readout chip: CURO

✓ S3A Board:
  ➔ FPGA to control the DAQ
  ➔ USB interface with PC

Switcher chip provides gate voltages

DEPFET Matrix
64x128 pixels
36 x 28.5µm²

CURO chip

Switcher chip provides clear voltages

PCB ‘hybrid’ with
DEPFET matrix,
2 x SWITCHER, 1 x CURO
Laser tests

✔ Use an infrared laser and scan an ILC pixel structure with the help of an XY-stage.

✔ We have 100% fill factor, with small variations of the signal.

The seed/cluster signal ratio shows how the charge is shared among neighboring pixels.

Even with a hit under the gate, the seed represents only 60% of the cluster signal.
Beam Test

- Beam test at CERN SPS using a DEPFET only telescope with 4 planes + 2 DUTs
- Sensor thickness: 400 μm
- SNR ~ 120
- Noise ~ 300 e⁻ ENC (mainly due to CURO chip)
- Resolution given by residuals (No MS nor tracking error correction) is ~2-3 μm in both coordinates

<table>
<thead>
<tr>
<th></th>
<th>D0 (32x24)</th>
<th>D1 (32x24)</th>
<th>D2 (24x24)</th>
<th>d3(32x24)</th>
<th>D4 (32x24)</th>
<th>D5 (32x24)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sig 3x3 (ADU)</td>
<td>1339</td>
<td>1497</td>
<td>1704</td>
<td>1715</td>
<td>1508</td>
<td>1654</td>
</tr>
<tr>
<td>Noise (ADU)</td>
<td>12.7</td>
<td>13.4</td>
<td>12.7</td>
<td>13.4</td>
<td>12.8</td>
<td>13.2</td>
</tr>
<tr>
<td>SNR</td>
<td>105</td>
<td>112</td>
<td>134</td>
<td>128</td>
<td>118</td>
<td>125</td>
</tr>
<tr>
<td>ENC (e⁻)</td>
<td>345</td>
<td>326</td>
<td>286</td>
<td>284</td>
<td>309</td>
<td>290</td>
</tr>
<tr>
<td>Gₚ (pA/e⁻)</td>
<td>283</td>
<td>316</td>
<td>360</td>
<td>363</td>
<td>319</td>
<td>350</td>
</tr>
<tr>
<td>Res X (μm)</td>
<td>2.9</td>
<td>2.2</td>
<td>2.1</td>
<td>2.1</td>
<td>3.0</td>
<td>3.4</td>
</tr>
<tr>
<td>Res Y (μm)</td>
<td>2.6</td>
<td>2.0</td>
<td>1.7</td>
<td>2.0</td>
<td>2.4</td>
<td>3.1</td>
</tr>
</tbody>
</table>
Summary

✔ DEPFET technology is a good candidate for the vertex detector in the coming $e^+e^-$ colliders
  ➔ A firm candidate for the Future Linear collider
  ➔ Baseline technology for the Belle upgrade (Belle II)
✔ A high level of maturity.
✔ Provides a low power, low noise, monolithic pixel detector technology.
✔ Charge is collected in a fully depleted bulk, providing the maximum charge for a given thickness.
✔ There is a smart thinning technology that allows to deliver a 50 μm thick detector with sufficient mechanical stability.
✔ Radiation tolerant up to ~1 Mrad (with today's measurements).