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A FPGA-based Network Interface Card with GPUDirect enabling real-time GPU computing in HEP experiments.

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While GPGPU paradigm is widely recognized as an effective approach to high performance computing, its usage in low-latency, real-time systems is still in early stages in HEP experiments.

GPUs typically show deterministic behaviour in terms of processing latency once data are available in their internal memories, but assessment of real-time features of a standard GPGPU system takes a careful characterization of all subsystems along data stream path. The networking subsystem results the most critical one in terms of latency fluctuations.

Our envisioned solution to this issue is NaNet, an FPGA-based PCIe Network Interface Card (NIC) design featuring a configurable set of network channels with direct access to NVIDIA Fermi/Kepler GPU memories (GPUDirect).

NaNet design currently supports both standard - 1GbE (1000Base-T) and 10GbE (10Base-R) - and custom - 34Gbps APElink and 2.5Gbps deterministic latency KM3link - channels, but its modularity allows for a straightforward inclusion of other link technologies.

To avoid host OS intervention on data stream and remove a possible source of jitter, the design includes a transport layer offload module with cycle-accurate upper-bound latency, supporting UDP, KM3link Time Domain Multiplexing and APElink protocols.

After NaNet architecture description and its latency/bandwidth characterization for all supported links, two real world use cases will be presented: the GPU-based low level trigger for the RICH detector in NA62 experiment and the on-/off-shore data link for KM3 underwater neutrino telescope.

NaNet performances in both experiments will be presented and discussed.

Primary authors: LONARDO, Alessandro (ROMA1); BIAGIONI, Andrea (ROMA1); PASTORELLI, Elena (INFN); AMELI, Fabrizio (ROMA1); Dr LOCICERO, Francesca (INFN); SIMEONE, Francesco (ROMA1); SIMULA, Francesco (ROMA1); LAMANNA, Gianluca (PI); TOSORATTO, Laura (ROMA1); Dr PONTISSO, Luca (Università di Roma "Sapienza"); SOZZI, Marco (PI); Dr FREZZA, Ottorino (INFN); VICINI, Piero (ROMA1); AMMENDOLA, Roberto (ROMA2)

Presenter: LONARDO, Alessandro (ROMA1)

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