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First Level Event Selection oackage for the CBV experiment

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Reconstruction Challenge in CBM



Open Charm Event Selection



$$\begin{array}{l} D^{\pm} (c\tau = 312 \ \mu\text{m}):\\ D^{+} \rightarrow \text{K}^{-}\pi^{+}\pi^{+} \quad (9.5\%)\\ D^{0} (c\tau = 123 \ \mu\text{m}):\\ D^{0} \rightarrow \text{K}^{-}\pi^{+} \quad (3.8\%)\\ D^{0} \rightarrow \text{K}^{-}\pi^{+}\pi^{+}\pi^{-} \quad (7.5\%)\\ D^{\pm}_{s} (c\tau = 150 \ \mu\text{m}):\\ D^{\pm}_{s} \rightarrow \text{K}^{+}\text{K}^{-}\pi^{+} \quad (5.3\%)\\ \Lambda^{+}_{c} (c\tau = 60 \ \mu\text{m}):\\ \Lambda^{+}_{c} \rightarrow \text{pK}^{-}\pi^{+} \quad (5.0\%) \end{array}$$

No simple trigger primitive, like high p_t , available to tag events of interest. The only selective signature is the detection of the decay vertex.



First level event selection will be done in a processor farm fed with data from the event building network

Many-Core CPU/GPU Architectures



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CBM Kalman Filter Track Fit Library

Kalman Filter Methods

Kalman Filter Tools:

- KF Track Fitter
- KF Track Smoother
- Deterministic Annealing Filter

Kalman Filter Approaches: • Conventional DP KF

- Conventional SP KF
- Square-Root SP KF
- UD-Filter SP
- Gaussian Sum Filter

Track Propagation:

- Runge-Kutta
- Analytic Formula





Implementations

Vectorization (SIMD):

- Header Files
- Vector Classes Vc
- Array Building Blocks ArBB
- OpenCL

Parallelization (many-cores):

- Open MP
- ITBB
- ArBB
- OpenCL

Precision:

- single
- double





Strong many-core scalability of the Kalman filter library

CPU Scalability

CPU Sc

CBM Kalman Filter Track Fit Library



Full portability of the Kalman filter library

Cellular Automaton as Track Finder



Useful for complicated event topologies with large combinatorics and for parallel hardware

CBM CA Track Finder: Efficiency



Efficient and stable event reconstruction

4D Event Building with CA Track Finder

Entries

Input Hits

- The beam in the CBM will have no bunch structure, but continuous.
- Measurements in this case will be 4D (x, y, z, t).
- Reconstruction of time slices rather than events will be needed.



Reconstructed tracks clearly represent groups, which correspond to the original events

4D Event Building with CA Track Finder

Total CA time = 84 ms



4D event building is scalable with the speed-up factor of 10.1 (out of 13)

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KF Particle Finder for Physics Analysis and Selection



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KF Particle Finder on Xeon Phi



- Standalone KF Particle Finder is adapted for the Xeon Phi card. The same code is used for the CPU and the Xeon Phi.
- The program is tested on search for K_s^0 , Λ , Ξ and Ω particles.
- The parallelism between cores is implemented on the event level and tested with 100 U+U mbias events per thread.
- The program scales up to 240 logical cores on the Xeon Phi.
- Time per one thread: CPU 3.7 ms, Xeon Phi 12.8 ms.
- SIMD Speedup: SSE (CPU, 4 elements) 3.67, AVX (CPU, length 8) 4.67, IMIC (Xeon Phi, length 16) 8.43.

KF Particle Finder is scalable with the speed-up factor of 120 on 240 logical cores.

STAR HLT

CBM Standalone First Level Event Selection (FLES) Package



The first version of the FLES package is vectorized, parallelized, portable and scalable

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Towards CBM FLES Demonstrator



- LOEWE CSC (FIAS, Frankfurt)
- Green Cube (GSI, Darmstadt)
- FAIR-Russia HPC Cluster (ITEP, Moscow)

From cores to the CBM FLES farm with 60 000 cores

Parallelization in the CBM Event Reconstruction

	CPU - Tracking					
Algorithm	SIMD	ITBB, OpenMP	CUDA	OpenCL CPU/GPU	Phi	ArBB
Hit Producers					All -	Benchmark
STS KF Track Fit	1	√	1	\checkmark	\checkmark	~
STS CA Track Finder	1	1				
MuCh Track Finder	✓	~	1			
TRD Track Finder	✓	1	1			
RICH Ring Finder	1	1		✓ GPU/Phi - Selection		
KF Particle Finder	1	\checkmark		<	 Image: A start of the start of	
Off-line Physics Analysis	1					
FLES Analysis and Selection	~	1				

CPU - Full reconstruction

Parallelization becomes a standard in the CBM experiment

Consolidate Efforts: Common Reconstruction Package



- Create a common FAIR reconstruction package
- Use also in running experiments (ALICE, STAR, ...)
- Optimize for many-core CPU/GPU/Phi architectures
- Hide parallelism and keep the traditional form of physics analysis

Consolidate Efforts: International Workshops FCTTC

International Workshops for Future Challenges in Tracking and Trigger Concepts

- GSI, Darmstadt, Germany, 1st 2nd CERN. Geneva. Switzerland.
- FIAS, Frankfurt, Germany, 3rd
- 4th CERN, Geneva, Switzerland,
- 5th
- FIAS, Frankfurt, Germany,
- 6th
- not yet fixed,

07-11.06.2010: 07-08.07.2011: 27-29.02.2012: 28-30.11.2012; 12-14.05.2014: April 2015.



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http://fias.uni-frankfurt.de/en/cs/conferences/fcttc-201-

Conclusion

For efficient use of many-core architectures we need to combine experience of physicists, computer scientists and CPU/GPU/Phi developers.