



Intel® HPC Portfolio

September 2014

Emiliano Politano
Technical Account Manager



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- Intel® Advanced Vector Extensions (Intel® AVX)* are designed to achieve higher throughput to certain integer and floating point operations. Due to varying processor power characteristics, utilizing AVX instructions may cause a) some parts to operate at less than the rated frequency and b) some parts with Intel® Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software, and system configuration and you should consult your system manufacturer for more information.
- No computer system can provide absolute security. Requires an enabled Intel® processor, enabled chipset, firmware and/or software optimized to use the technologies. Consult your system manufacturer and/or software vendor for more information

*Intel® Advanced Vector Extensions refers to Intel® AVX, Intel® AVX2 or Intel® AVX-512. For more information on Intel® Turbo Boost Technology 2.0, visit <http://www.intel.com/go/turbo>

Optimization Notice

Optimization Notice

Intel® compilers, associated libraries and associated development tools may include or utilize options that optimize for instruction sets that are available in both Intel® and non-Intel microprocessors (for example SIMD instruction sets), but do not optimize equally for non-Intel microprocessors. In addition, certain compiler options for Intel compilers, including some that are not specific to Intel micro-architecture, are reserved for Intel microprocessors. For a detailed description of Intel compiler options, including the instruction sets and specific microprocessors they implicate, please refer to the “Intel® Compiler User and Reference Guides” under “Compiler Options.” Many library routines that are part of Intel® compiler products are more highly optimized for Intel microprocessors than for other microprocessors. While the compilers and libraries in Intel® compiler products offer optimizations for both Intel and Intel-compatible microprocessors, depending on the options you select, your code and other factors, you likely will get extra performance on Intel microprocessors.

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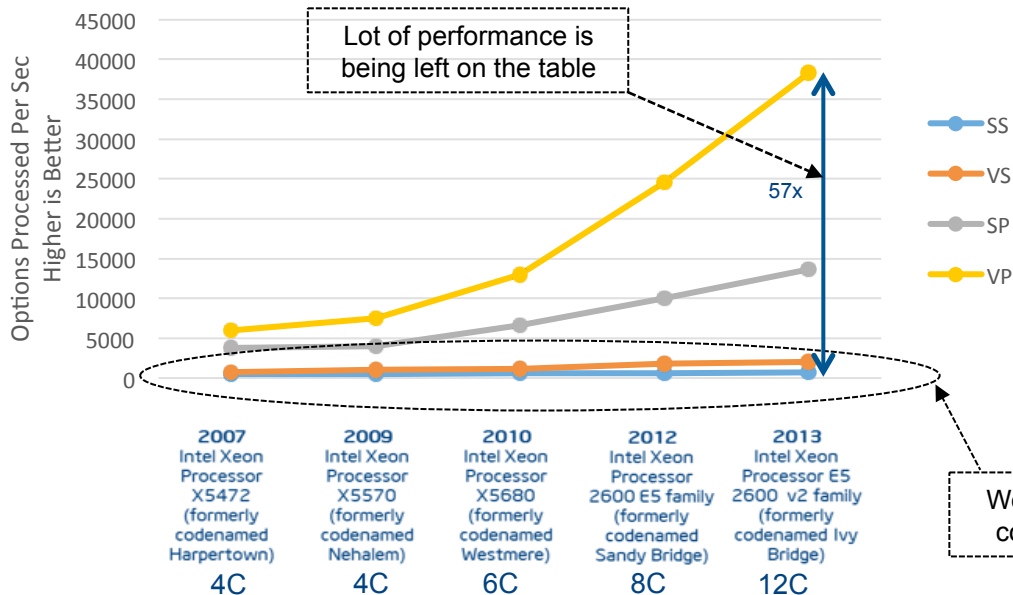
While Intel believes our compilers and libraries are excellent choices to assist in obtaining the best performance on Intel® and non-Intel microprocessors, Intel recommends that you evaluate other compilers and libraries to determine which best meet your requirements. We hope to win your business by striving to offer the best performance of any compiler or library; please let us know if you find we do not.

Notice revision #20101101

Impact Of Code Modernization



Binomial Options DP

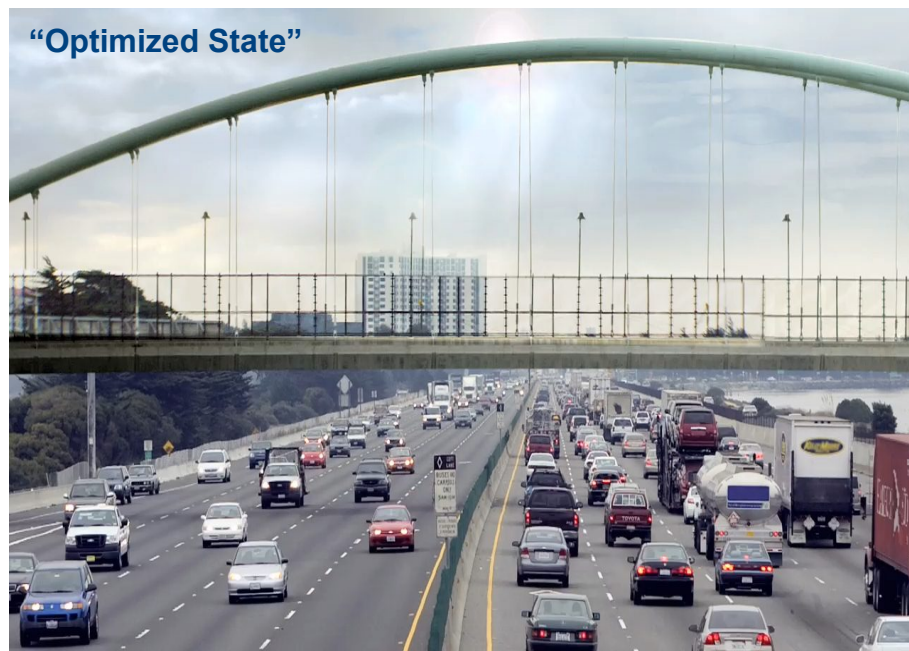


SS: Single threaded and Scalar
VS: Vectorized and Single threaded
SP: Scalar and parallel
VP: Vectorized and Parallelized.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. See slide in back-up for configuration details

Modernized software employs all available resources on existing/future Intel® Xeon® processors enabling maximization of ROI

What Maximum Performance Can Look Like With Usage Of All Intel® Xeon® Processor Lanes And



Intel can help maximize your ROI through parallelization and vectorization of your code

Intel® Xeon Phi™ Coprocessor provides further benefits...

What are Intel® Xeon Phi™ Coprocessors?



Intel® Xeon Phi™ Coprocessors work synergistically with Intel® Xeon® Processors

PCI Express form factor add-in cards

Up to 61 Cores, 1.24 Ghz and 244 Threads

Used primarily in servers and workstations

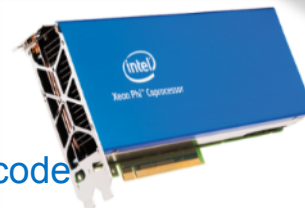
Great for Developers and Users with access to in-house software code

Ensure that your systems have BIOS to support Intel Xeon Phi™ Coprocessors

Key installations have been in HPC, or High Performance Computing, such as Supercomputers, including the #1 Supercomputer in the world.

What these are not:

- Desktop GPU replacements
- These coprocessors are not overclockable



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Source: [Intel® Xeon Phi™ Coprocessors Specifications](#)

Intel® Xeon Phi™ Coprocessor Product Lineup

7 Family

Highest Performance, Most
Memory
Performance leadership

16GB GDDR5
352GB/s
>1.2TF DP
300W TDP



5 Family

Optimized for High Density
Environments
Performance/watt leadership

8GB GDDR5
>300GB/s
>1TF DP
225-245W TDP



3 Family

Outstanding Parallel Computing
Solution
Performance/\$ leadership

6GB GDDR5
240GB/s
>1TF DP
300W TDP



Optional 3-year Warranty

Extend to 3-year warranty on any Intel® Xeon Phi™
Coprocessor. Product Code: XPX100WRNTY, MM# 933057

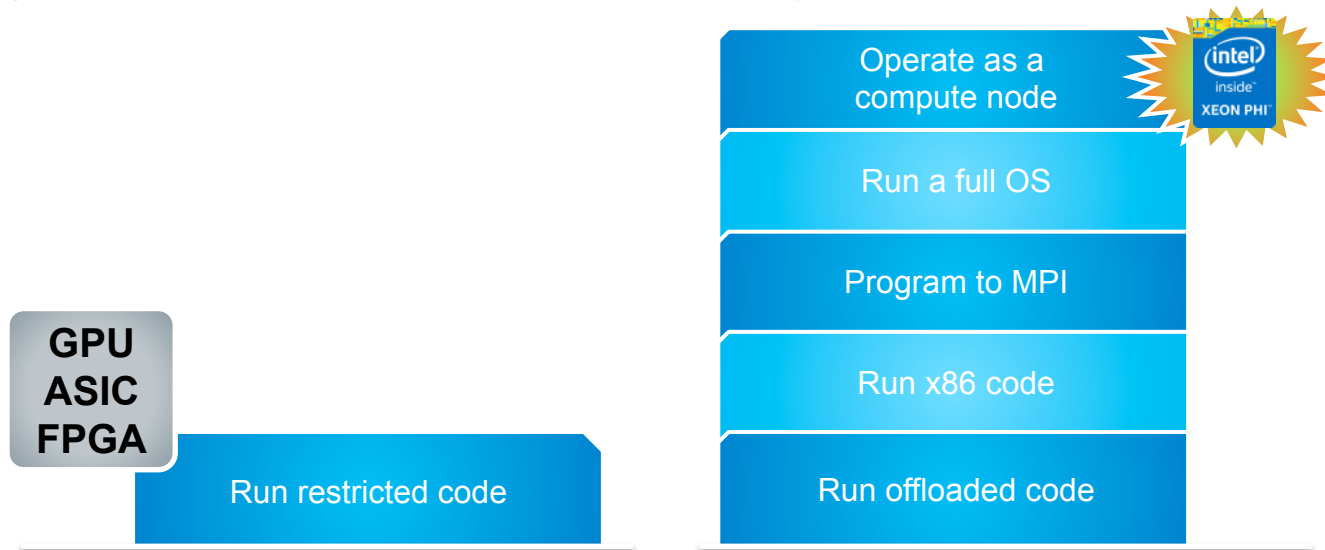
Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to <http://www.intel.com/performance>

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Intel® Xeon Phi™ Coprocessors: They're So Much More

General purpose IA Hardware leads to less idle time for your investment



Custom HW Acceleration

Intel® Xeon Phi™ Coprocessor*

Restrictive architectures limit the ability for applications to use arbitrary nested parallelism, functions calls and threading models

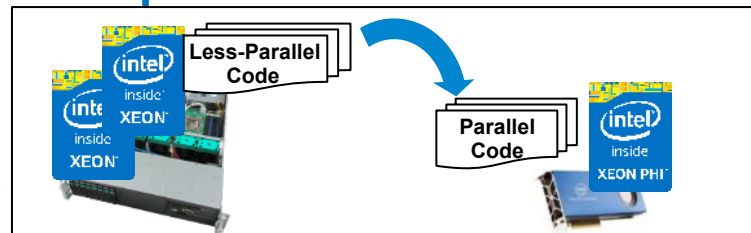
*Refer to software.intel.com/mic-developer for details on the Intel Xeon Phi™ coprocessor

Intel® Xeon Phi™ Coprocessor Execution Modes can be used to Fully Utilize All Compute Resources

Offload

Splitting up a workload where highly-parallel code is offloaded to the coprocessor, and the Xeon® host processors primarily run less-parallel code

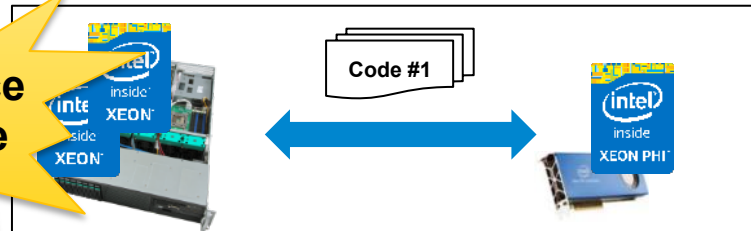
Nvidia GPUs only operate in OFFLOAD mode



Symmetric

Workload is split up into multiple instances which are distributed and run on both the host processors and Intel® Xeon Phi™ coprocessors

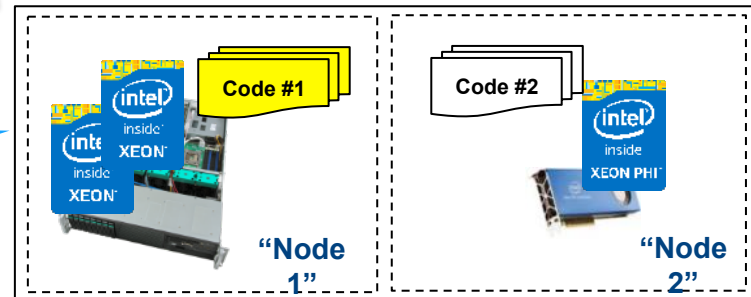
Load Balance to Maximize Utilization



Native

Coprocessor is configured as a separate compute node (full OS, IP addressable) to run an independent workload. Host CPUs are freed up to run separate workload(s)

Two Nodes, One System



Next Intel® Xeon Phi™ Product Family

(Codenamed *Knights Landing*)



- “Knights Landing” **code name** for the 2nd generation Intel® Xeon Phi™ product
- Based on Intel’s **14 nanometer** manufacturing process
- Standalone **bootable processor** (running the host OS) and a **PCIe coprocessor** (PCIe end-point device)
- Integrated **on-package high-bandwidth memory**
- **Flexible memory modes** for the on package memory include: cache and flat
- Support for Intel® Advanced Vector Extensions 512 (Intel® AVX-512)
- **60+ cores, 3+ TeraFLOPS** of double-precision peak performance per single socket node
- **Multiple hardware threads** per core with improved single-thread performance over the current generation Intel® Xeon Phi™ coprocessor

Picking the Right Tool for the Right Job

Xeon® will continue to be the right choice for MOST HPC workloads with parallel AND SERIAL components

Parallel and Fast Serial



Highly Parallel

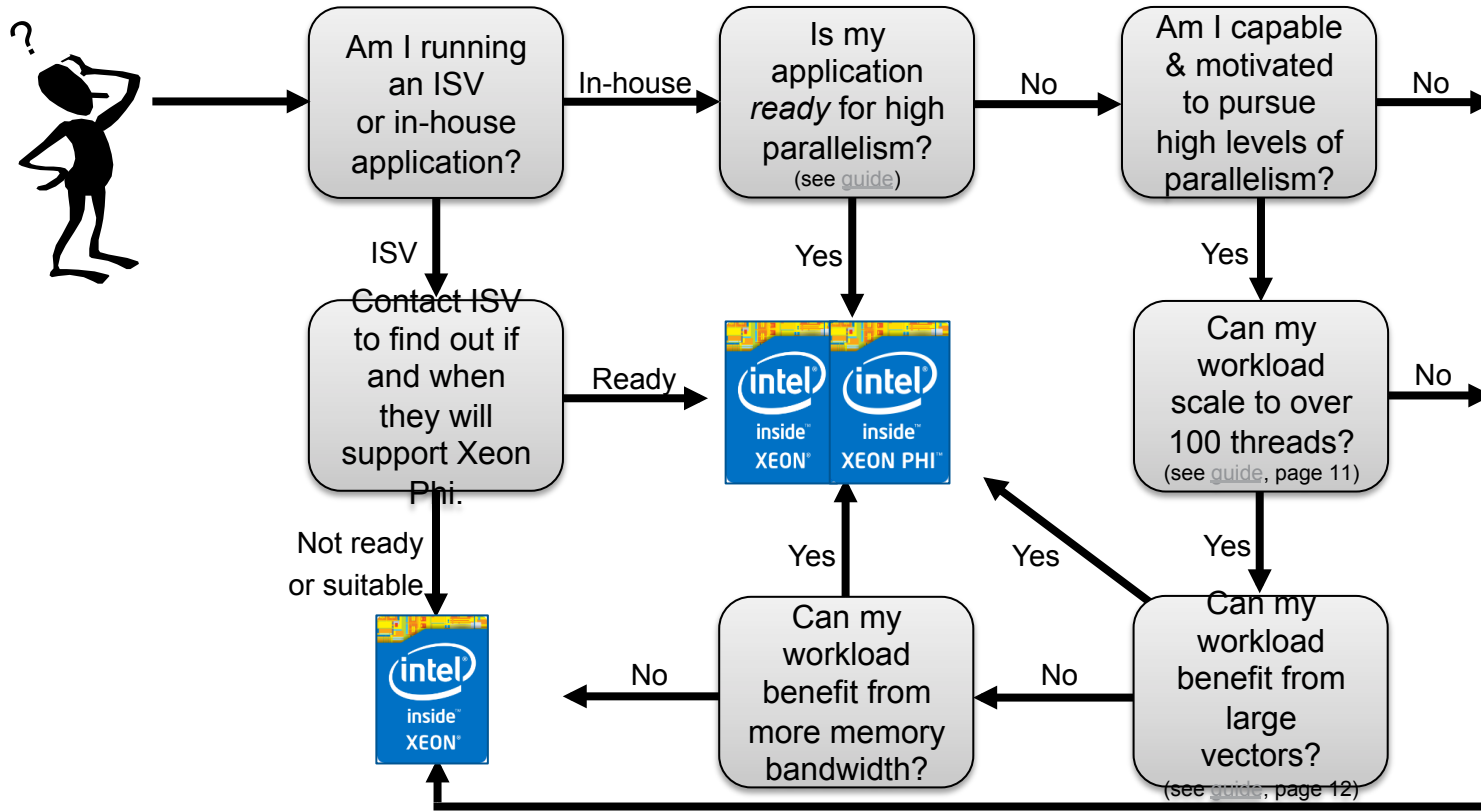


Xeon Phi™ is optimized for HIGHLY PARALLEL workloads

Programmability Benefits:
Single source,
converging ISA
Common environment

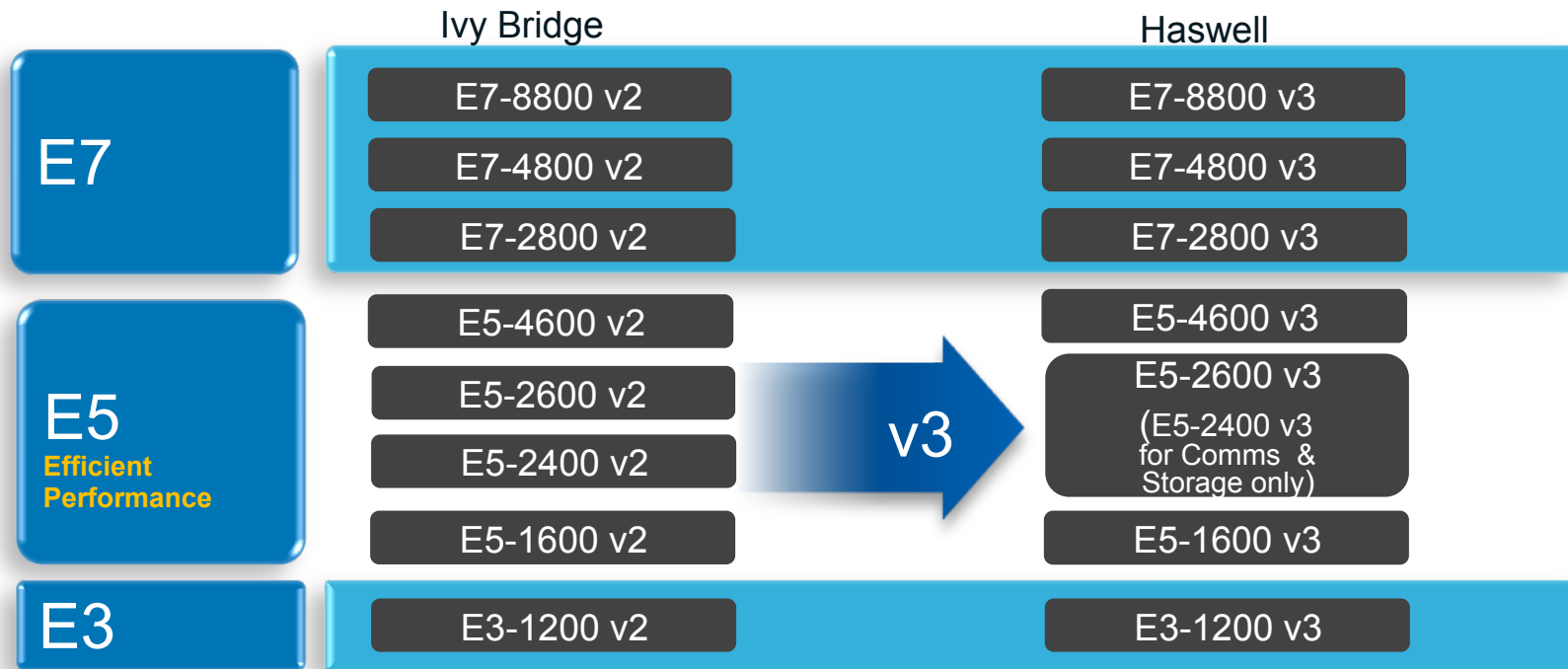
<https://software.intel.com/en-us/articles/is-intelr-xeon-phitm-coprocessor-right-for-you>

Is the Intel® Xeon Phi™ Coprocessor right for me?



<https://www-ssl.intel.com/content/www/us/en/processors/xeon/xeon-phi-detail.html>

Product Family Positioning – E5 Focus



Note: Above does not represent schedule, represents product family number construct only.

E5-2400 v3 moves to Storage and Comms servers only

Intel® Xeon® E5-2600 v3 Product Family



Up to 70% increase in workload performance with Intel® AVX 2[^]

Up to 36% increase in power efficiency with smarter power cores with Per Core P-States (PCPS)⁺

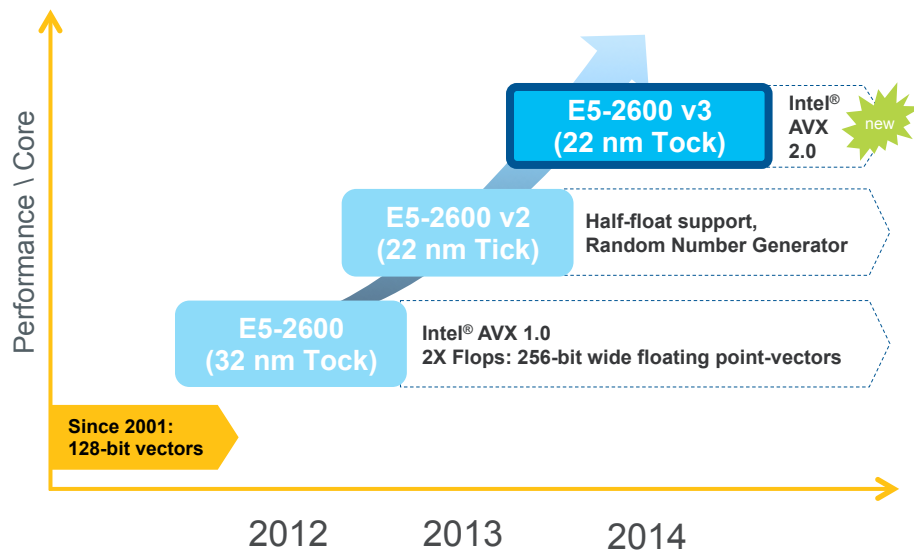
**Enabling virtualization orchestration with
Cache QoS monitoring**

[^]Refer to Slide 16 for Source and Configuration details

⁺Refer to Slide 20 for Source and Configuration details

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Intel® Advanced Vector Extensions (AVX) 2.0



- Floating point Fused Multiply Add (FMA) improves high performance computing, professional imaging, feature detection
- 256-bit integer vector instructions benefits math, codec, image processing and DSP software.

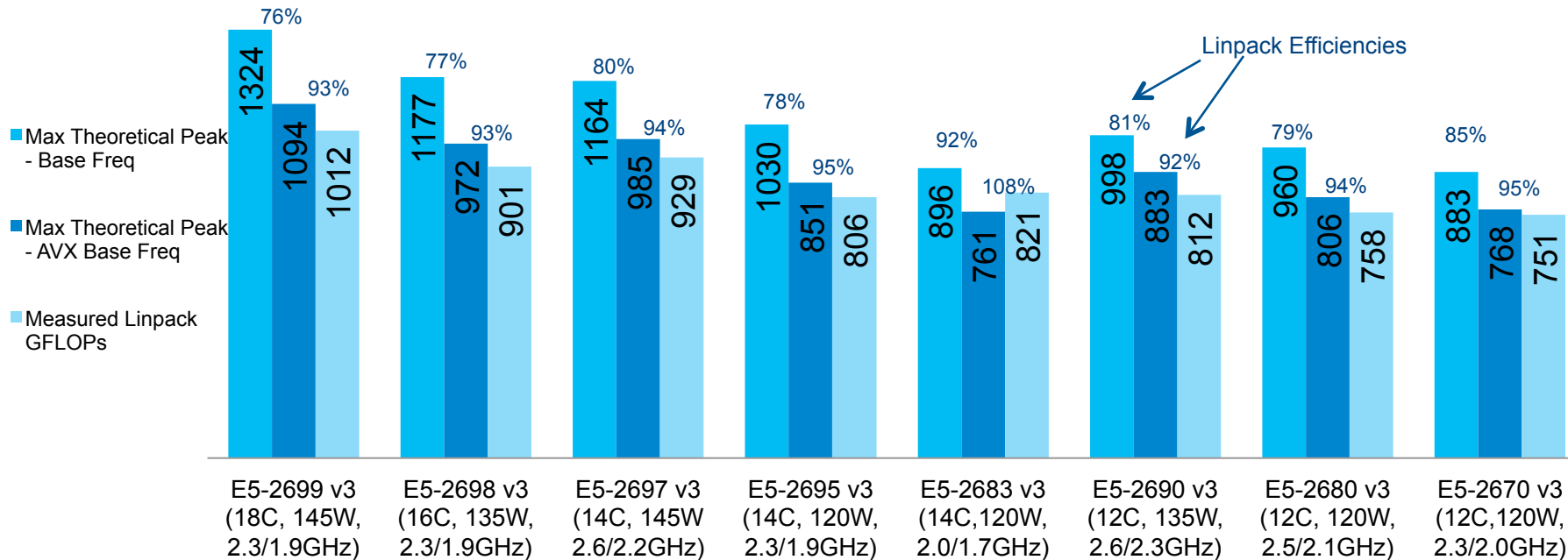
70% **UP TO 70% INCREASED PERFORMANCE**

Source as of 3 April 2014: Intel internal measurements on platform with two E5-2697 v2 (12C, 2.7GHz), 8x8GB DDR3-1866, RHEL6.3. Platform with two E5-2697 v3 (14C, 2.6GHz, 145W), 8x8GB DDR4-2133, RHEL 6.3. Performance based on geomean of BlackScholes, binomialcpu, MonteCarlo workloads. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. **For more information go to <http://www.intel.com/performance>** *Other names and brands may be claimed as the property of others.

Intel® Xeon® Processor E5-2600 v3 Product Family

Preliminary Theoretical Peak FLOPS

Max Theoretical Peak Performance (DP FLOPS) = 2 sockets x (#cores) x (freq) x (16 DP FLOPS)

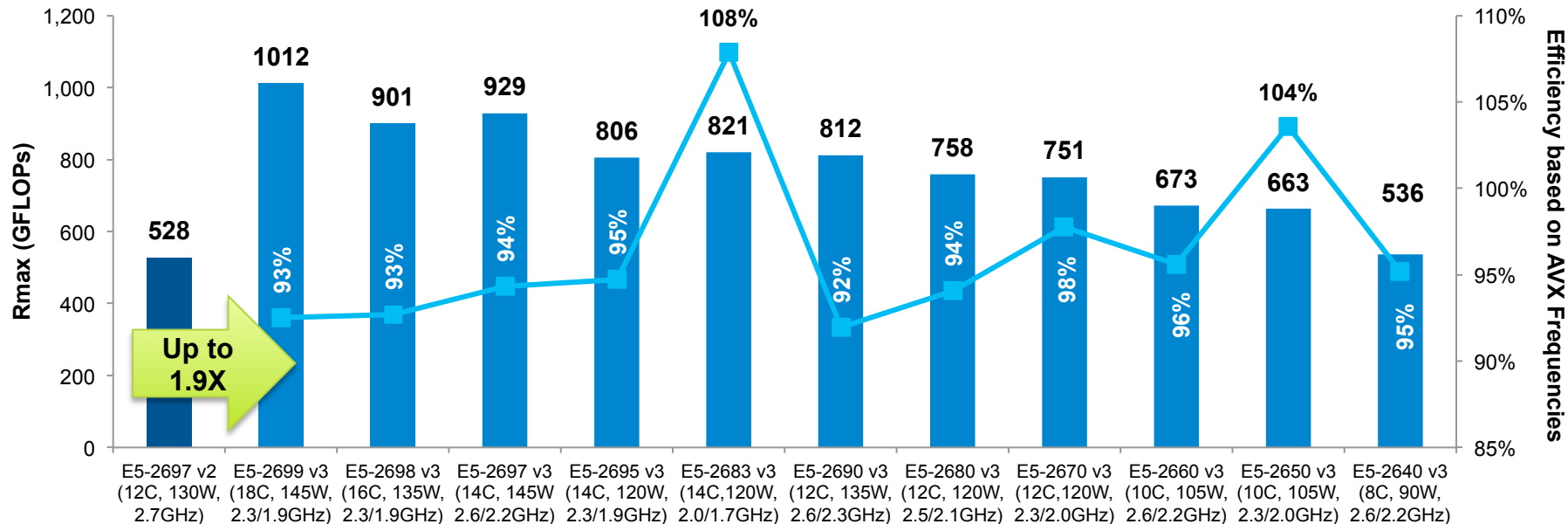


Source as of June 2014: Platform with two E5 v3, HSW-C1, BIOS 27.R01, HT disabled, Turbo enabled, NUMA & COD mode, 8x16GB DDR4-2133, RHEL 6.4, IC14.0-AVX2, MKL 11.1.1. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. **For more information go to** <http://www.intel.com/performance> *Other names and brands may be claimed as the property of others.

Intel® Xeon® Processor E5-2600 v3 Product Family

Preliminary Linpack Performance

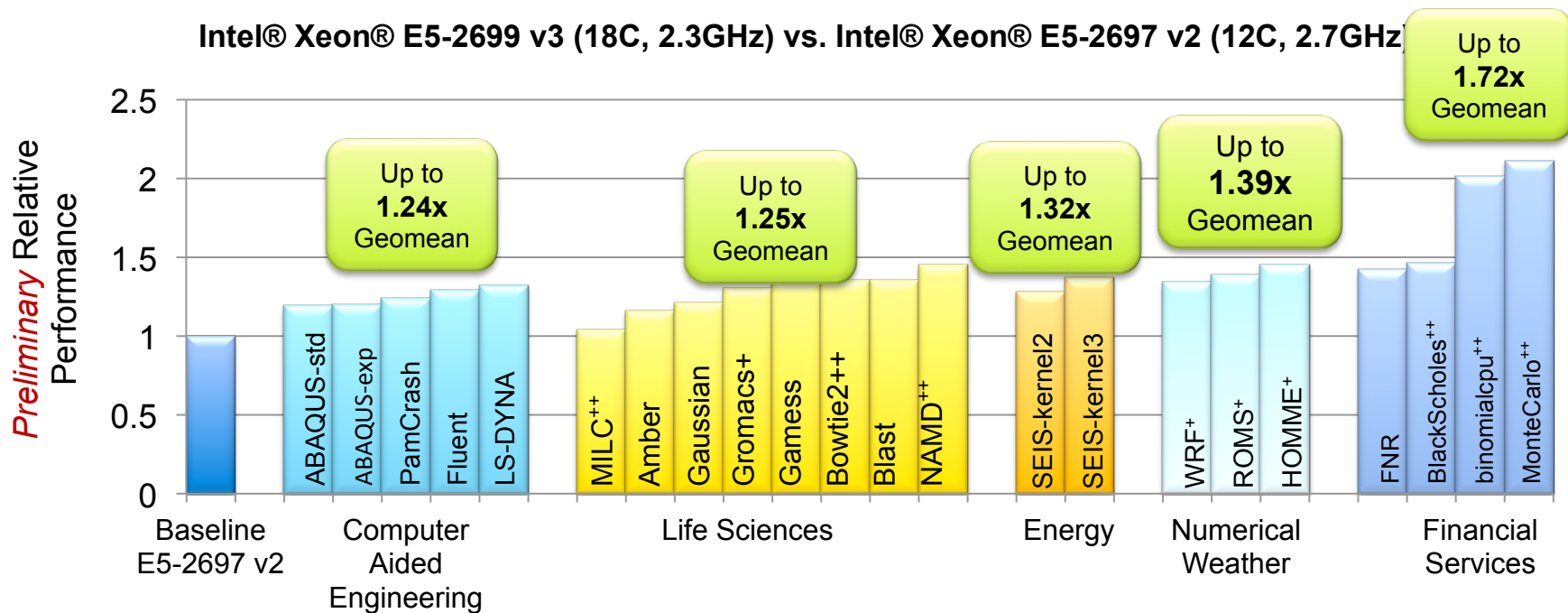
Max Theoretical Peak Performance (DP FLOPS) = 2 sockets x (#cores) x (AVX freq) x (16 DP FLOPS)



Source as of June 2014: Intel internal measurements on platform with two E5-2697 v2, HT disabled, Turbo enabled, 8x8GB DDR3-1866, RHEL6.3, MKL 11.0.5. Platform with two E5 v3, HSW-C1, BIOS 27.R01, HT disabled, Turbo enabled, NUMA & COD mode, 8x16GB DDR4-2133, RHEL 6.4, IC14.0-AVX2, MKL 11.1.1. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to <http://www.intel.com/performance> *Other names and brands may be claimed as the property of others.

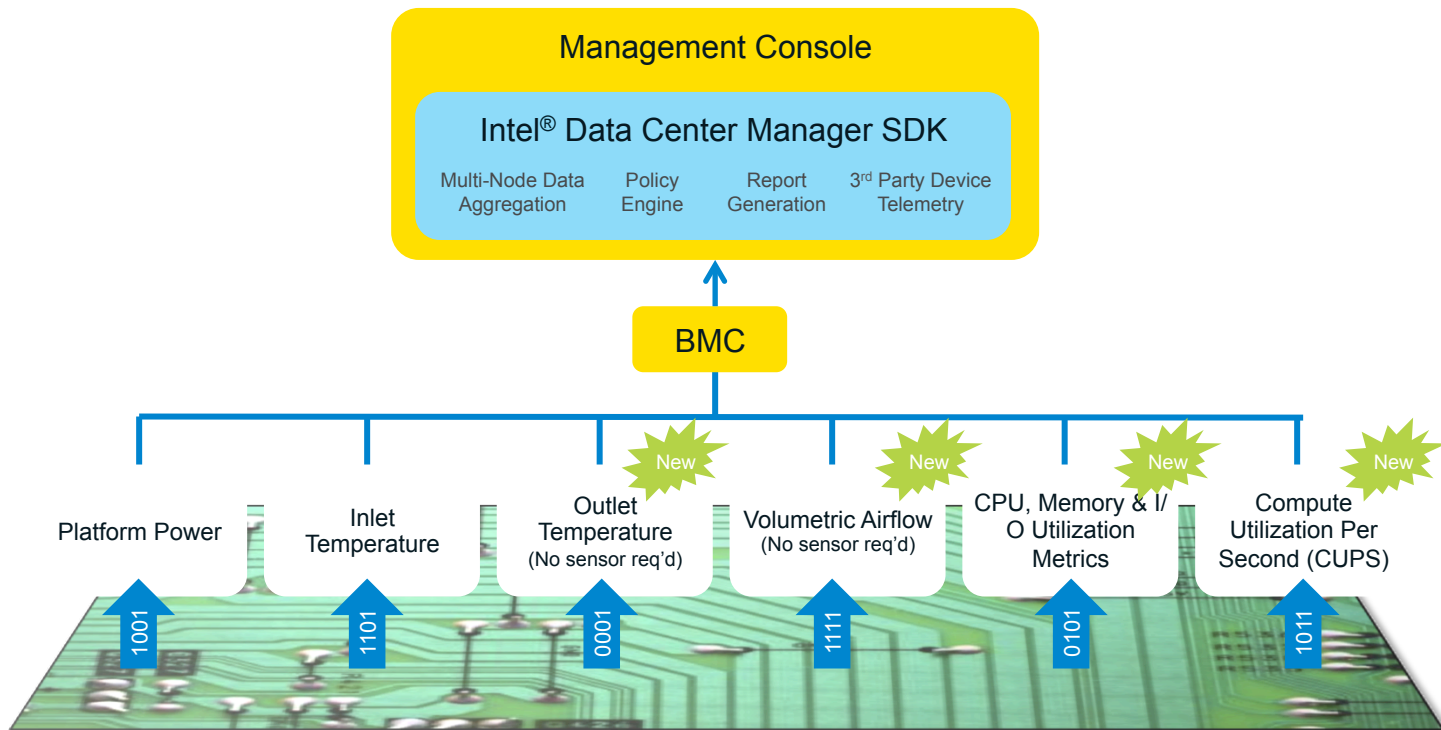
Intel® Xeon® Processor E5-2600 v3 Product Family

High Performance Computing Summary



*Optimized for AVX. **Optimized for AVX2. Source as of June 2014: Intel internal measurements on platform with two E5-2697 v2, 8x8GB DDR3-1866, RHEL6.3. Platform with two E5-2699 v3, 8x8GB DDR4-2133, RHEL 6.3, NUMA-COD mode for all except Energy- ES mode. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to <http://www.intel.com/performance> *Other names and brands may be claimed as the property of others.

Platform Telemetry is increasing: Node Manager 3.0



Modernizing Code on an Open, Standard Road



High-level Abstract

THRU TRAFFIC

Standards: OMP,
MPI...
Portable,
Sustainable

Proprietary HW off ramp:

- No Xeon® optimization benefits
- Very difficult to backtrack to Xeon® and Xeon Phi™ code later

❖ Xeon = Intel® Xeon® processor
❖ Xeon Phi = Intel® Xeon Phi™ coprocessor

*Other names and brands may be claimed as the property of others.

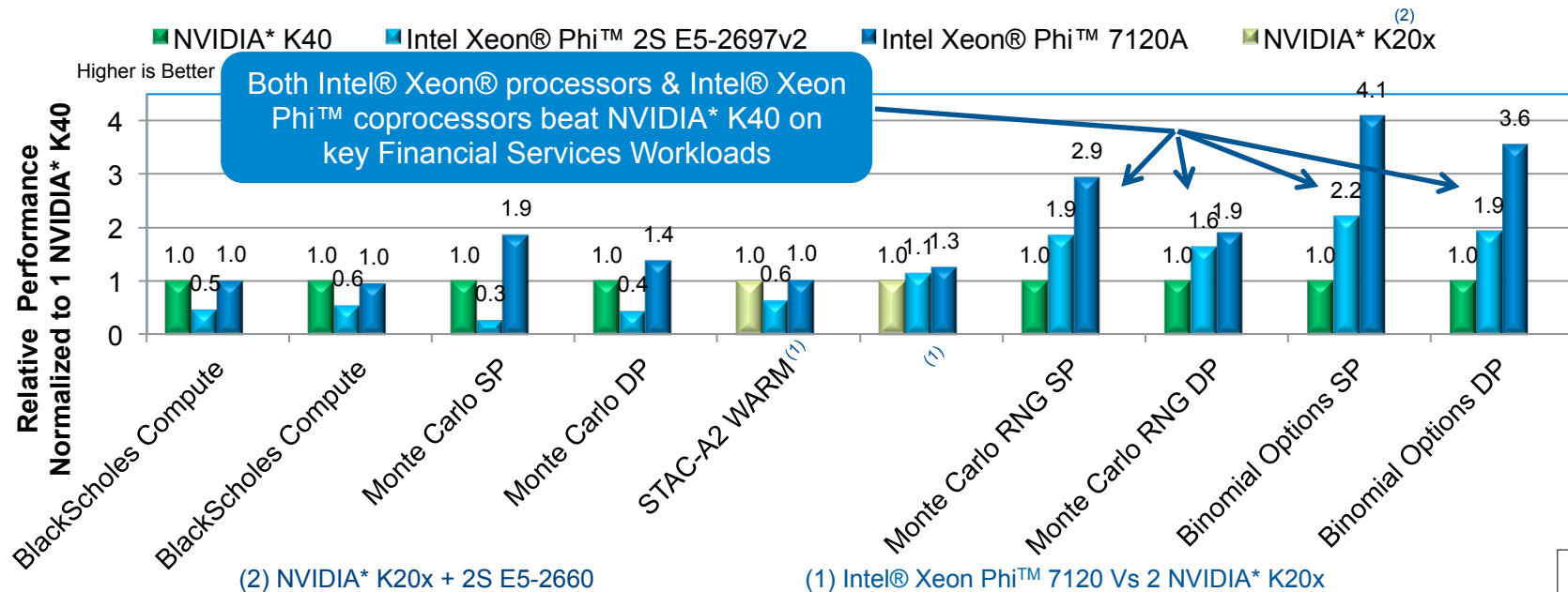


Back-Up

Financial Services Workloads

Intel® Xeon Phi™ Coprocessor 7120A vs. NVIDIA* vs. Intel® Xeon® Processor (E5-2697v2)

Intel FSI Performance



Intel Measured Results: Different hardware architectures may require different source code. Results are based on Intel's best efforts to use code optimized to run best on all architectures and perform the same work. Future code optimizations may result in different results.

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Source: Intel measured as of Jan 2013. Configuration Details: Please see slide speaker notes. For more information go to <http://www.intel.com/performance>

*Other names and brands may be claimed as the property of others.

Config. Summary

IC 14.0 U1
MPSS 6720-16
ECC on
Turbo On (7120P)
CUDA 5.5 (875MHz
boost Enabled)

Strategic Benefits – Intel® Xeon Phi™ Product Family

- **Significant speedup** for highly parallel workloads based on threads, vectors, and memory bandwidth
- **Same source code**, programming languages, tools, and techniques as the Intel® Xeon® processor
- Supports **native and symmetric execution** models (not supported by GPU) since it's a coprocessor
- Optimization efforts for Intel® Xeon Phi™ coprocessor also benefit Intel® Xeon® processor (AKA “**dual-transforming-tuning advantage**”)
- Knights Landing will be a bootable processor with high bandwidth memory, up to 72 cores, two 512b wide vector units per core, and **binary compatibility with future Intel® Xeon® processors**
- **Best way to be ready for Knights Landing is to get your apps optimized on Intel® Xeon Phi™ coprocessor**
 - Applications optimized for Intel® Xeon Phi™ coprocessor will see benefits transferred to Knights Landing with just a recompile

Executive Summary

- We have kept in mind customer's "grid" environment and their system admins heavy focus on maximum utilization of all compute resources
- With this environment in mind, we are offering the following elements:
 - A compelling set of performance proof-points Vs K40 which are being shared publicly
 - Standard programming tools and techniques which eliminate a heavy lift for developers
 - Execution models (not supported by GPUs) that enable higher number of compute cores
 - Collaboration with your preferred OEM for test systems/cluster
 - Support for parallelizing customer's code for Xeon and Xeon Phi on significant deals
 - Value for investment now on Xeon/Xeon-Phi and continuity with future Xeon Phi products
- We believe that the mantra now is "to maximize your ROI, you must parallelize your code."