The Serial Link Processor for the Fast TracKer (FTK) at ATLAS

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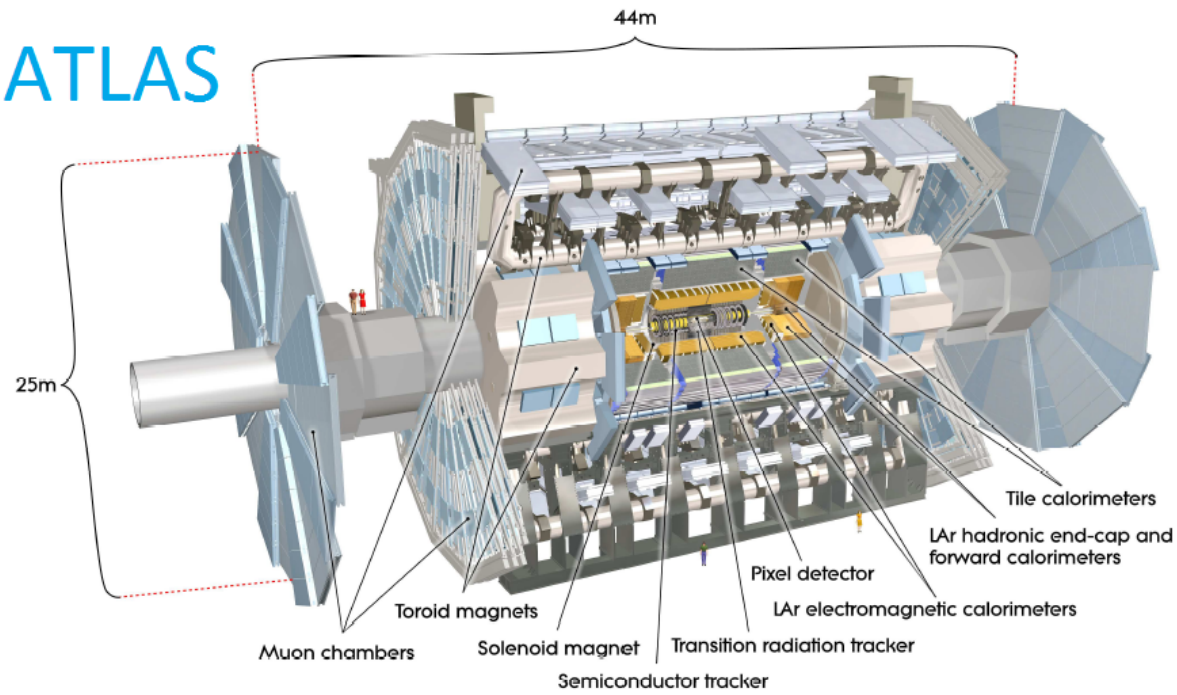
Fellow at INFN

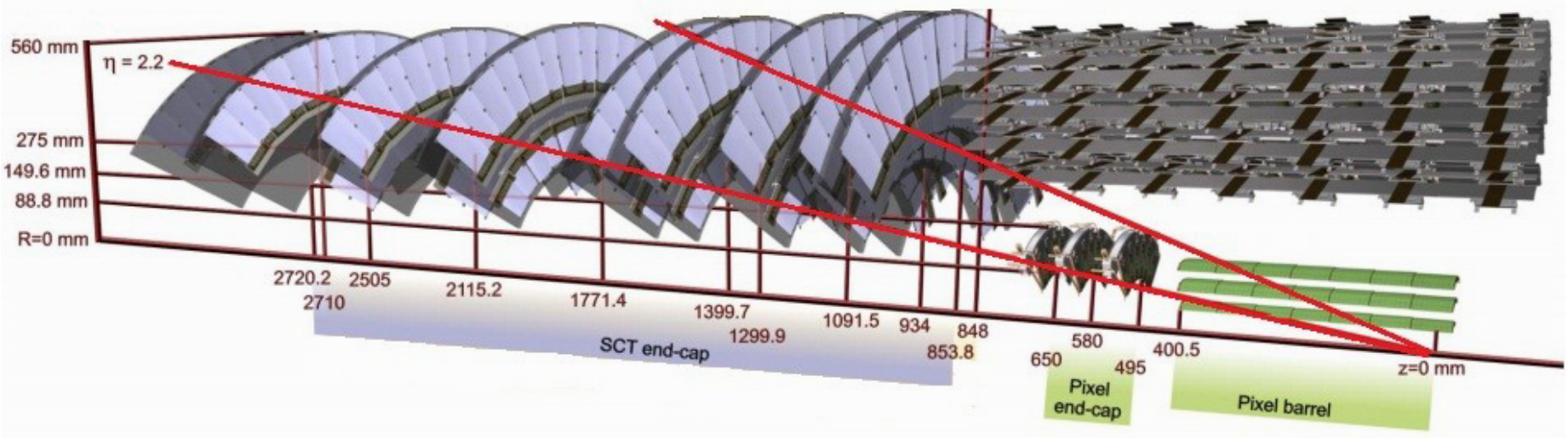
Outline

FTK: the Online Silicon Detector Tracker for ATLAS upgrade

- FTK reconstructs charged particle trajectories in the silicon tracker (Pixel & SCT) at "1.5" trigger level.

- Extremely difficult task
  - 25 ns inter-bunch time ~70 pile-up events at top luminosity.





An online silicon detector tracker for the ATLAS upgrade

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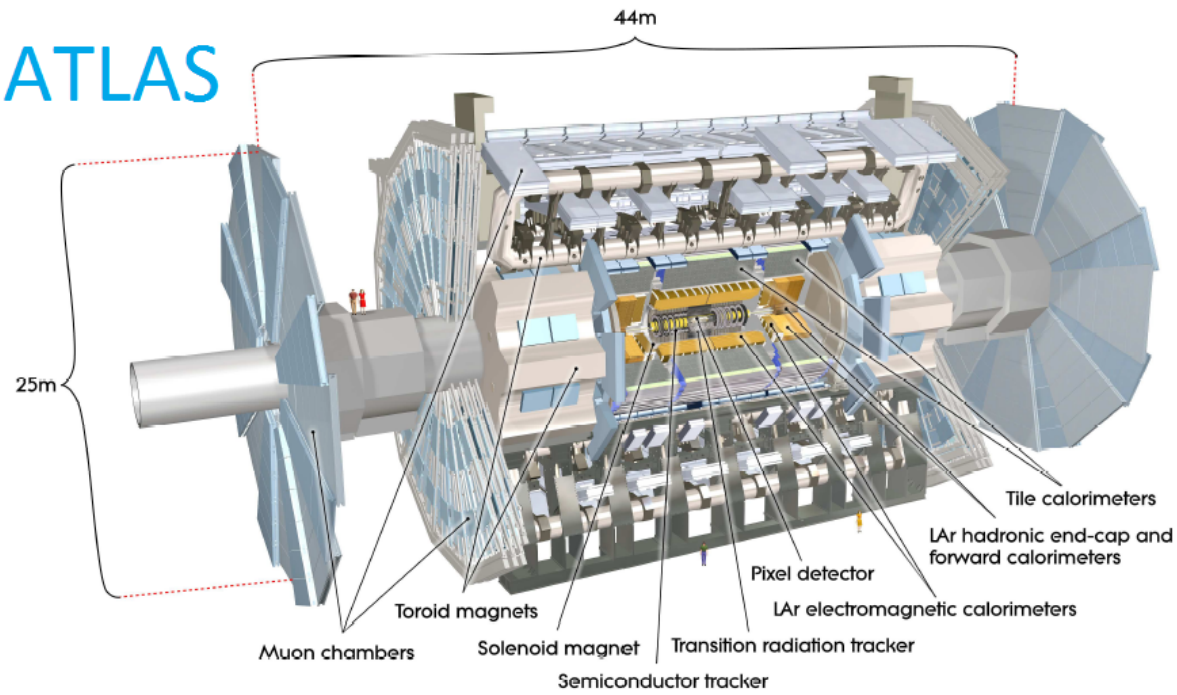
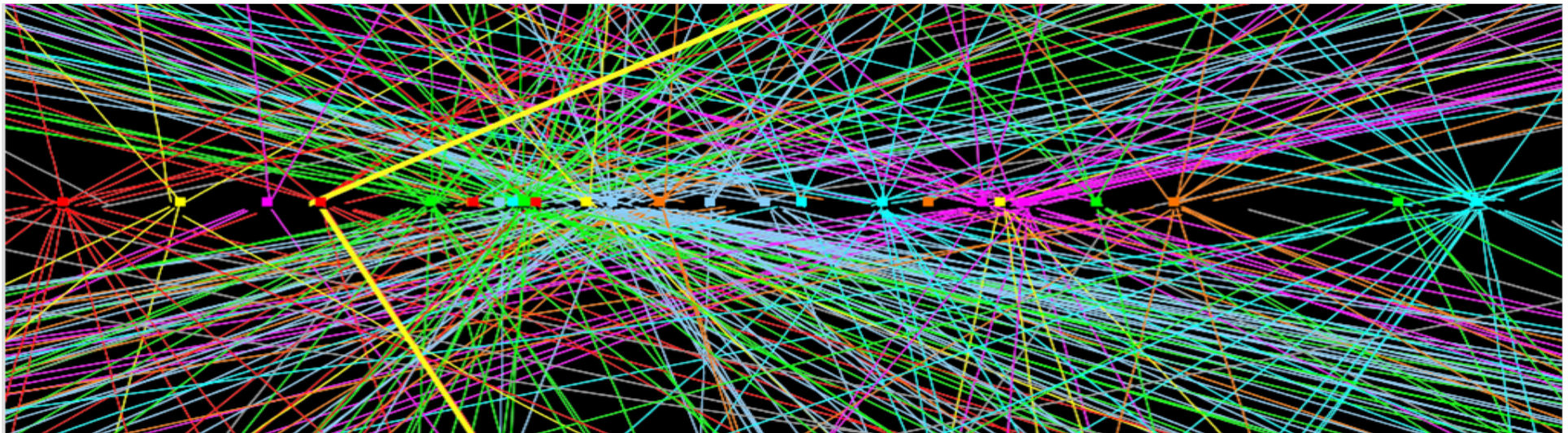
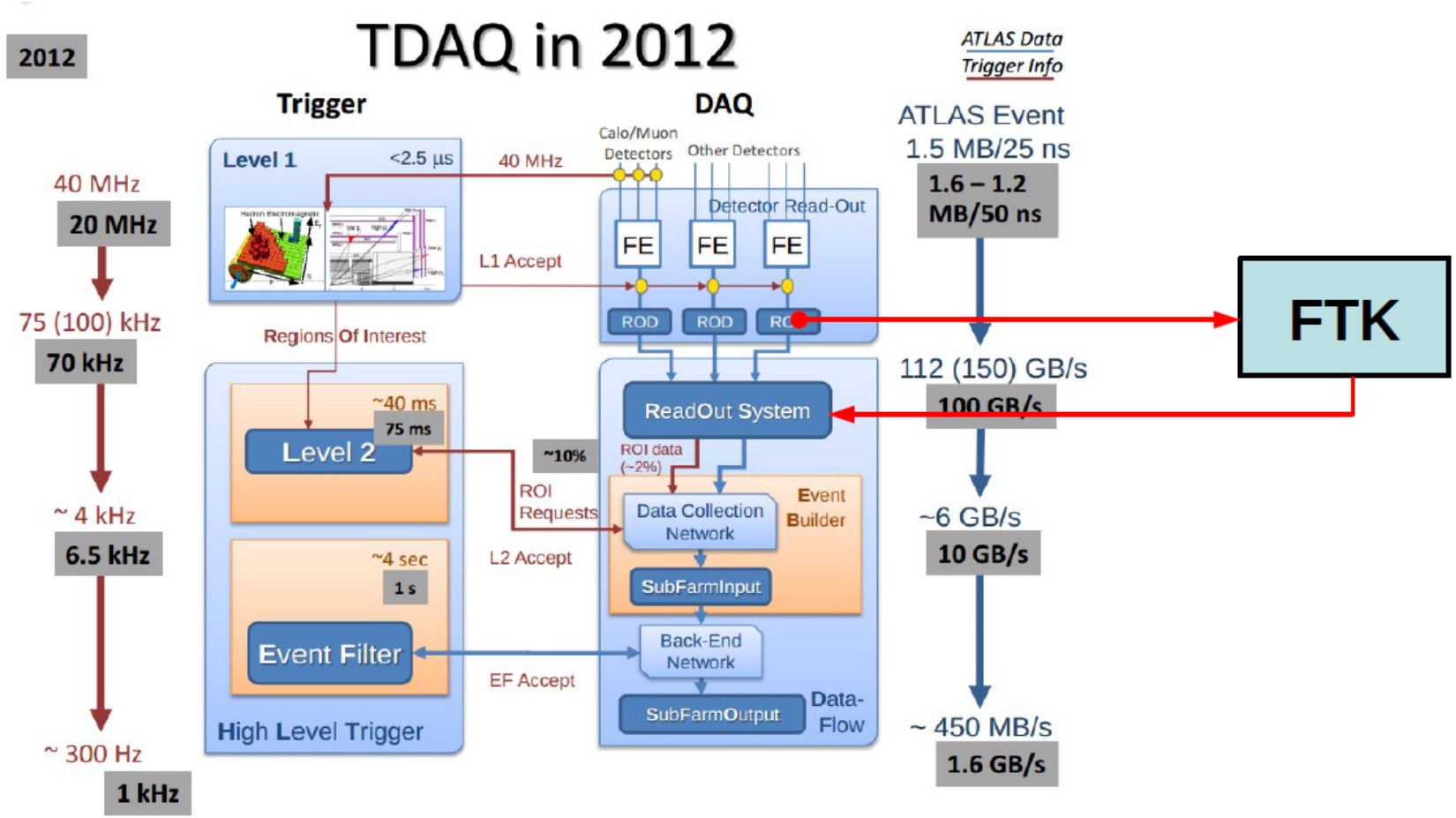




“1.5” Level Trigger processor

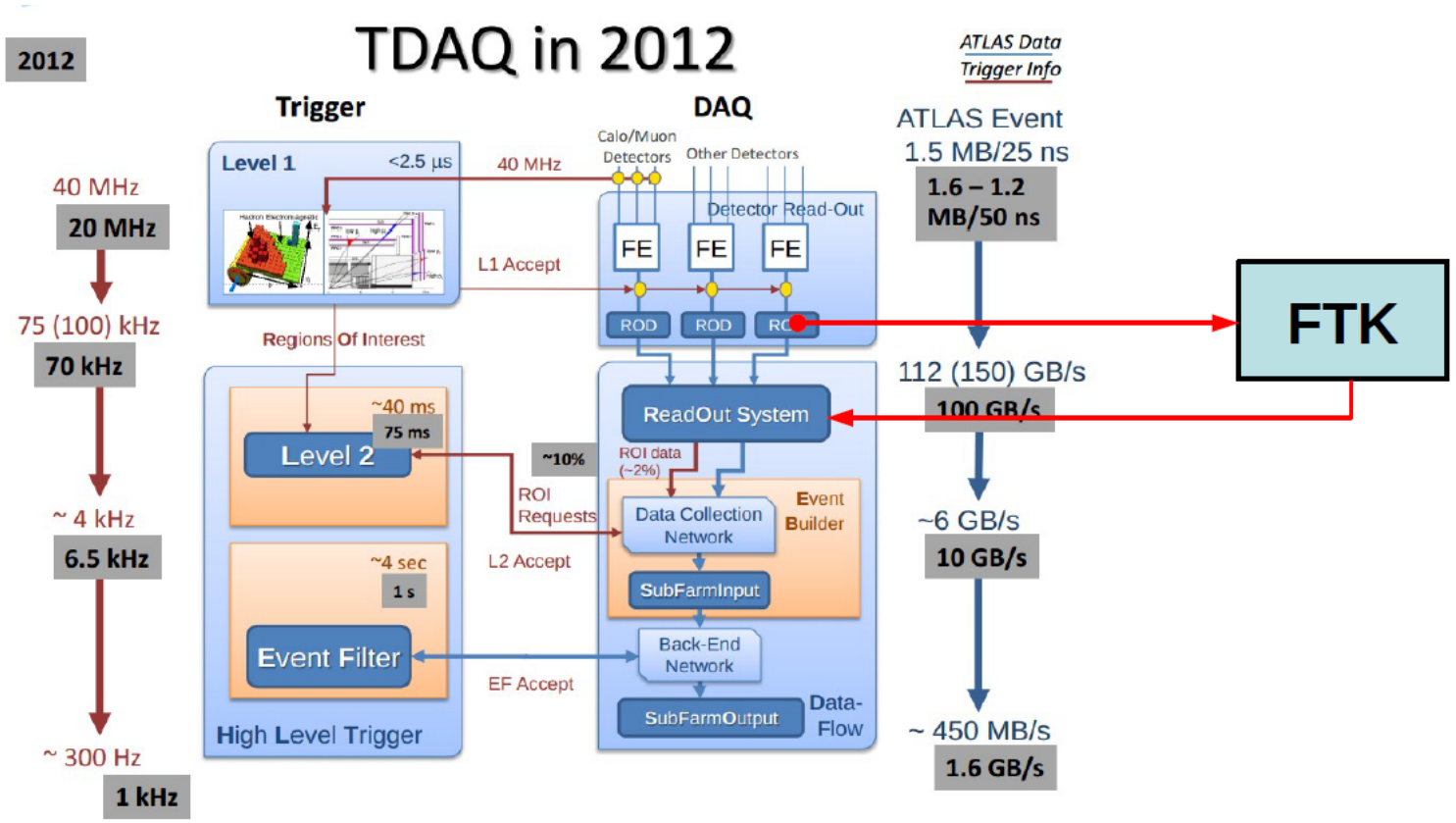


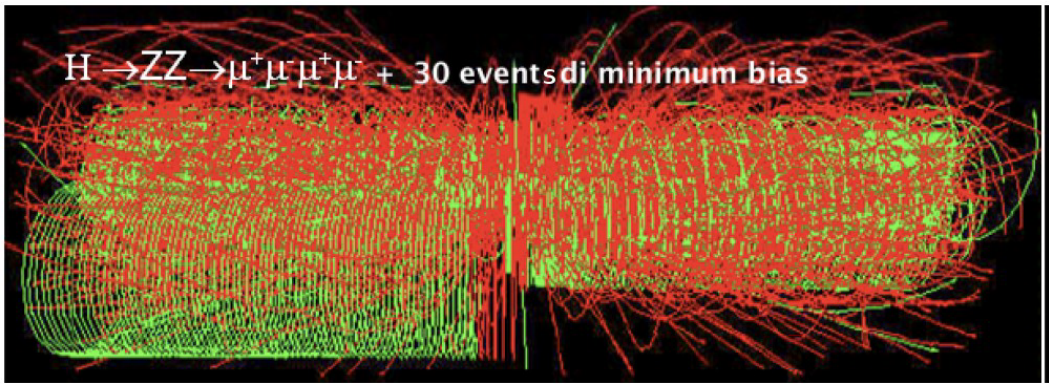
- Silicon data currently used only locally (ROI) and late in Level 2.

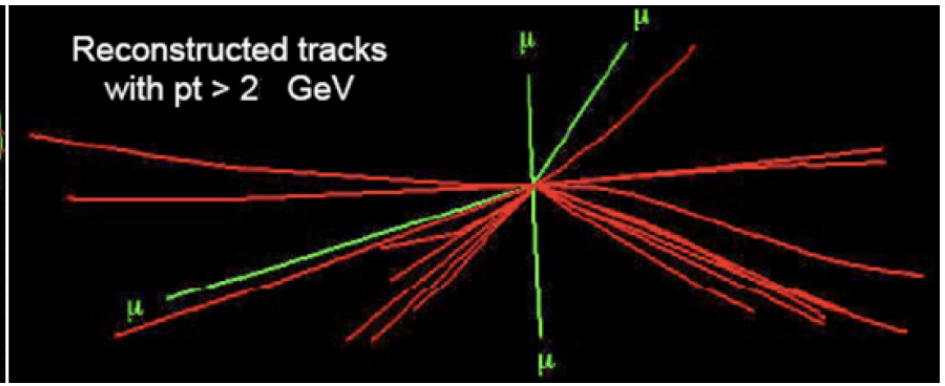
- FTK reconstructs all tracks with pT>1 GeV/c in time for Level 2.

- Track parameters are computed with full detector resolution.

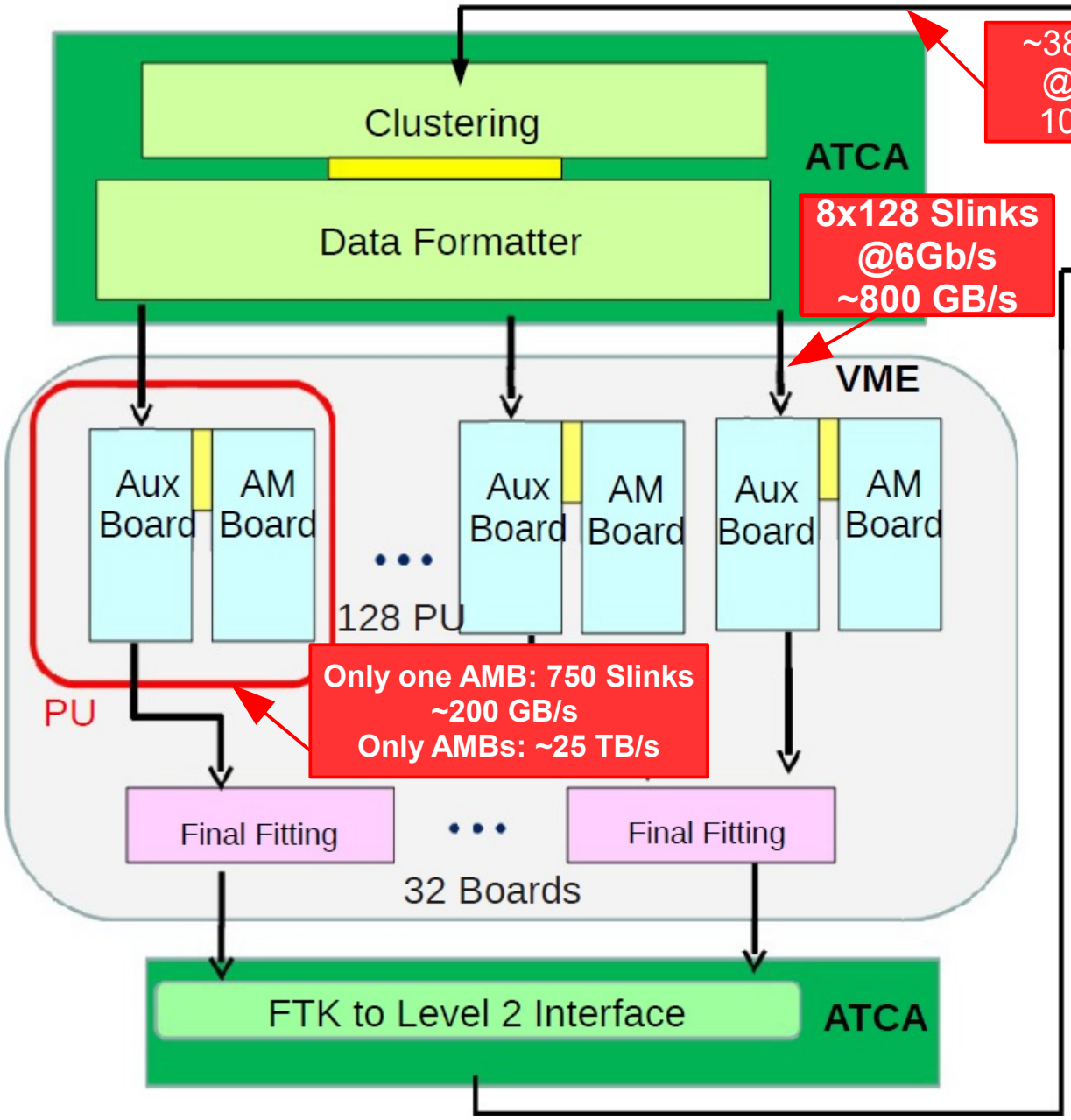
“1.5” Level Trigger processor

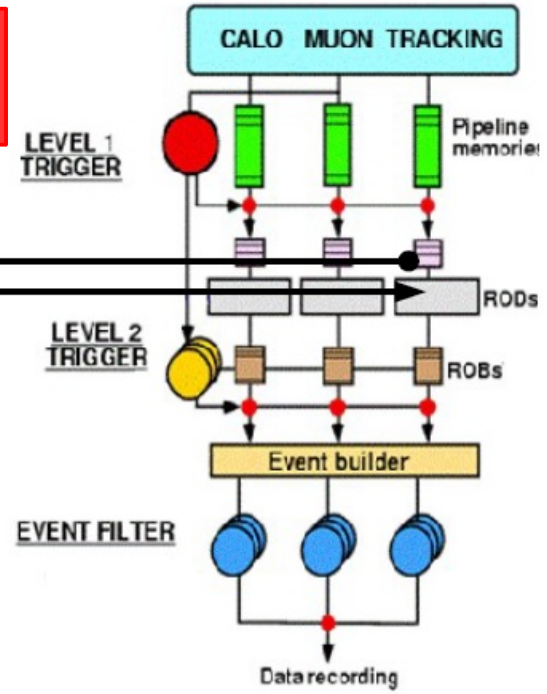






FTK architecture

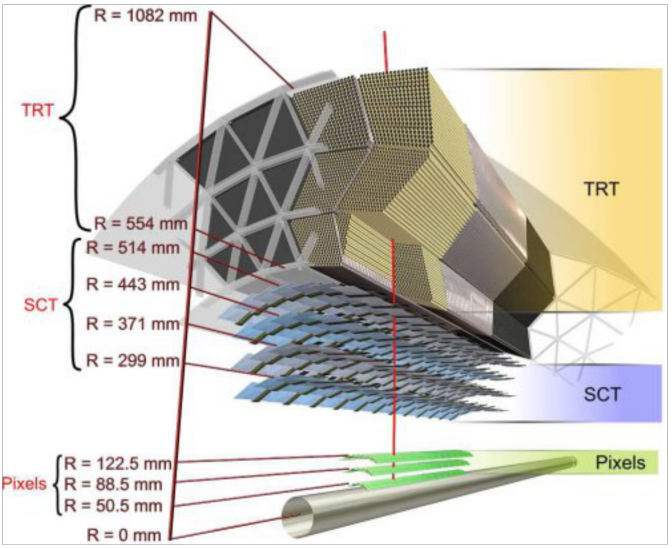


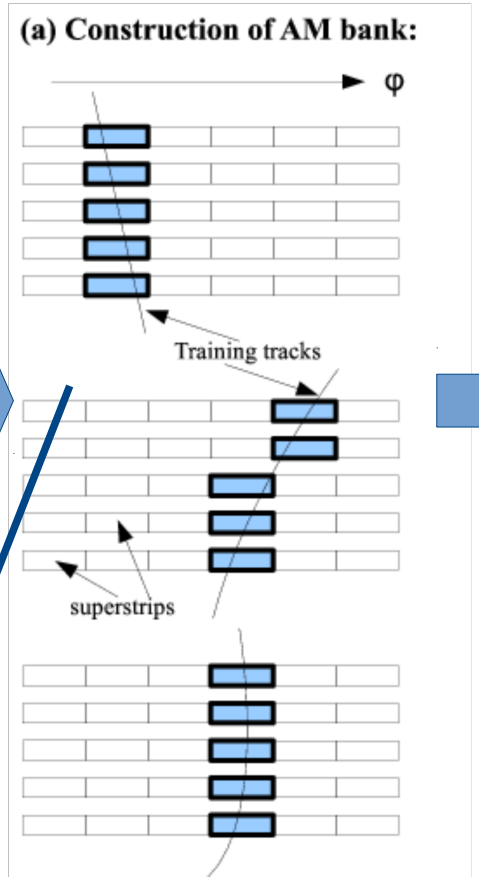


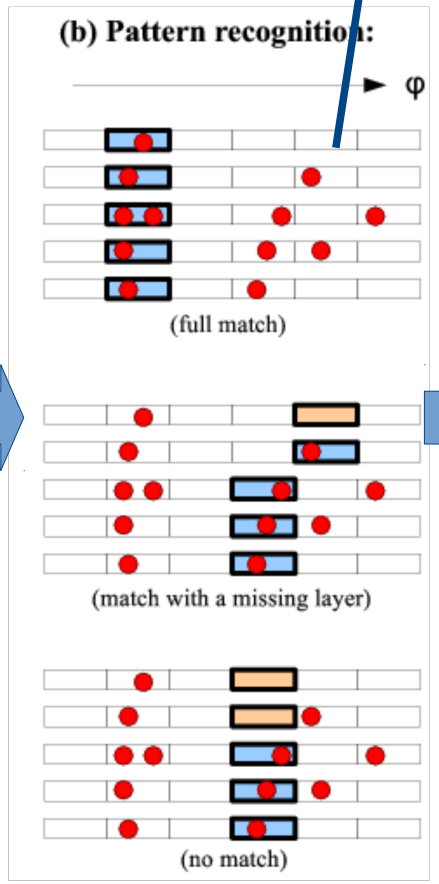
- 5 ATCA crates (clustering on silicon)
- 8 VME Crates:
  - 128 Processing Unit (track reconstruction)
- Total of ~1500 FPGAs, ~8200 AMChips

Pattern Matching & Track Fitting

- The Fast TracKer is an hardware processor that perform the on-line track reconstruction.
- Two sequential steps:
  →***pattern matching*** & the track fitting







The input Hits are compared with the pattern bank.

Roads
Matched pattern

Definition of pattern bank: list of low resolution candidate tracks.

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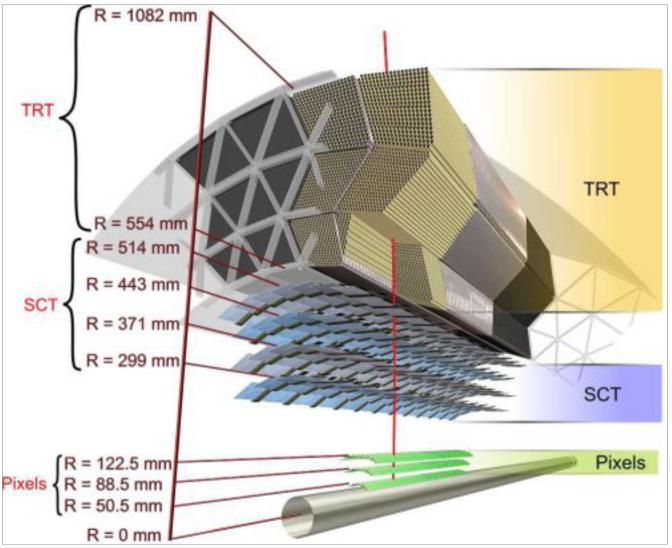

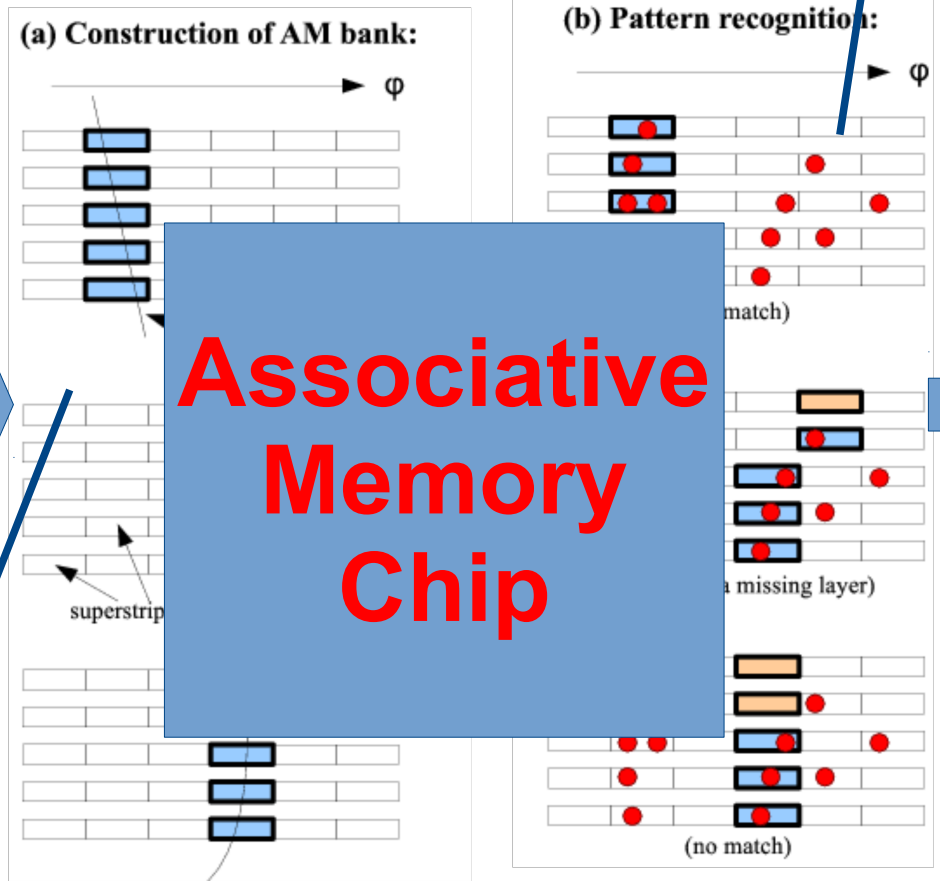

Associative Memory Chip

The input Hits are compared with the pattern bank.

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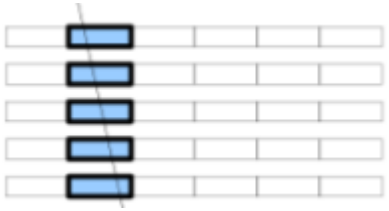
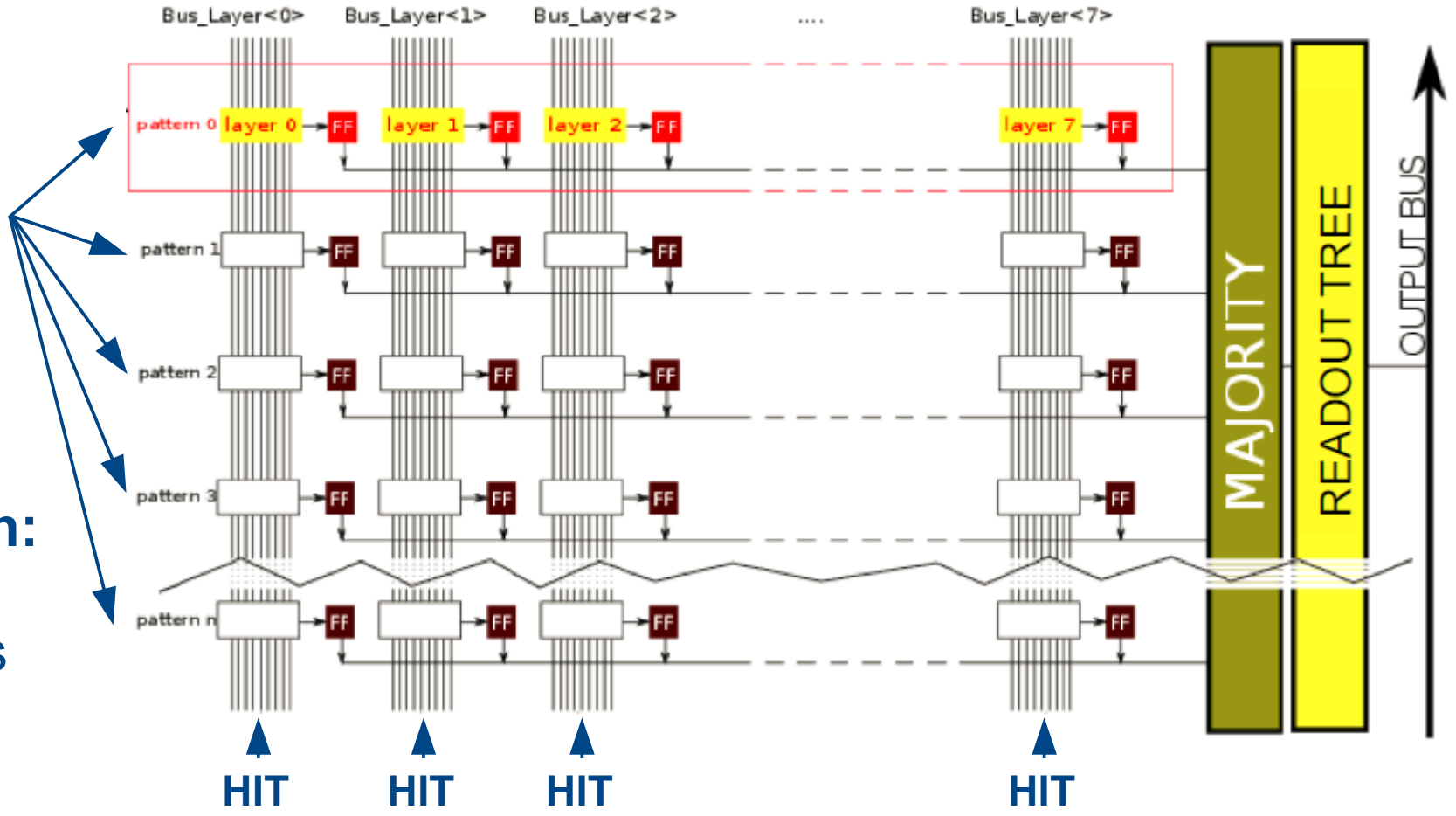
AM chip working principle

Pattern

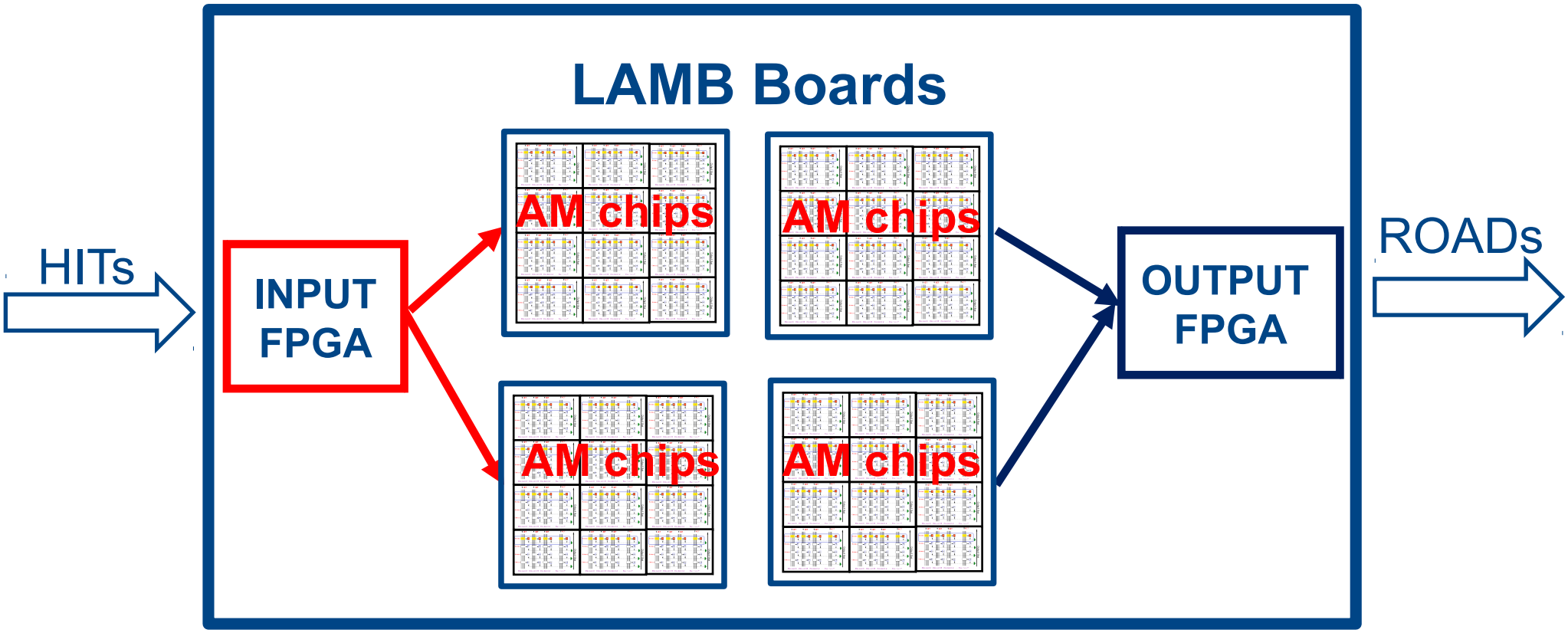




AM chip consumption:
~ 2.5 W for
128 kpatterns

AM chip computing power:
Each pattern: 8*16 (o 4*32) bits comparators
Each 10 ns 128 kpat *4 = 500 K instructions → 500 K * 100 M = 50 10^6 MIP/CHIP
- $3.2*10^9$ MIP/AMB (64 chips)
- $4*10^{11}$ MIP in the whole AM system

Associative Memory Board



- The **Input FPGA** distributes silicon **HITs** to the 4 **LAMBs.**

- The **Input FPGA** monitors the **HITs** format to check the end event and the errors in the data

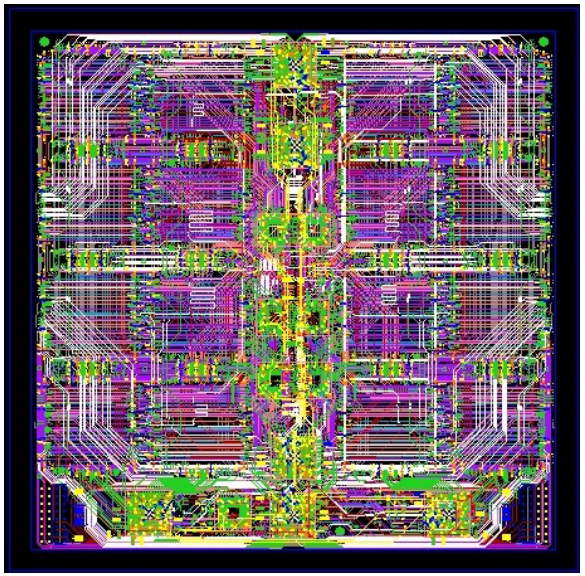
- The matched **ROADs** are collected from the **OUT FPGA**

- The **OUT FPGA** creates the end event word

Recent developments of the Associative Memory chip

AM chip 04:

- Package: PQ208
- Parallel I/O interface
- 8k patterns
- Crazy routing of LAMB



More performance needed with the new AMChip06:

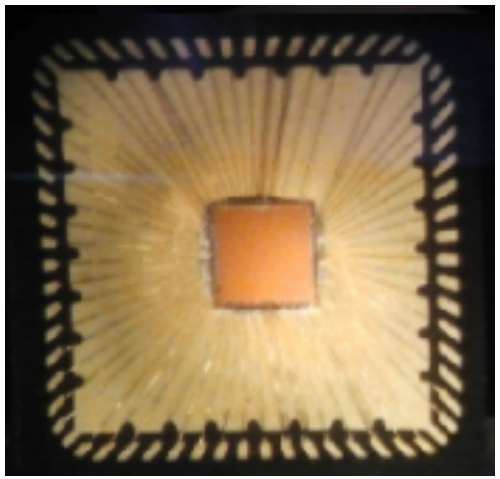
- Increase the number of pads.
- Use BGA package for more pins
- Simplify LAMB routing

Idea: **serial link** to transmit the data

Associative Memory Chip - Family 05

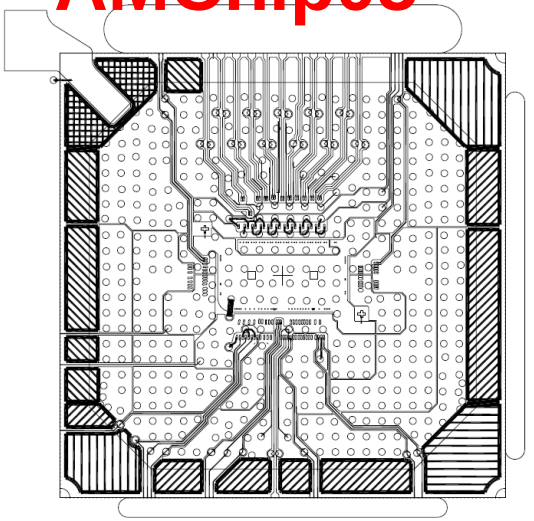
We bought a *IP-CORE* to provide the *chip* with serialisers and deserialisers.

MiniAMChip05



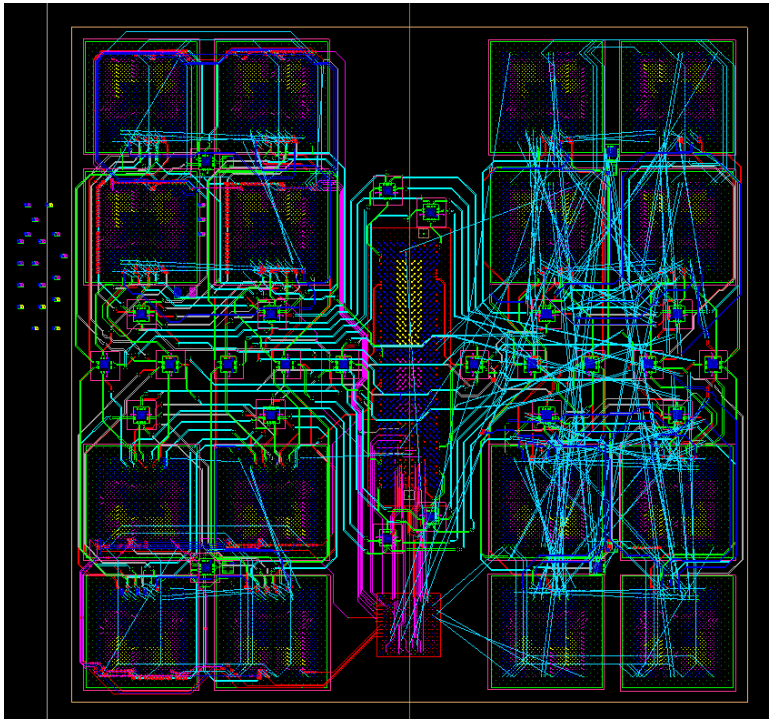
Package: QFN 64
Die: 3.7 mm^2
Board: MiniLAMB-SLP
Status: under test

AMChip05



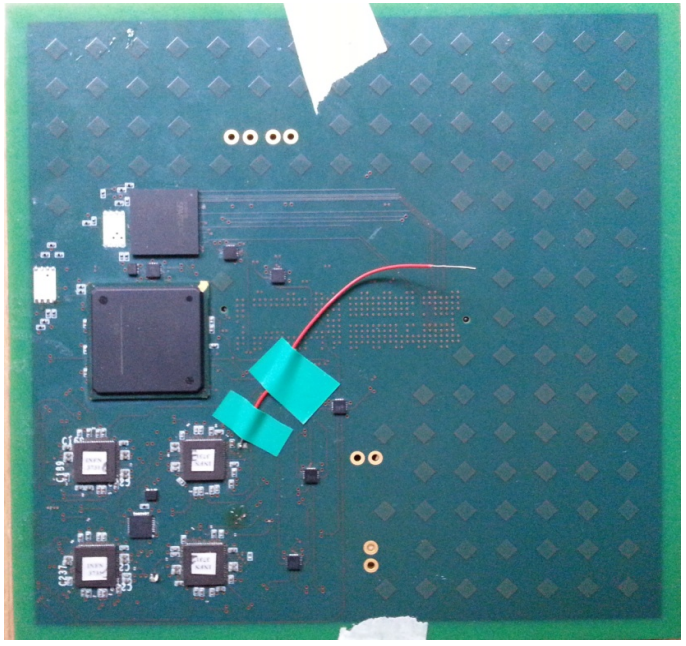
Package: BGA 23 x 23 mm
Die: 12 mm^2
Board: LAMB-SLP
Status: submitted

MiniLAMB-SLP & LAMB-SLP



- The final LAMB-SLP board will be ready in short time.
- In one LAMB-SLP board will have 16 Amchips.
  → for a total of ~2 M of **patterns**
- The routing is simplified.

- This is a prototype of **LAMB-SLP** board with 4 **MiniAM chips**.
  → This board is important to confirm our idea and our solution on **Serial Link**.



MiniLAMB-SLP & LAMB-SLP

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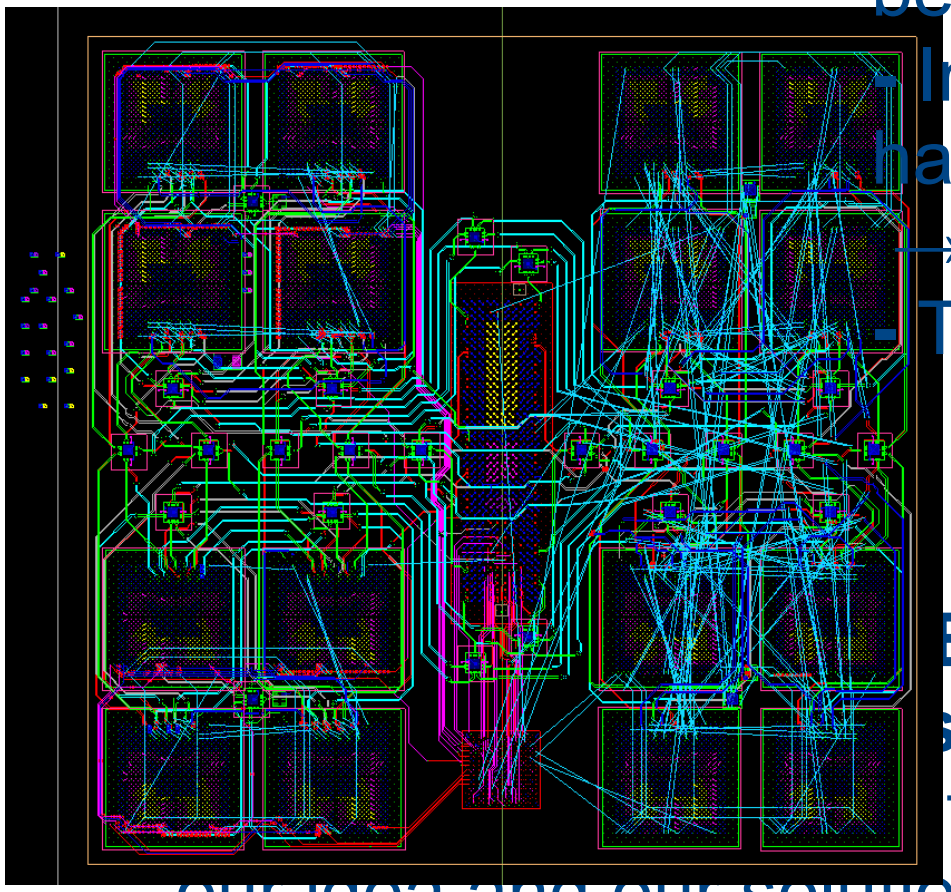

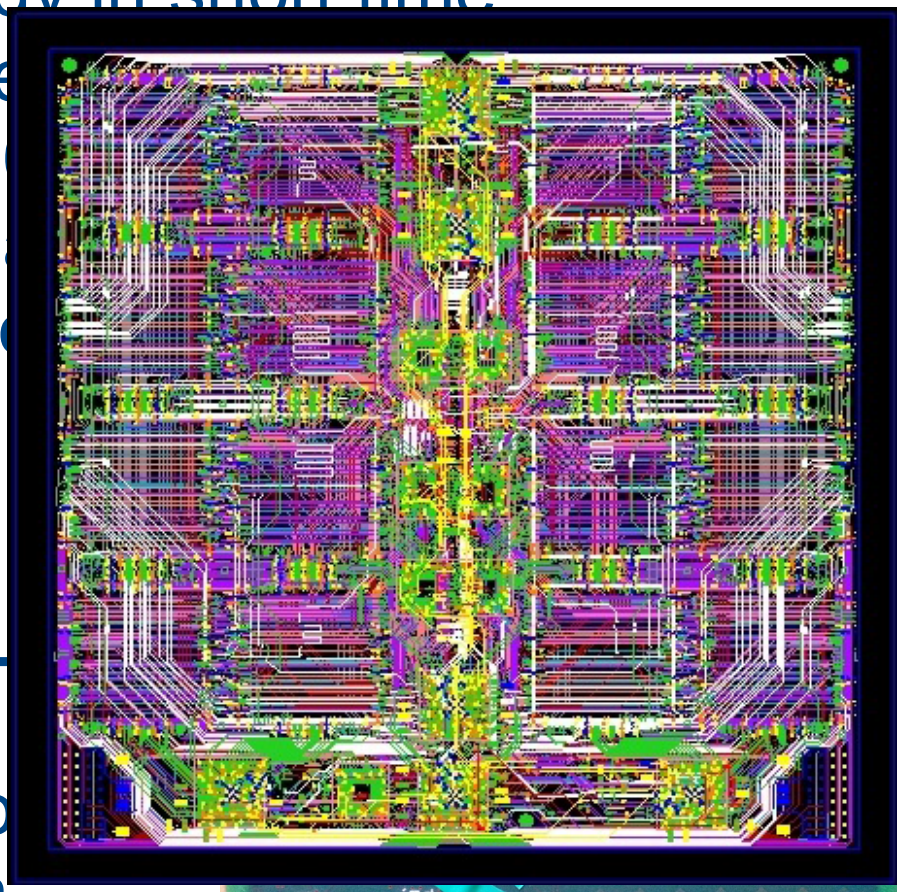

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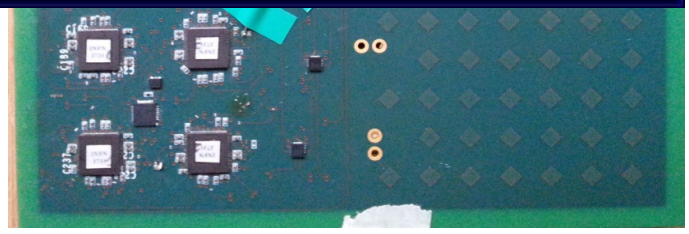

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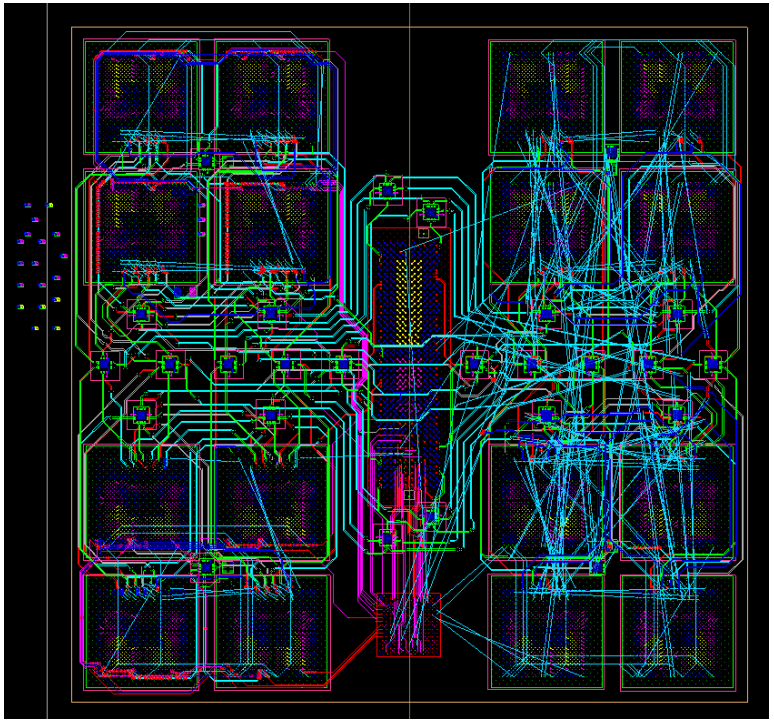

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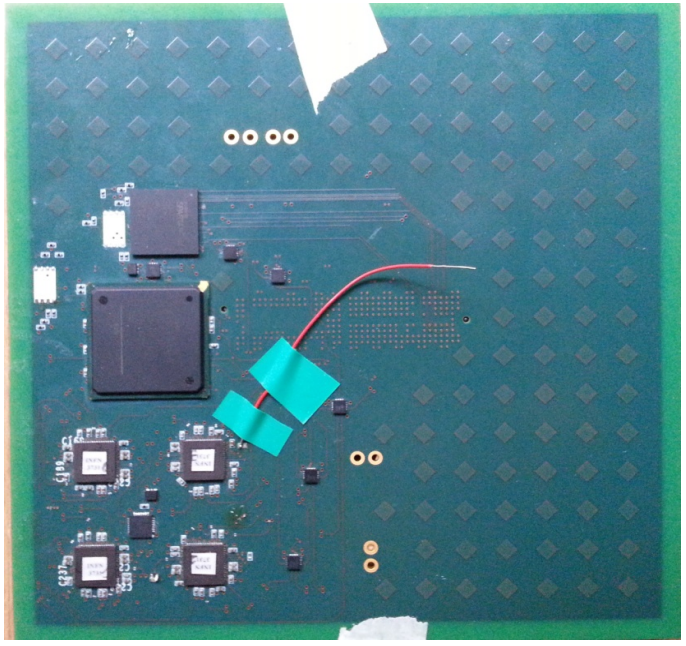
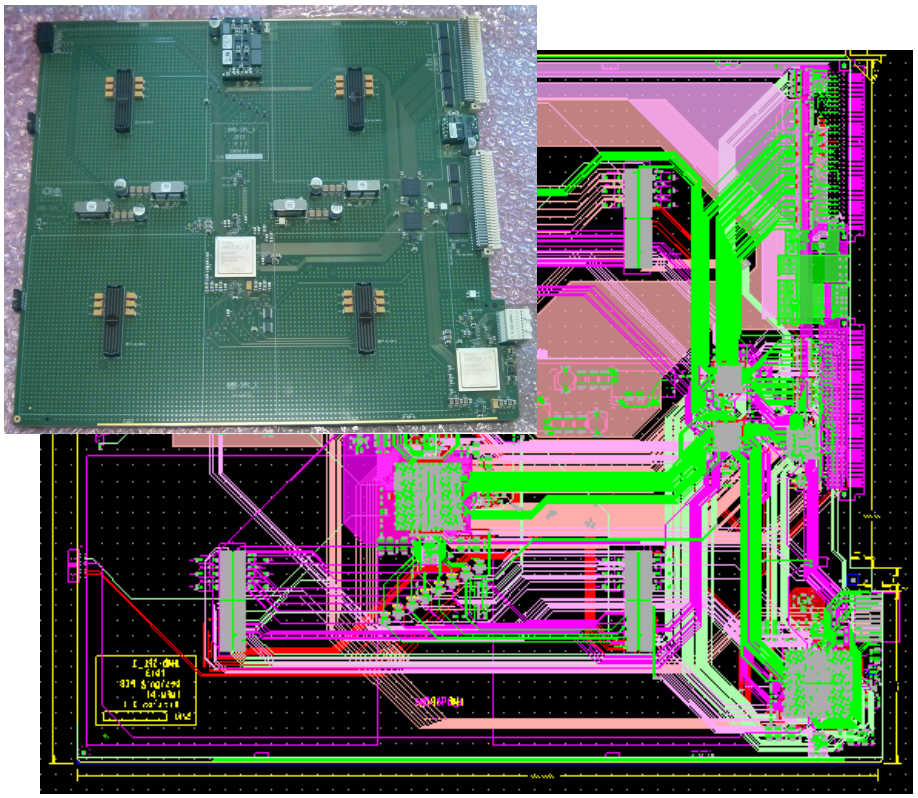


AMB-SLP board

The AMBSLP (Serial Link Processor) board design:



Interface:

- 12 input buses @ 24Gbps
- 16 output buses @ 32Gpbs

Three FPGA:

- 1 for the input data distribution (ARTIX-7)
- 1 for the output data distribution (ARTIX-7)
- 1 FPGA for the data control logic (SPARTAN 6)

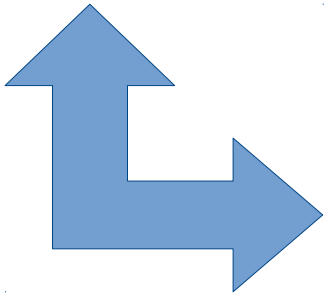
We used only serial standard for data distribution to and from the AM chips

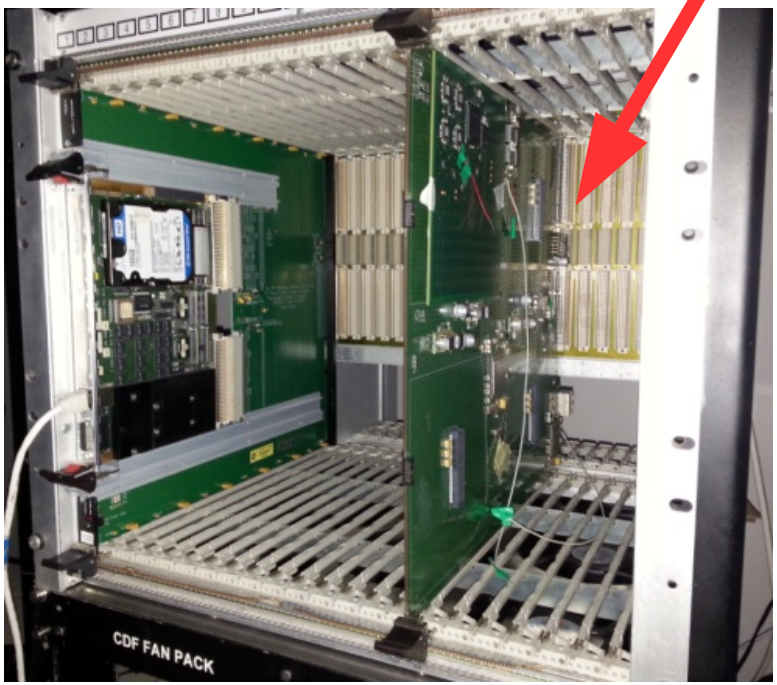
Test Stand

Complete test with:

- AMB-SLP board.
- MiniLAMB-SLP board.
- Crate VME.
- CPU TDAQ 4.

Strobe

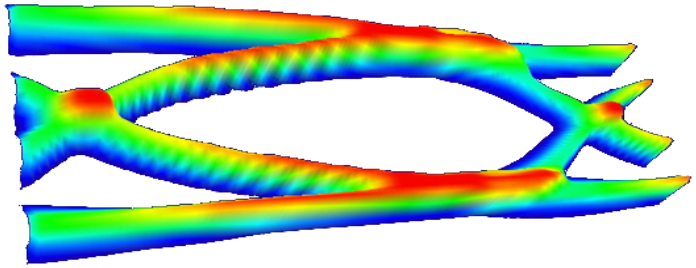




- We perform a Serial Link's test with a PRBS Generator.
- We used a IBERT core in Xilinx's ISE.

Serial Links

Both input and output serial links characterized for signal integrity.



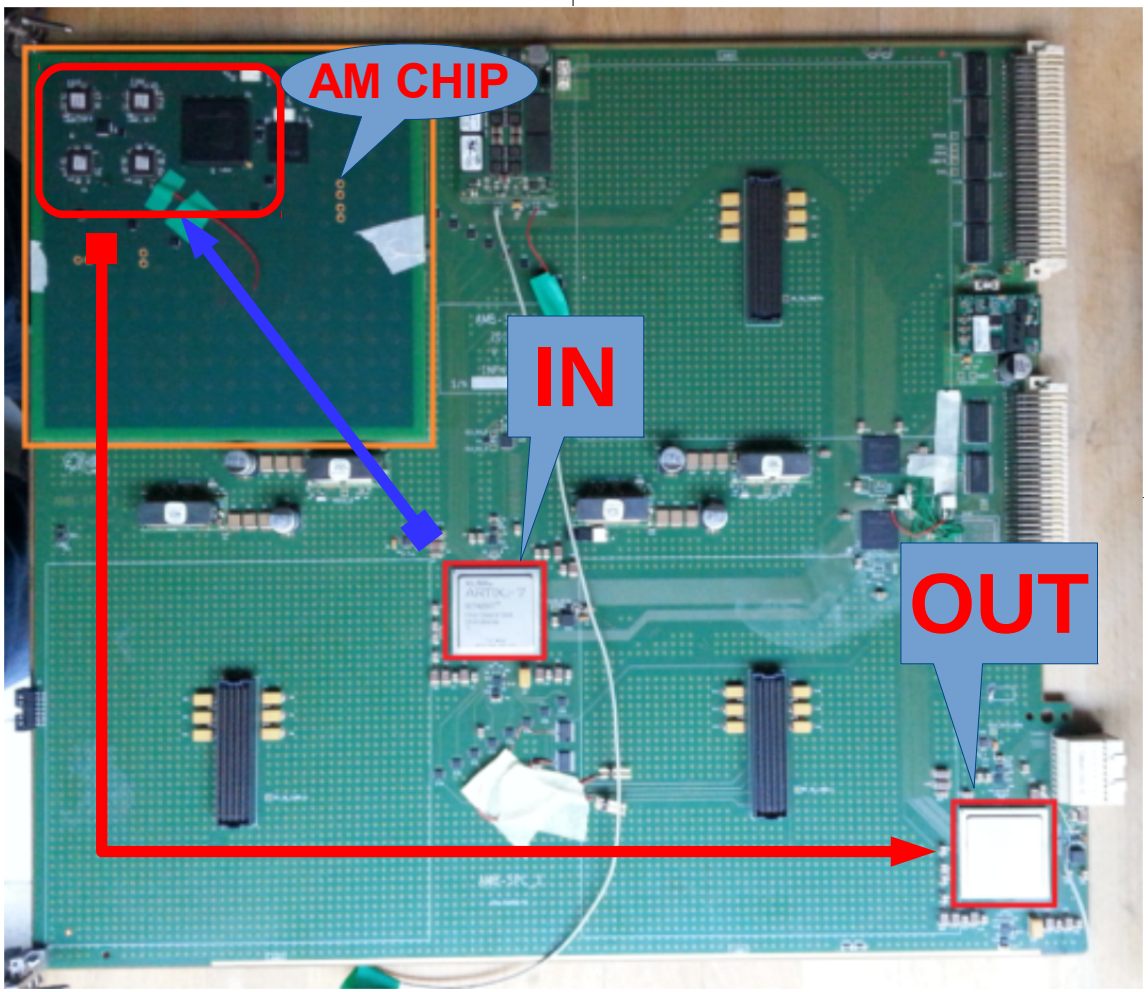
- Serial Link @ 2 Gb/s

→ Input path

- FPGA to FANOUT to AM Chip
- Intermediate buffers

→ Output path

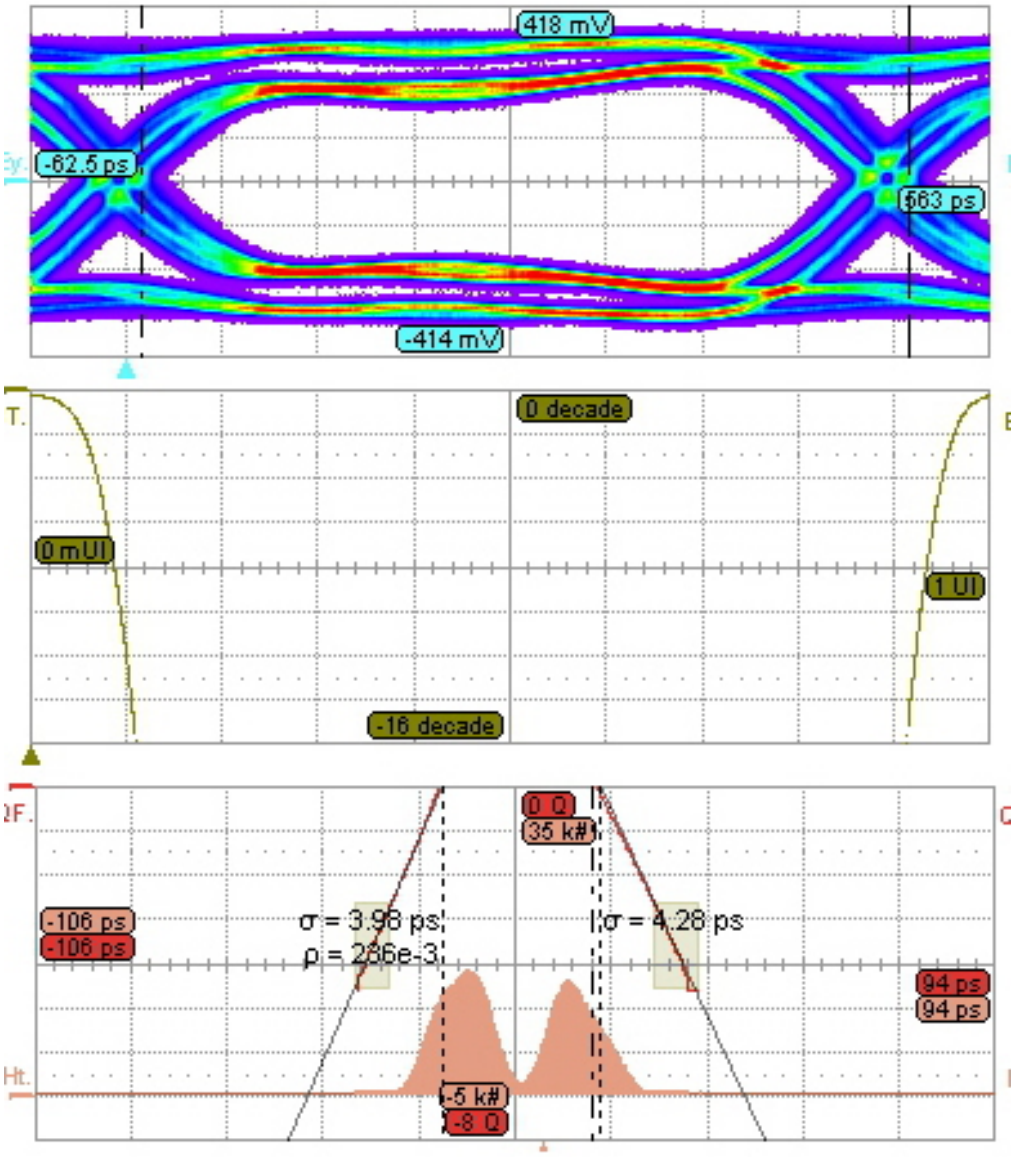
- AM Chip to FPGA
- Intermediate repeater



Result

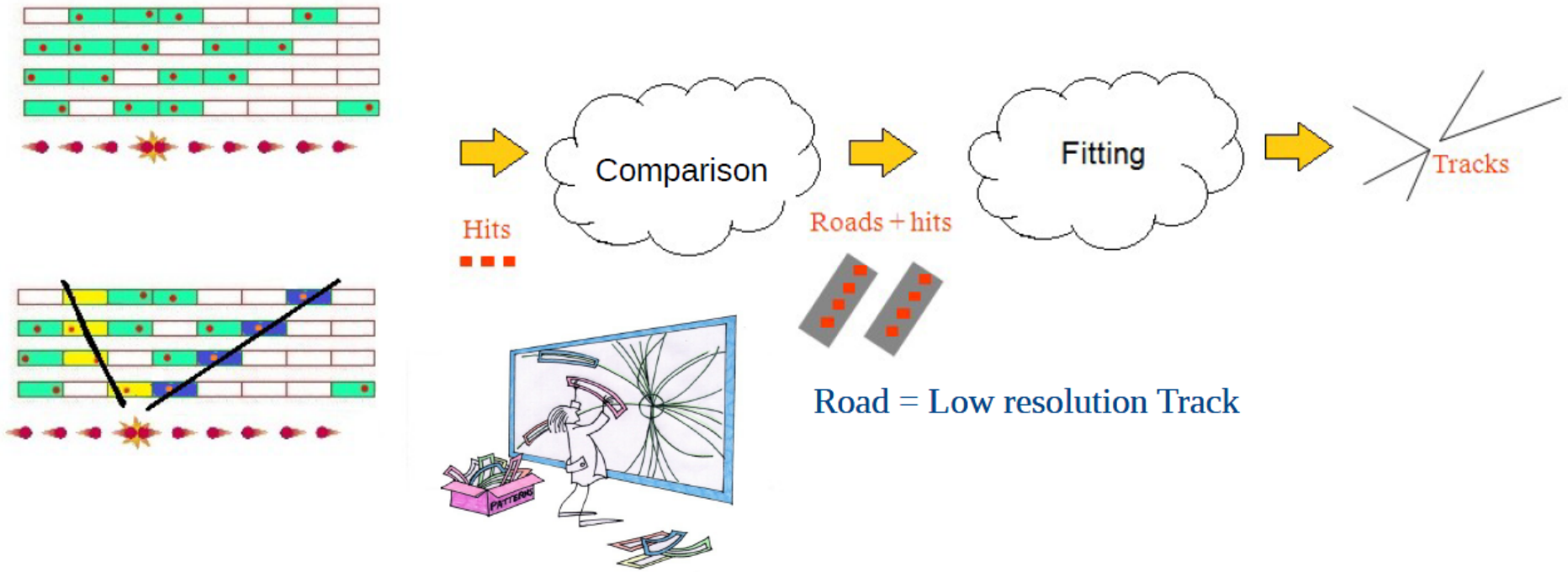
- Types of measure:
.Jitter Analysis
.BER
.Eye diagram

- Send PRBS data:
PRBS checker
BER < 10^{-14}



Conclusion

Pattern Matching

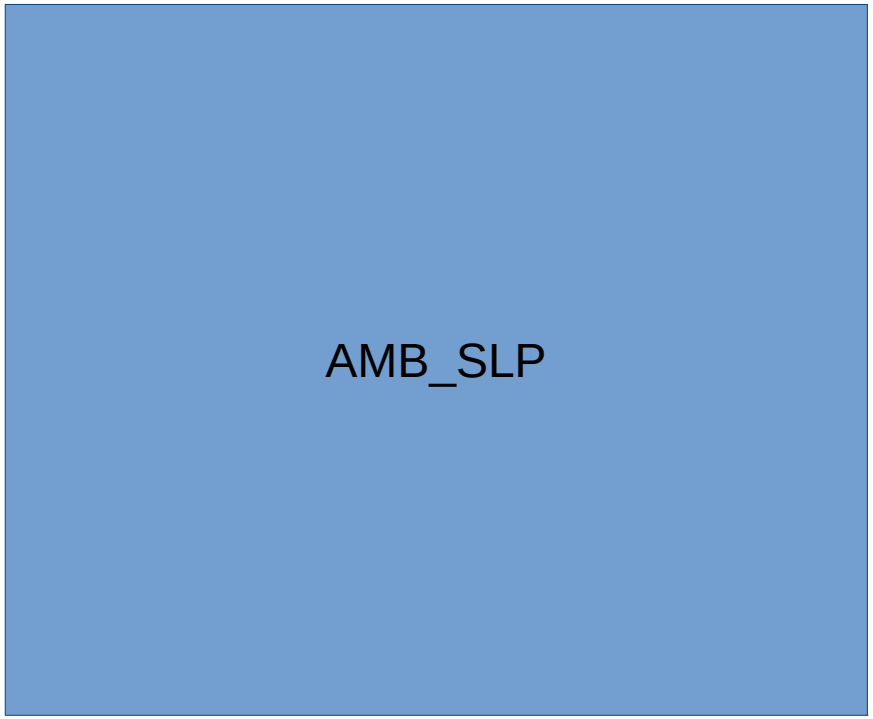


- Pattern Bank: All the possible patterns (low resolution real track candidates) are precalculated and stored in the Pattern Bank.

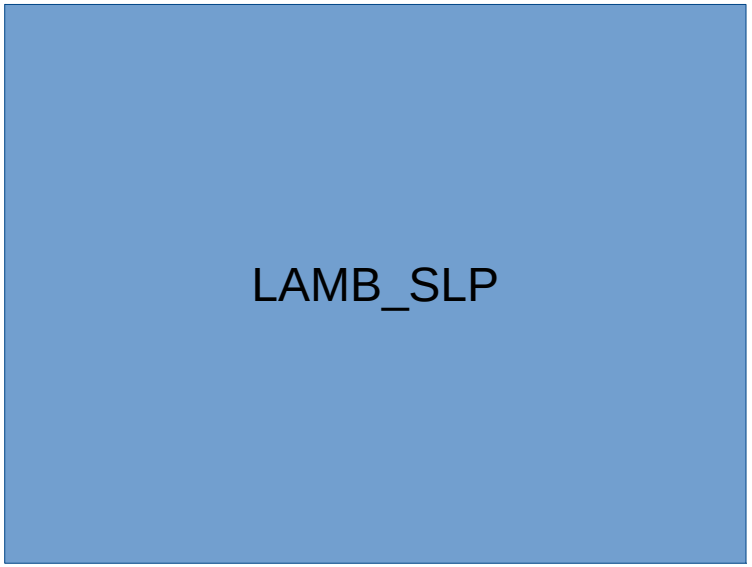
- Pattern matching: All the hits in each event are compared with all the patterns in the Bank and track candidates (ROADs) are found.

- Track Fitting: Fits of the full resolution silicon HITs contained in each ROAD determine particle tracks parameters.

Hardware to perform Pattern Matching



- VME 9U
- Serial Links @ 2 Gbs
- Clock @ 100 MHz

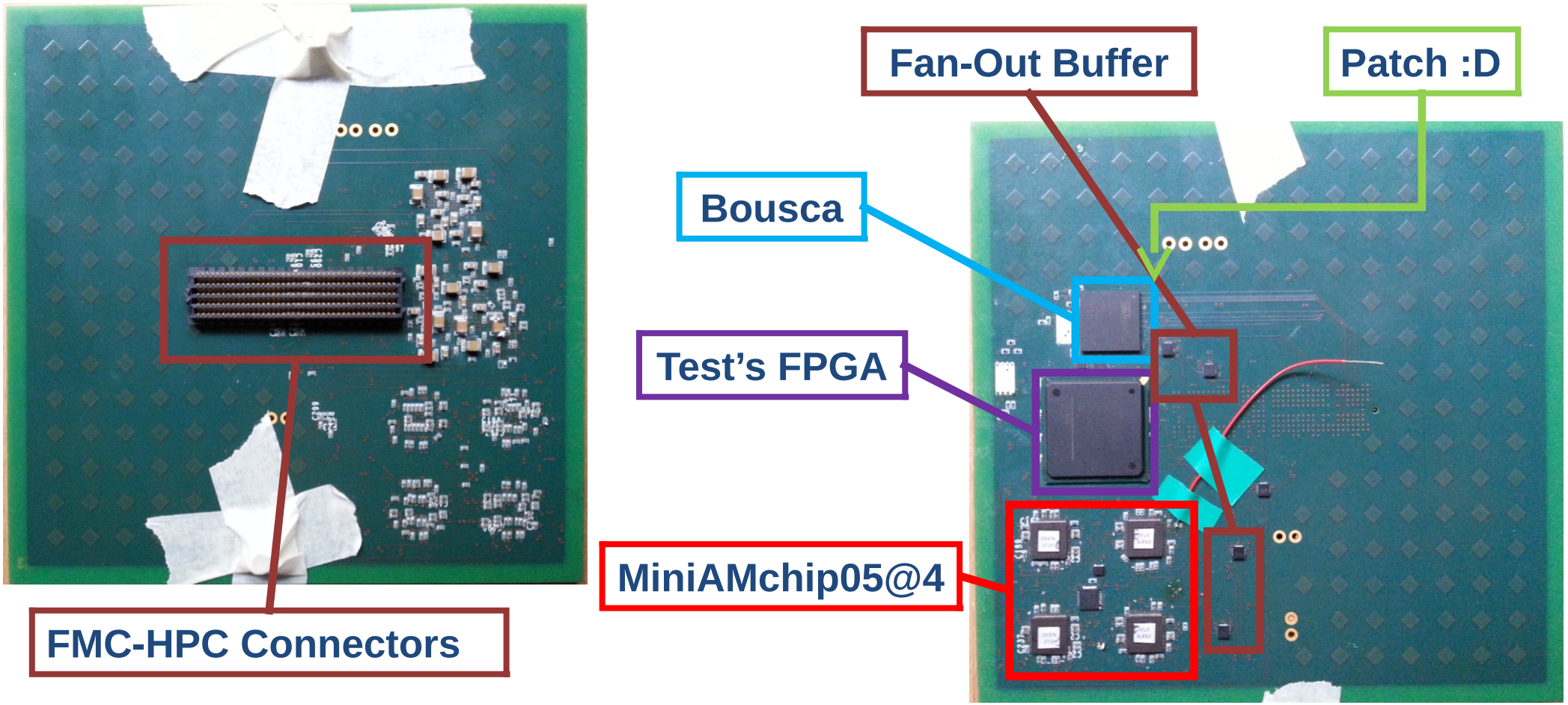


- Custom dimension
- Serial Links @ 2 Gbs
- Clock @ 100 Mhz
- 16 Associative Memory chips

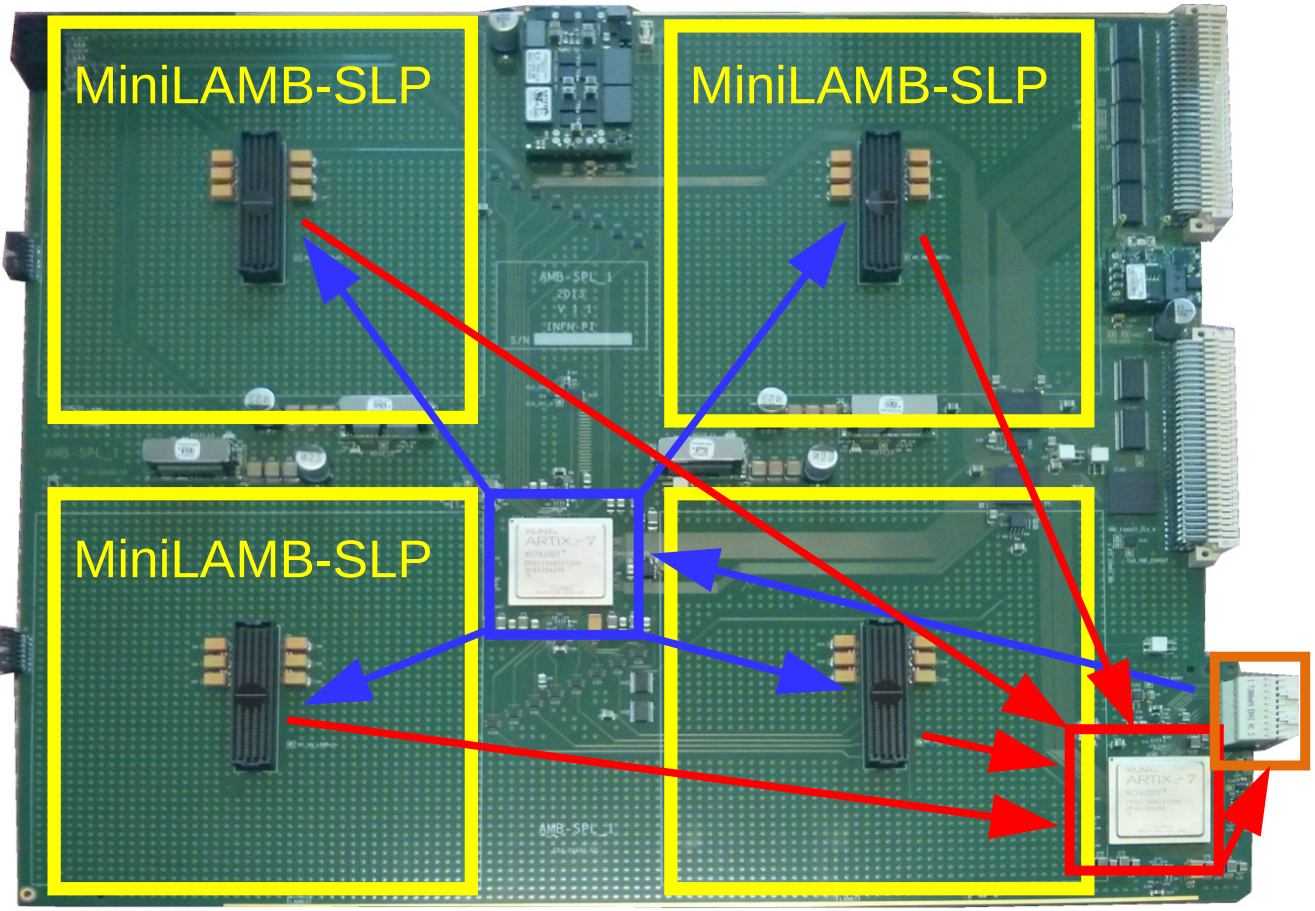
Status: we have a prototype reduced

MiniLAMB-SLP

- 16 AM chip are mounted on one MiniLAMB-SLP board.
- 4 MiniLAMB-SLP board are mounted on AMB-SLP board



Data flow in AM system



AMB-SLP Board

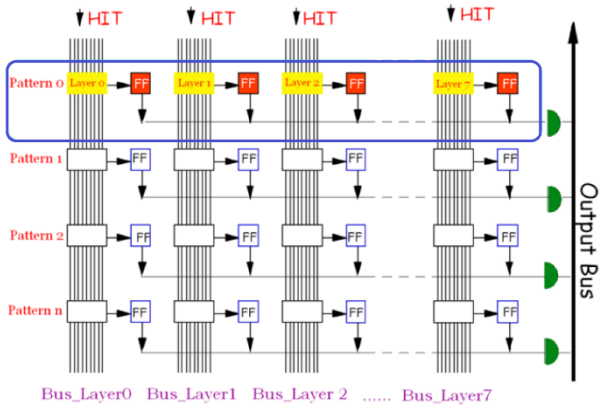
- The *FPGA* receive the *cluster's list* from P3 connector and distributes to 4 *MiniLAMB-SLP* boards.
- L'*FPGA* receive the *road* from *MiniLAMB-SLP board* and sends them to the rest of the system through the P3 connector.

Processing Unit

- In a Processing Unit we perform a Pattern Matching's algorithm.
- The AM chip is the key of this algorithm.

HITs

AM Chip



ROADs

- **More than one AM Chip** is controlled in parallel
- **Increase** the capability to store pattern

- Dedicated device: **Maximum** parallelism
- Each pattern with **private comparator**
- **No need synchronization** of different HITs layer

Match with **missing layer**

AMChip04:

- Package: PQ208
- Parallel I/O interface

It's necessary to increase the number of pads for future versions:

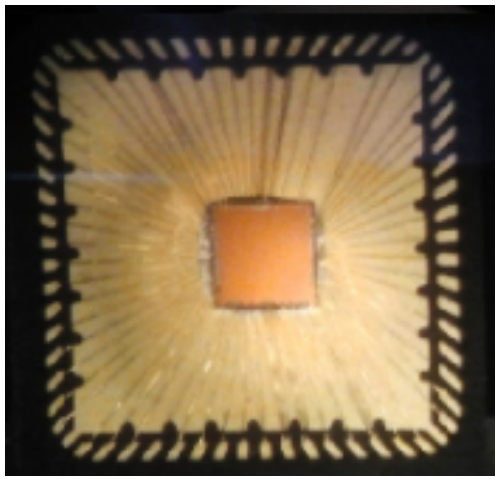
- To use a BGA package.
- It's necessary to simplify the routing of board.

Idea: **serial link** to transmit the data

Associative Memory Chip - Family 05

We have bought a *IP-CORE* to provide the *chip* of serialisers and deserialisers.

MiniAMChip05



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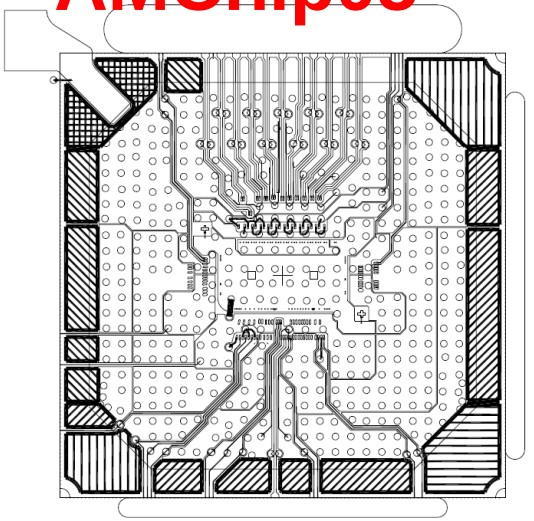
Die: 3.7 mm^2
Board: MiniLAMB-SLP
Status: under test

AMChip05



Package: BGA 23 x 23 mm
Die: 12 mm^2
Board: LAMB-SLP
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Recent developments of the Associative Memory chip

AM chip 04:

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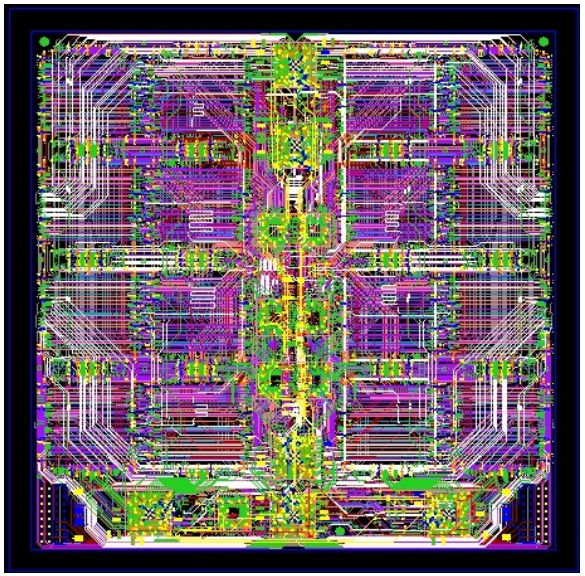
- 8k patterns
- Crazy routing of LAMB



- With the new AMChip06 we need more performance.
- It's necessary to increase the number of pads for future versions:
  - To use a BGA package for more pins.

But it's necessary to simplify the routing of board.

Idea: **serial link** to transmit the data