Proposal for a First Level Trigger based on Tracking

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Submitted Oct. 31 2008

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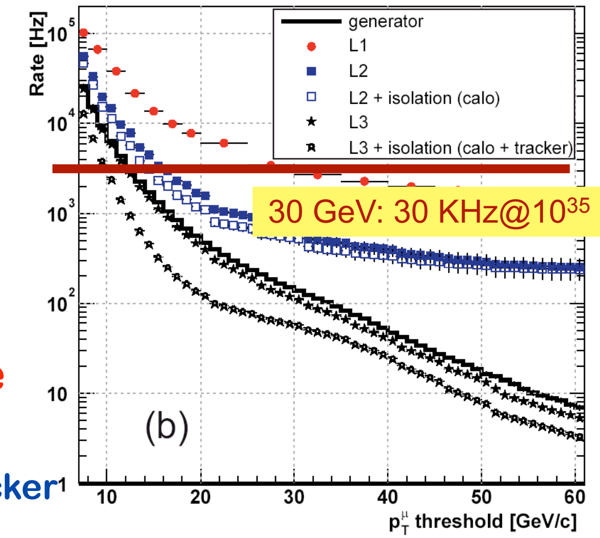
Main issues for Tracker L1 Trigger

- **What a L1 Tracker Trigger for?**
  - high p_T leptons (muons, electrons)
  - good jets-primary vertex matching (400 p.v./bx @20 MHz!)
- **Implies...**
  - high efficiency for tracks with relatively large (>~10 GeV) p_T
  - medium-good momentum resolution
  - good matching with calorimeters
- **The key issue for L1 Trigger using the Tracker is the huge data rate**
  - About 12k primary tracks per bunch crossing (50 ns) in the Tracker volume |η|<2.5 ...
    - ...plus any other coming from γ conversions and nuclear interactions
  - Must handle O(10) MHz cm^{-2} at radii larger than 50 cm in the Barrel✤
    - Aim to retain all hits from primary tracks above a given p_T and few others in order to no compromise the fake rate
    - Want to avoid difficult multi-layer correlation logic on-detector
      - ➨ Local data reduction deemed before going to trigger logic

From CMS-DAQ TDR



✤Huge uncertainties - extrapolation from LHC fluence

Tracking Trigger Proposals in CMS

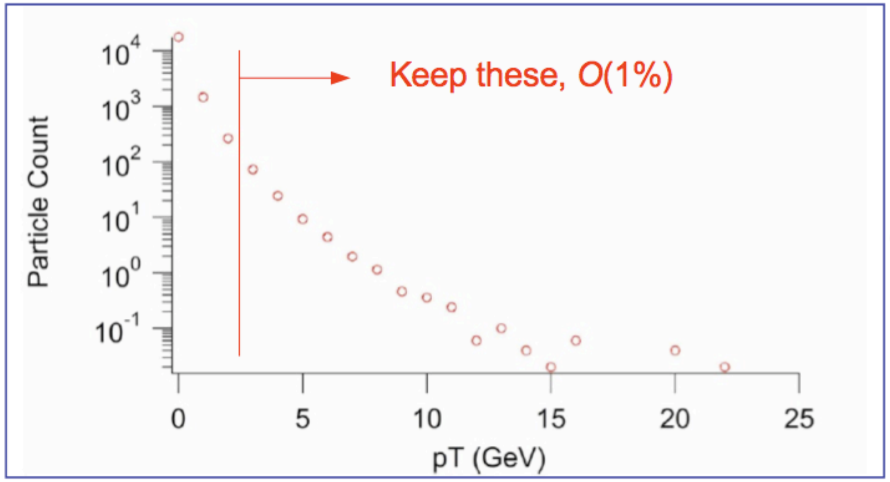
Two possible approaches

- Tracker primitives
  - Large data rate to handle different philosophies
    - ➨detector level data reduction using Cluster width(this talk)[1]
    - ➨detector level data selection using Stacked doublets (UK, see backup)[2] - already funded!
- Selective readout using Mu or Calo information
  - See A. Montanari talk[3]

1. F. Palla and G. Parrini, Tracking in the trigger: from the CDF experience to CMS upgrade, PoS(Vertex 2007)03
G. Barbagli, F. Palla and G. Parrini, Track Momentum Discrimination Using Cluster Width in Silicon Strip Sensors for SLHC, TWEPP-07, Prague 2007 http://indico.cern.ch/contributionDisplay.pycontribId=80&sessionId=29&confId=11994
2. J. Jones, G. Hall, C. Foudas, and A. Rose, “A pixel detector for level-1 triggering at SLHC,” arXiv:physics/0510228.
3. A. Montanari et al. CMS-IN 2007-058

Tracking Trigger driving idea

- Select only tracks above a given p_T since they are very few

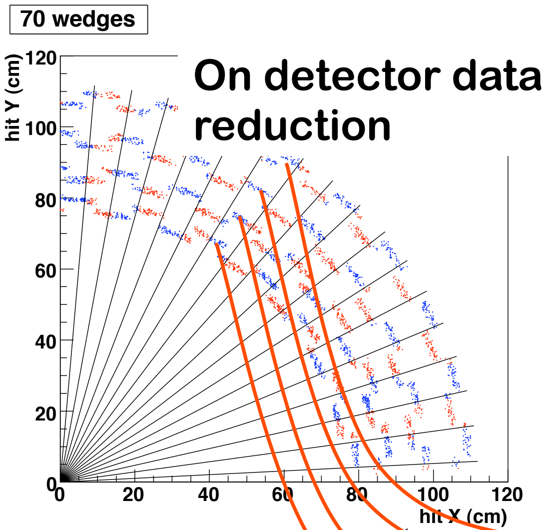


- Design considerations:
  - Reduce to a minimum Tracker trigger-only layers
    - i.e. same layers for triggers and data
  - Limit as much as possible the needed bandwidth and number of channels for trigger
  - Keep the system as much flexible as possible to adapt to any SLHC conditions

Trigger working model

- Subdivide barrel layers into many - O(50 to 100) - φ sectors
  - Keep data volume limited in each sector
  - Match with the detector sizes. High p_T tracks well inside (already a momentum discrimination!)
- Data reduction and transfer (outer layers R>50 cm)
  - Use silicon strip detectors
    - no time stamp in synchronous readout
  - Reduce the data rate for Trigger purpose on detector
    - local data reduction using Cluster Width
  - Use very high speed data links O(10 Gbps) to limit the no. of links
- Process the data off detector
  - Extend and rescale to CMS the CDF approach using Associative Memories (AM)
    - majority of at least 3 layers out of 4 in each trigger sector
    - “compute” p_T
    - match with muons and calorimeters
- Output of the Trigger
  - Tracks reconstructed above a given pT in each sector

Off-detector Trigger Logic



On detector data reduction

Each AM searches in a small $\Delta\varphi$
and produces a set of tracks above a given p_T

OFF DETECTOR

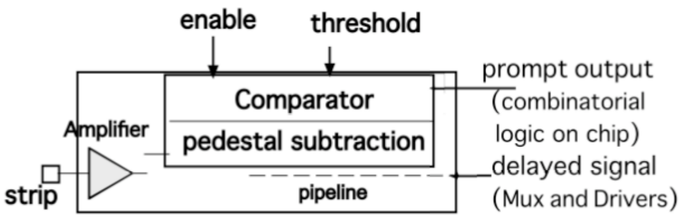
1 AM for each enough-small $\Delta\phi$
Patterns
Hits: position+time stamp
All patterns inside a single chip
N chips for N overlapping events
(identified by the time stamp)

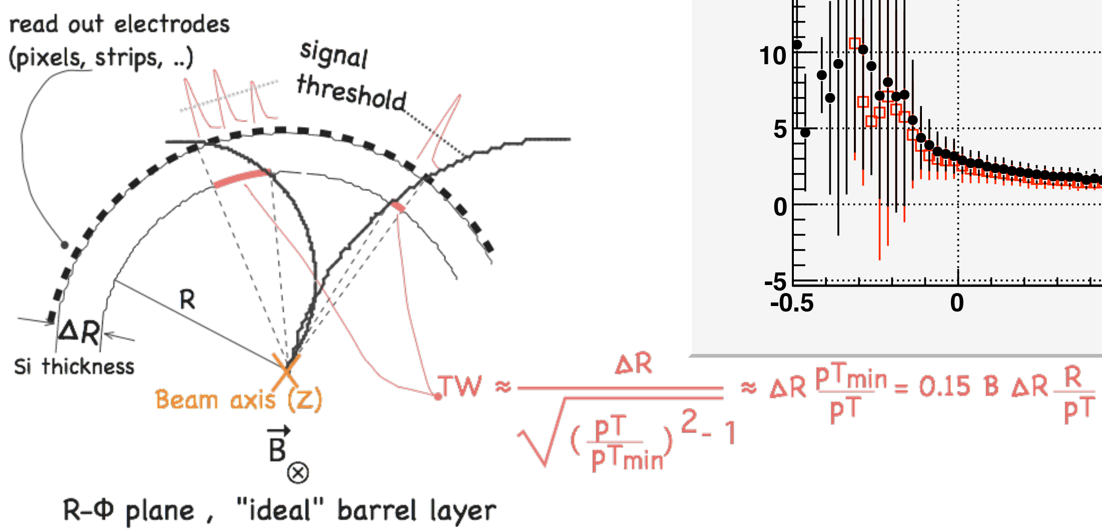
Fast
data links

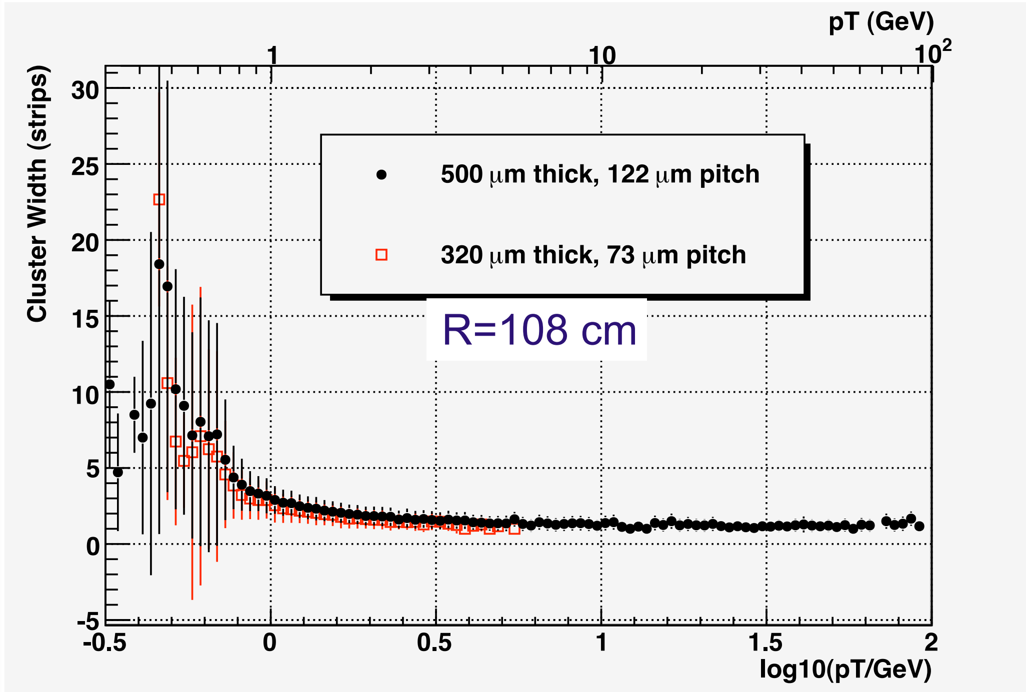
Event1 AMchip1	Event2 AMchip2	Event3 AMchip3	• • • • •	EventN AMchipN

Data rate reduction on sensor

- Select clusters from high p_T particles using the different cluster width (CW) pattern
- Need a clusterizer ASIC after the FE stage.





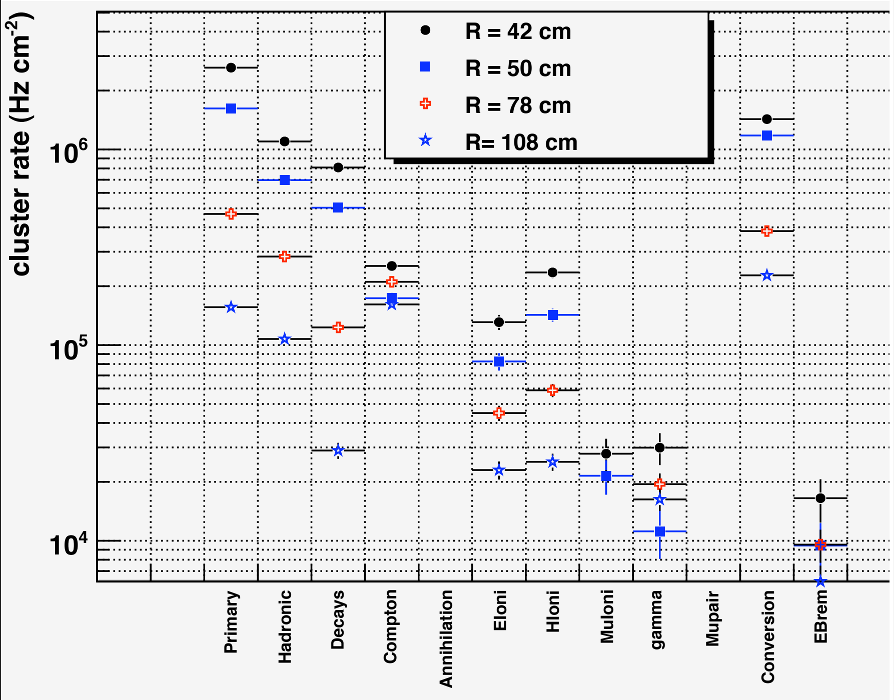


Note scaling applies

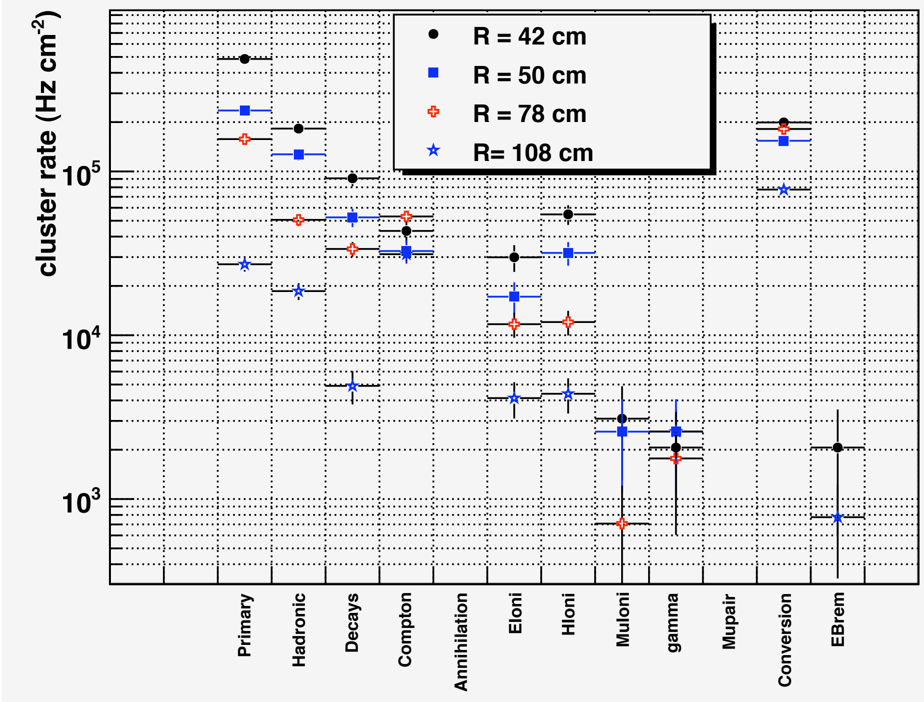
Data rate in Barrel

- **Large reduction in data rate expected:**
  - R=78 cm: 500 kHz cm^{-2} (it was 6 MHz cm^{-2} hit rate)
  - R=108 cm : 170 kHz cm^{-2} (it was 3.6 MHz cm^{-2} hit rate)

Cluster rate **before** CW reduction

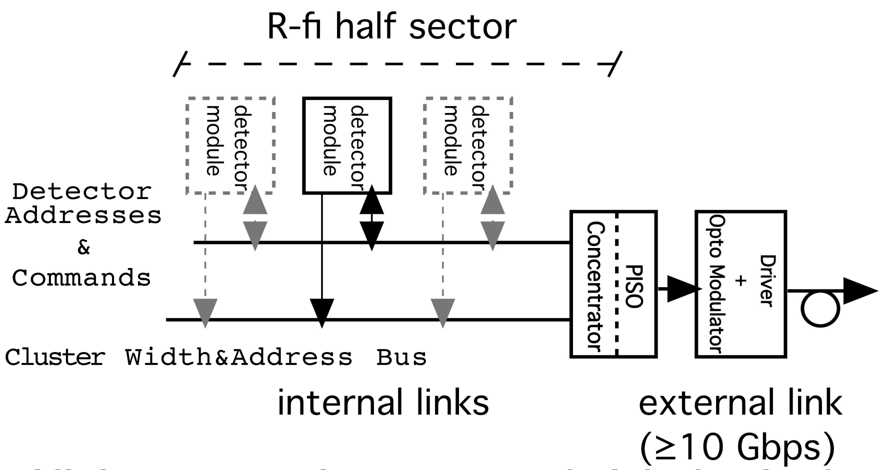


Cluster rate **after** CW reduction



Routing signals off the Tracker

- Even if CW computed with full granularity, for trigger needs a reduced granularity is acceptable
  - (12 bits for full granularity; 375 µm "effective" pitch≡10 bits)
    - A module (~9x4 cm^2) is expected to route on average~≤ 220 (70) Mbps at 78 cm (108) radius at full granularity
    - Study several connection schemes between each module and the high-speed links "hubs" located at the end of each sector

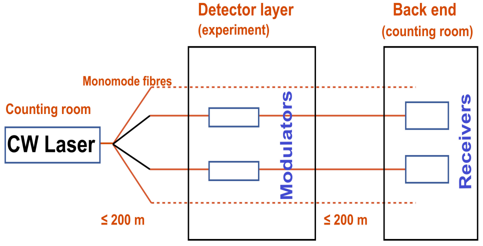


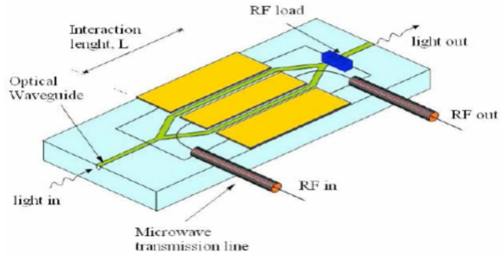
- Internal links can use low power µ-twisted pairs (see B. Meyer talk at TWEPP 2008)
  - ➡ <u>These kind of links also useful for Phase 1</u>

Fast Links

Telecommunication/IT standards

Put Laser power outside the detector and use modulators



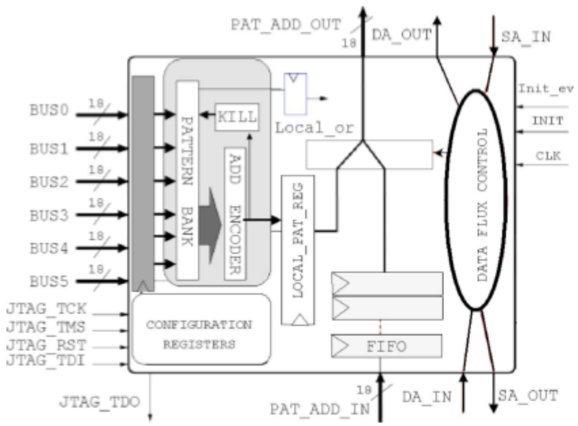


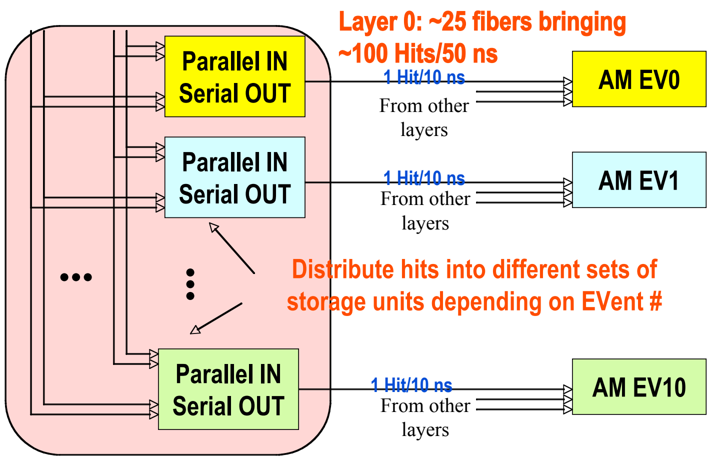
- Normally uses electro-optical modulators (reaching up to 40 Gbps)
- Need to be tested in high fluence, low temperature and high B field

	Size (mm^3)	Power (mW)	Driving Voltage (V)	Working Temp. (°C)	Magn. Fields Comp.	Availability
$LiNbO_3$ MZM	≤ 125 x15x10	250 (modulator only)	≈ 5	0 to 70	Good	YES
InP MZM	~ 60 x13 x 8 (laser included)	250 (modulator only)	≈ 5	0 to 70	Poor	YES
Si MZM	50 x 15 x 8 (estimate)	===	≈ 1	===	Good?	NO
EAM	~ 50 x30x10	≈ 1000 (TEC)	≈ 2.5	-20 to 70 (case)	Good?	YES

Data switch

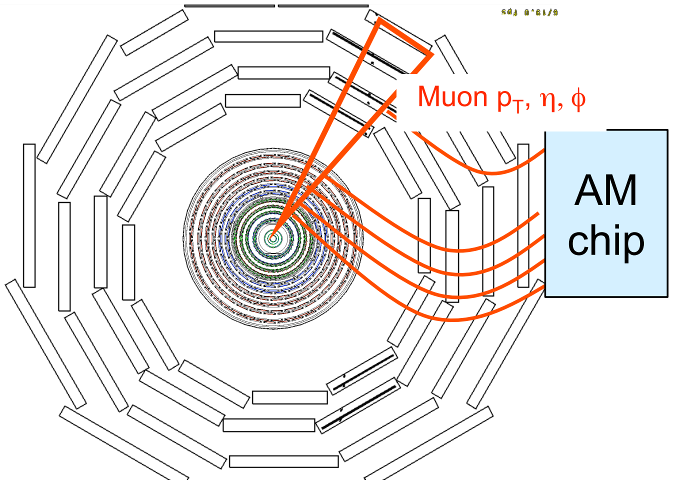
- Each AM chip will receive inputs from different layers in the same trigger sector
  - depending on the I/O speed and processing time a single AM chip cannot sustain the bandwidth of a single sector
    - Forecast ~3.6 Gbps (200 MHz x 18 bit) AM/input to be compared with ~10 Gbps of the busiest sector
  - Need a “traffic control” switch to distribute the data into different parallel AM engines

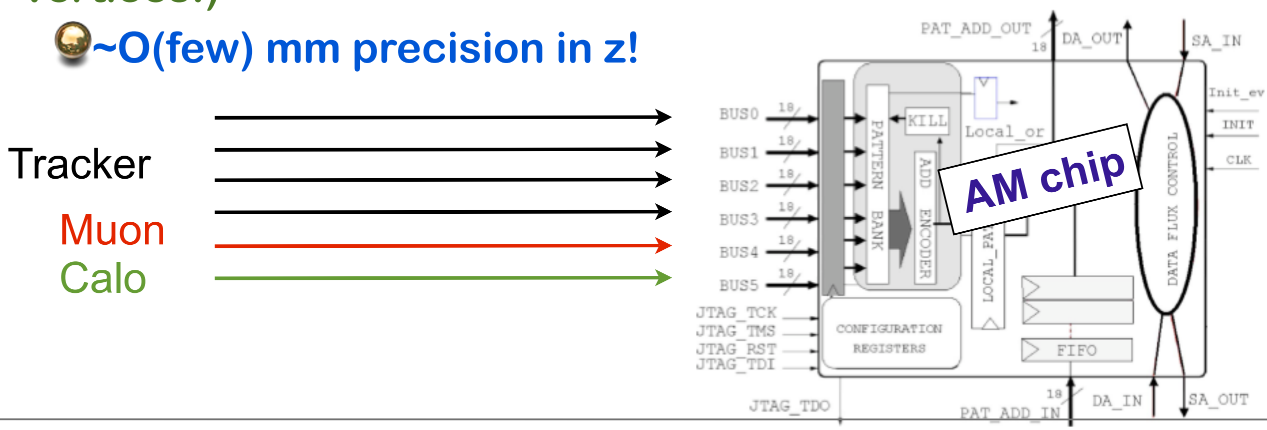




Building e/μ / γ / τ objects with AM

- **Correlation using AM chips is naturally embedded**
  - Input the AM with
    - L1 Muon primitives
      - ➨ Muon: play with isolation cuts
    - L1 Calorimeter primitives
      - ➨ Electron
      - ➨ Jets
      - Veto of high momentum tracks: Photon
      - Single or triple track match: Tau
    - Primary vertex correlation (remember 400 primary vertices!)
      - ~O(few) mm precision in z!





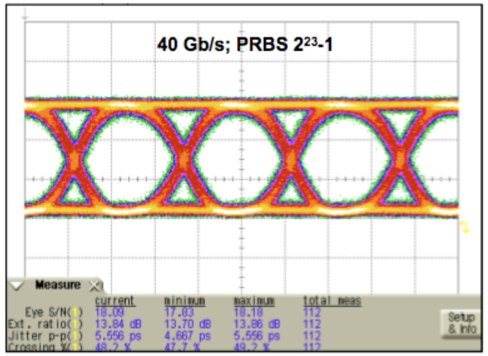
What this proposal will study - I

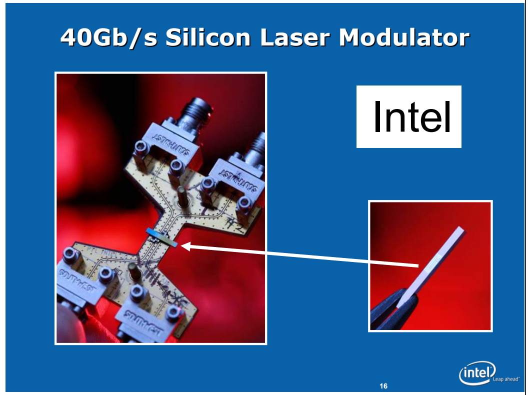
- On-detector data reduction using Cluster Width
  - Strip sensor design and locations (see later) (INFN + others)
  - Data formatting and estimate of the detector bandwidth (INFN + others)
  - Clusterization ASIC dimensioning
    - a first FPGA prototype foreseen on the first year (INFN + Lyon), followed by conceptual ASIC, first in 0.35 um techology; possibly followed in lower pitch submicron technology (Lyon)
  - Validation of the method by using real p-p LHC collision data as well as a dedicated test beam (INFN + others)
- <u>INFN will be leading the studies</u>
  - Already actively working on system design and validation
    - Pisa and Florence
  - Expect to contribute to the FPGA for studying the clusterization logic
    - Florence

What this proposal will study - II

- **Data shipment off-detector using high speed links (INFN + others)**
  - Procurement of MZM and drivers
  - First choice will be $LiNbO_3$ modulators from several vendors (Avanex, JDSU or Photline)
    - If Si-based modulators will be available (Intel) they will also be procured
  - Irradiation at several facilities followed by qualification
    - Univ. Massachusetts Lowell facility (proton, neutron)
    - Labec Florence (proton)
  - High magnetic field and low temperature qualification
  - Want to study modifications with Companies, possibly also to be performed at ICFO Labs.
- **Some funds (2009 only) already granted by CSN5 to Florence within the DACEL II in 2008**
- **<u>CNR Florence and ICFO Barcelona have expertise to test and qualify MZM</u>**

AVANEX

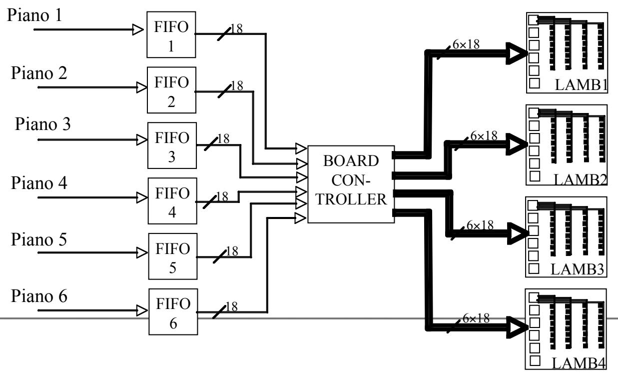




What this proposal will study - III

- **Organization and dimensioning of the Trigger logic**
  - **Dimensioning of the number of patterns and AM chips (INFN + others)**
    - depends upon the (coarse) pitch segmentation, the number of layers and detectors in a sector, the minimum pT threshold and the number of sectors
  - **Dimensioning of the Switch (INFN + others)**
    - Will depend upon the effective speed of AM chips
    - Need to follow the development of the new chips by FTK collaboration (outside CMS)
  - **Want to develop a prototype switch and study the best architecture to distribute clusters to the AM chips (Boston)**
    - based on FPGA and high-speed LVDS links
    - Profit of recent developments from SLIM5 collaboration, as well as of past experience in D0 (Boston, Brown)

http://www.pi.infn.it/slim5/



Sensors and Layers

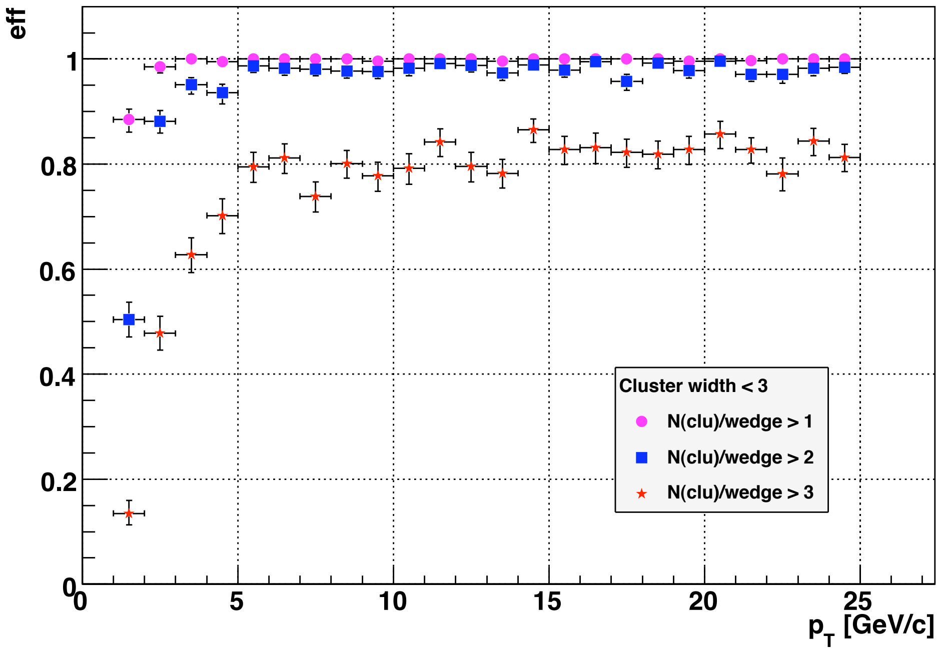
- Use silicon strip detectors
  - Want to study the effects of several parameters:
    - pitch and thickness
    - material substrate (p or n bulk will influence the Lorentz angle)
    - strip length
    - Electronics front end coupling (AC vs DC), noise and cross talk
    - Optimize radial distance
- Preliminary studies done with a modified Strawman A*:
  - Detection layers located at radii: 78, 87, 97, 108 cm (current last 4 TOB)
  - 290 µm active thickness, 91.5 µm pitch (97 and 108 cm layers) and 122 µm pitch (78 and 87 cm layers), n-type bulk, 4.65 cm strips length, AC coupling, 3% inter-strip couplings
    - no Lorentz angle compensation
    - 12192 mini-modules, 7.96 M channels

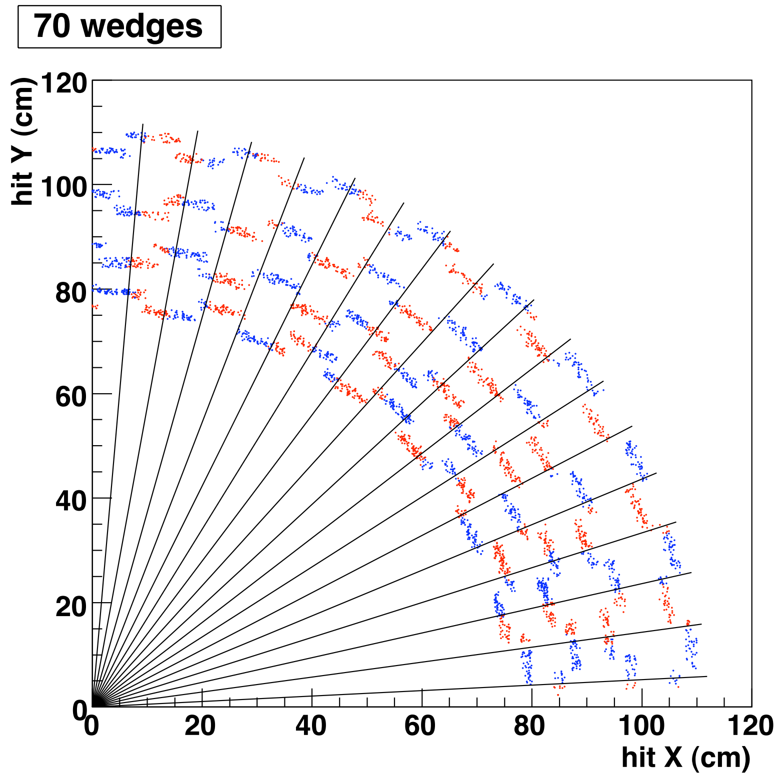
*Some dimensions constrained by the Strawman A approach

- Tracking Trigger offers INFN a leading oppurtunity
  - To consolidate expertise on Simulation (see A. Tricomi talk) and Sensors (see A. Messineo)
  - To increase expertise on analogue and digital electronics

Some (very) preliminary results

Fraction of muons with minimum number of clusters in any of the 70 trigger sectors





- APV at the borders are shared between sectors
- Majority of 3 layers per sector give ~100% efficiency above p_T~5 GeV/c

Job sharing

Institute\Item	Cluster width Simulation & Validation	AM chip, off-detector trigger processors and switch	Links	Electronics
Lyon IN2P3	X	X		X
Bari INFN	X			X
Florence INFN/CNR	X		X	X
Pisa INFN	X	X		
Barcelona ICFO			X	
Boston University		X		
University of Minnesota			X	
Brown University	X	X	X	

Work plan to be accomplished in 3 years
(see full table in the backup slides)

Financial plan for INFN

Item	Cost (k€)
Modulators + drivers	40
FPGA + electronics	20
Equipments for test beams	30
Mechanics	20
Consumables	40
Total (3 years)	150

BACKUP

UK Project funding approved

UK Upgrade Project "WP1"

"Tracker and Level-1 Track Trigger:
Design and Optimisation"

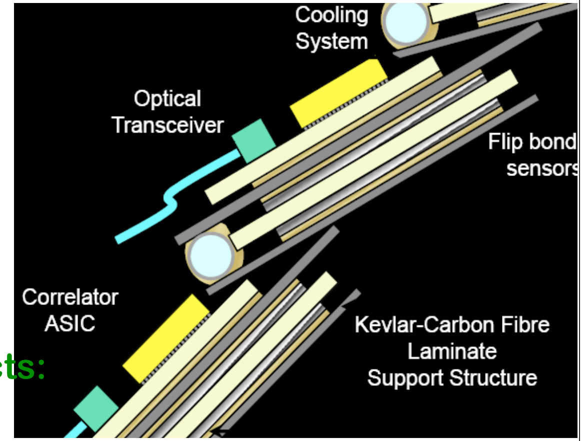
- Areas of work
  - Tracker layout studies and optimisation
  - Track trigger primitives generation and optimisation
  - L1 trigger upgrade – tracking algorithms
  - L1 trigger upgrade – requirements and physics performance
- Project scope and schedule
  - Project duration 2.5 years: 1/1/09 until 30/6/11
  - STFC authorises us to deploy ~14SY of effort over this period (plus students)
    - Of which ~10SY is new effort; can aim to make a step change in rate of progress in some areas
- Organisation
  - Four 'sub packages' coordinated by experienced collaborators
  - Recruitment of new postdocs to start immediately (candidates?)

Timeline

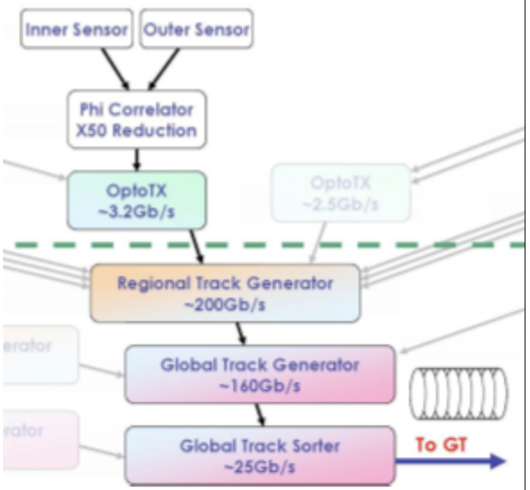
Item\Year	Year 1	Year 2	Year 3
Cluster width Simulation & Validation	LHC collision data analysis. Tracker layout geometry and basic characteristics of CW algorithms. Sensor and strip dimensions versus radius. Determination of the data rate and data reduction efficiency.	Trigger performances on benchmark processes. Experimental set up to verify the CW method and to study charge sharing effects.	Trigger performances on benchmark processes. Test beam measurements and analyses
AM chip and off-detector trigger processors and switch	Dimensioning of the patterns per AM chip. Evaluate existing R&D projects, testing existing hardware if appropriate. Test board design to test timing performance. Preliminary system design, including tentative choice of bus and communications standards with system.	Trigger efficiencies and trigger sectors dimensioning. Design and fabricate prototype PCBs to demonstrate key features of system design. Design firmware for system operation.	Dimensioning of the system using existing solutions for AM chips. Fabricate updated prototypes if required. Evaluate operation of system using prototype detector in available test benches.
Links	Commercial opto-link devices survey and the GBT project adaptability. Plan of the experimental tests on external MZM devices and drivers.	Tests on MZM and drivers. Summary: project of a custom device.	Validation of the custom device. Proposal of link system.
Electronics	On detector electronics: architecture requirements and survey of existing solutions and projects. First detector prototype assembly. Telescope procurement. Clustering FPGA and ASIC conceptual design.	Test beam and result analysis. Tests on prototype board (FPGA) of discrimination algorithm. ASIC first submission Electronics and detector prototype survey. New detector prototypes assembly	Solutions for silicon data connection to optical links. ASIC second submission Test beam and result analysis.

Alternative Stacked layers (UK)

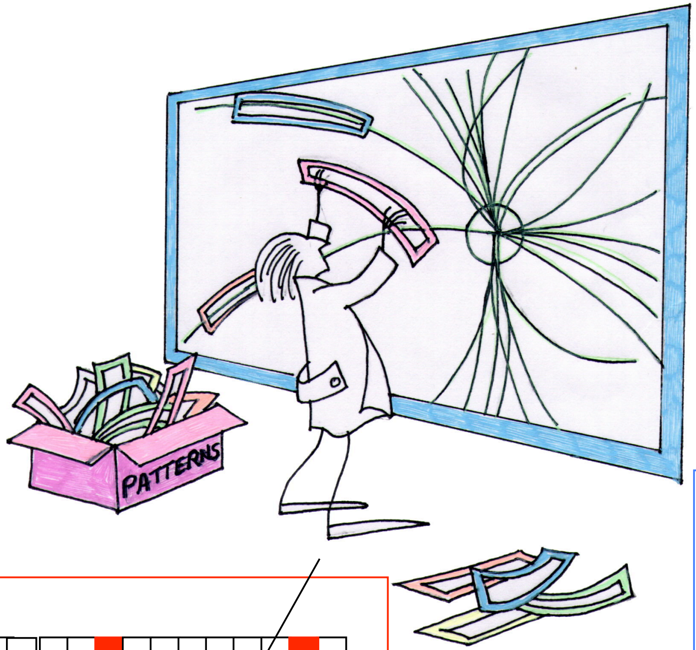
- **Sensor and module**
  - sensor pitch (60-120µm in r-ϕ and ~1 mm z)
  - Tight mechanical structure
- **Data reduction logic on detector:**
  - Correlator ASIC between two sensors in the stack
    - run on full resolution r-ϕ and z correlations
    - need to compensate for Lorentz angle and misalignment effects: need calibration constants to be uploaded



- **Off detector:**
  - Regional Track Generator - FPGA based
    - projects track stubs from outer to inner super-layers in several η regions.
  - Global Track Generator
    - builds up tracks and computes pT
    - applies a further cut in pT
  - Global Track Sorter
    - holds tracks and forward them to the Global Trigger

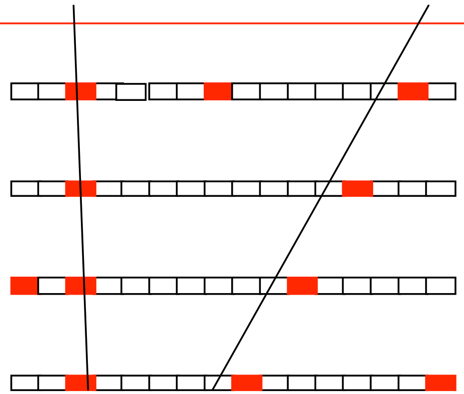


Pattern matching in CDF (M. Dell'Orso, L. Ristori – 1985)

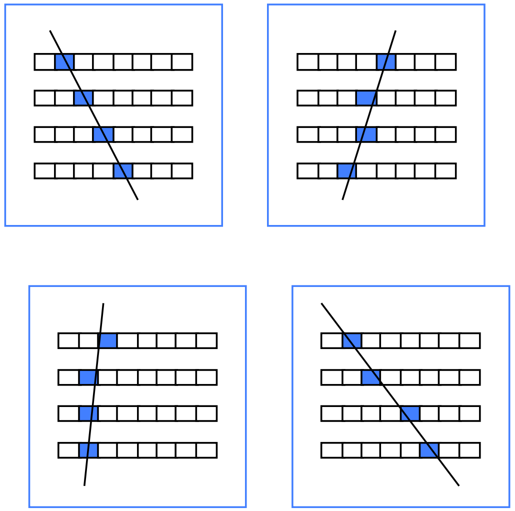


The pattern bank is flexible set of pre-calculated patterns:

- can account for misalignment
- changing detector conditions
- beam movement
- …



The Event



The Pattern Bank

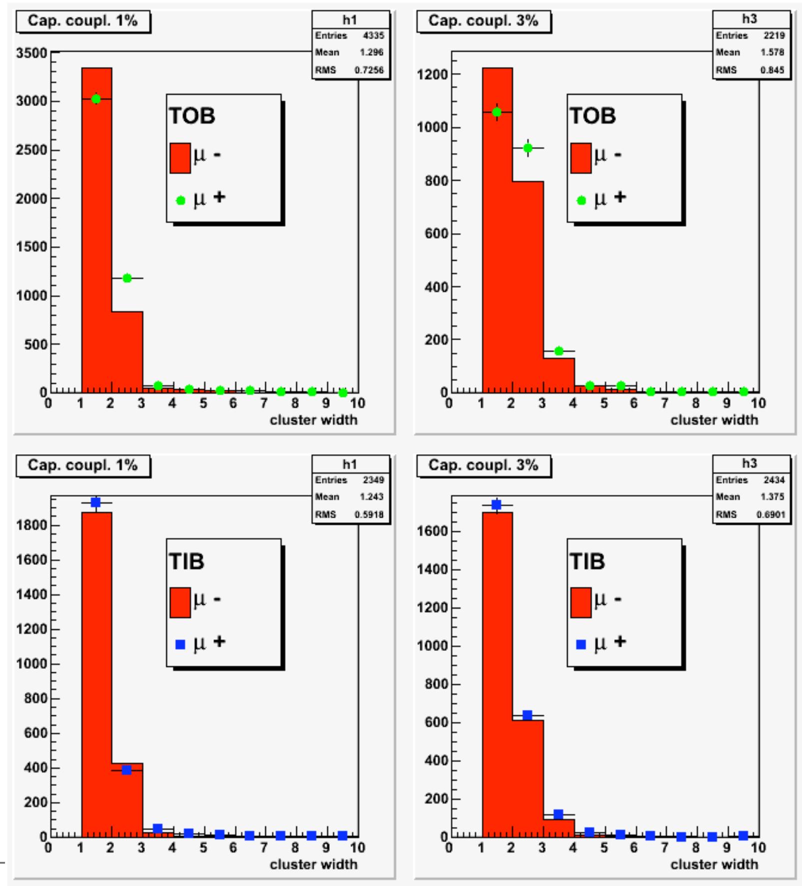
• • •

Cap. couplings and Lorentz angle

Cluster width for muons above 10 GeV/c

- clear effect due to capacitive couplings and Lorentz angle
- Note the TIB is compensated

1% CC



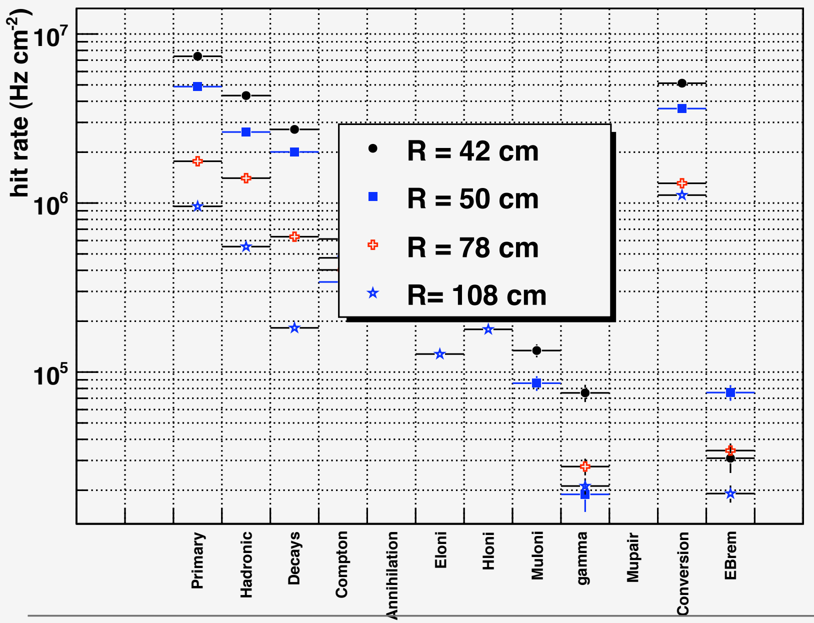
3 % CC

Data rate in Barrel - I

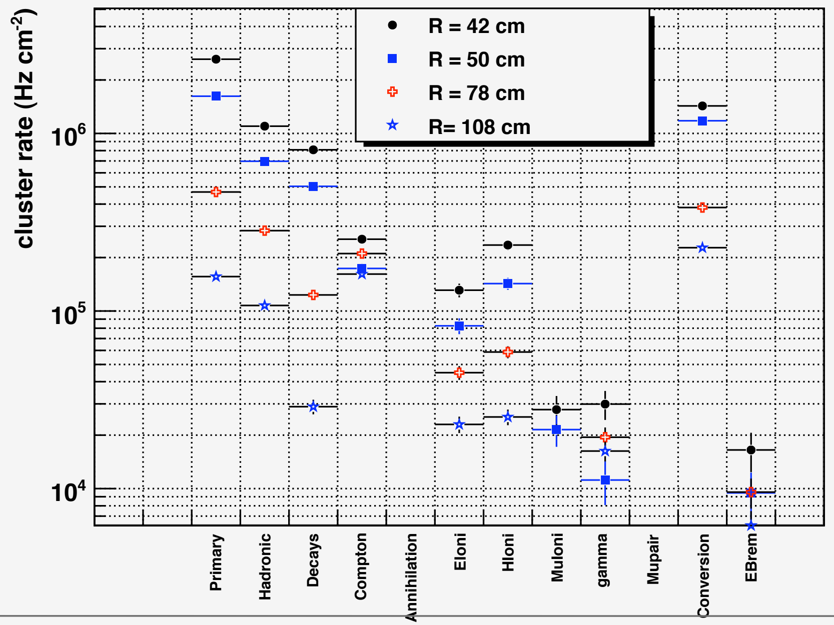
- **Huge data rate (at 10^{35} cm^{-2} s^{-1})**
  - **Use clusters instead of hits to first decrease the rate**
    - **R=42 cm: clusters (hits) ~7 (22) MHz cm^{-2}**
    - **R=78 cm: clusters (hits) ~1.6 (6) MHz cm^{-2}**
    - **R=108 cm: clusters (hits) ~0.7 (3.6) MHz cm^{-2}**

    (Note: if no zero-suppression applied (DIGI) rates are a factor 10 larger)

HITS

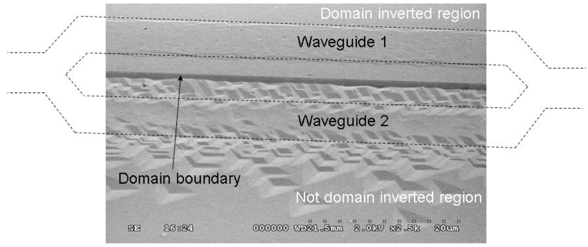


CLUSTERS

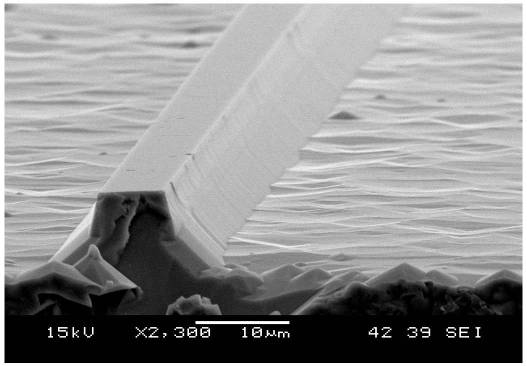


ICFO Optoelectronics group

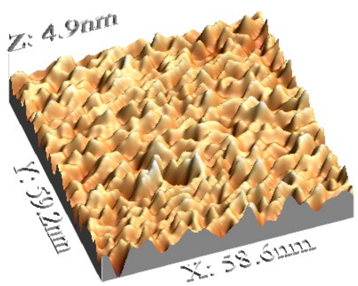
15 Members:
1 Group leader, 4 post-docs, 6 PhD students, 4 Research engineers

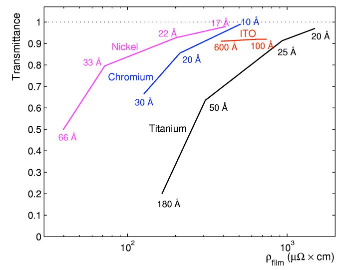


Research topics:
- Micro- and nano-engineered electro-optics (EO) and acousto-optics devices
- Ultra-thin metal films for transparent electrodes
-Photonic crystal fibers (PCF) and nanowire devices



Ongoing projects:
-Ultra low voltage and broad band integrated EO modulator (Ministry of Research)
-Quantum transceiver (European Space Agency)
-High temperature PCF sensor (European Space Agency)
-Head up display for car safety (Ficosa, Seat, AD Telecom)
-3D liquid crystal cell for display (AD Telecom)





Examples of fabrication of low voltage
Modulators and ultra thin metal films
Done at ICFO

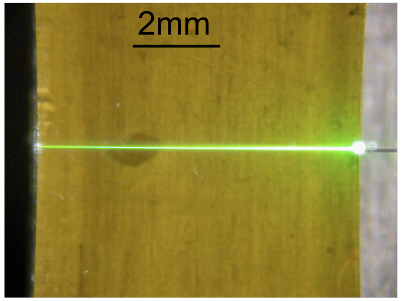
Materials and Devices for Photonics - MDF Group

Activities on glass planar waveguides, fibres and microcavities for telecom and sensing

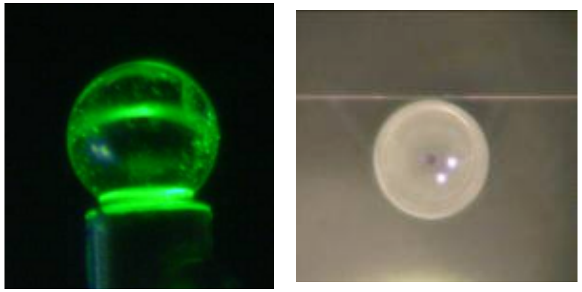
People

- 5 researchers
- 1 post doc
- 1 PhD student
- 1 graduate student
- 2 technicians

contact: s.pelli@ifac.cnr.it



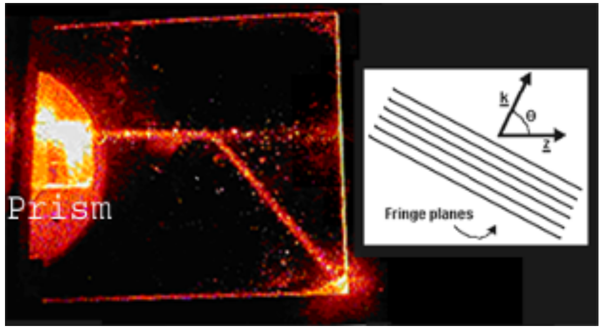
Channel waveguide in Er^{3+}-doped glass



High Q microcavities

Main research topics

- Rare earth doped oxide glasses and glass ceramics, **photorefractive** film and polymers.
- Planar **waveguides** by ion-exchange, UV imprinting, ion implantation; waveguide and fibre **gratings**; waveguide **lasers** and **amplifiers**.
- **High Q** Whispering Gallery Modes (WGMs) **microcavities**.



Waveguide gratings

Fabrication facilities

- **Class 100** (and class 1000) **clean room** with Mask Aligners, RF Sputtering, Reactive Ion Etching, Spinner, Profilometer.

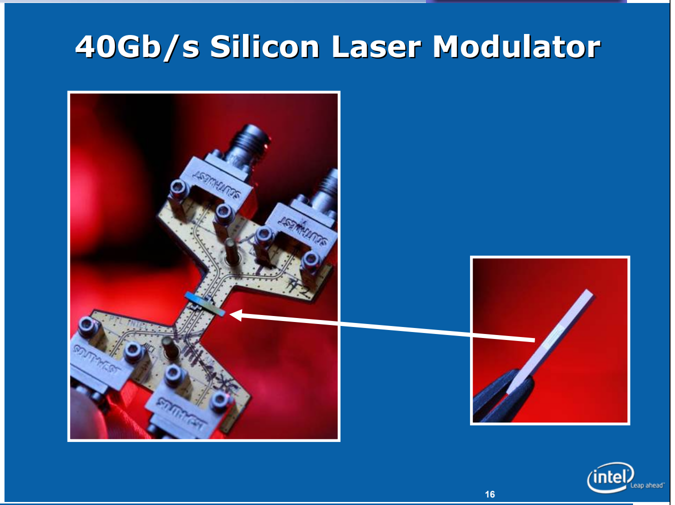
Characterization labs

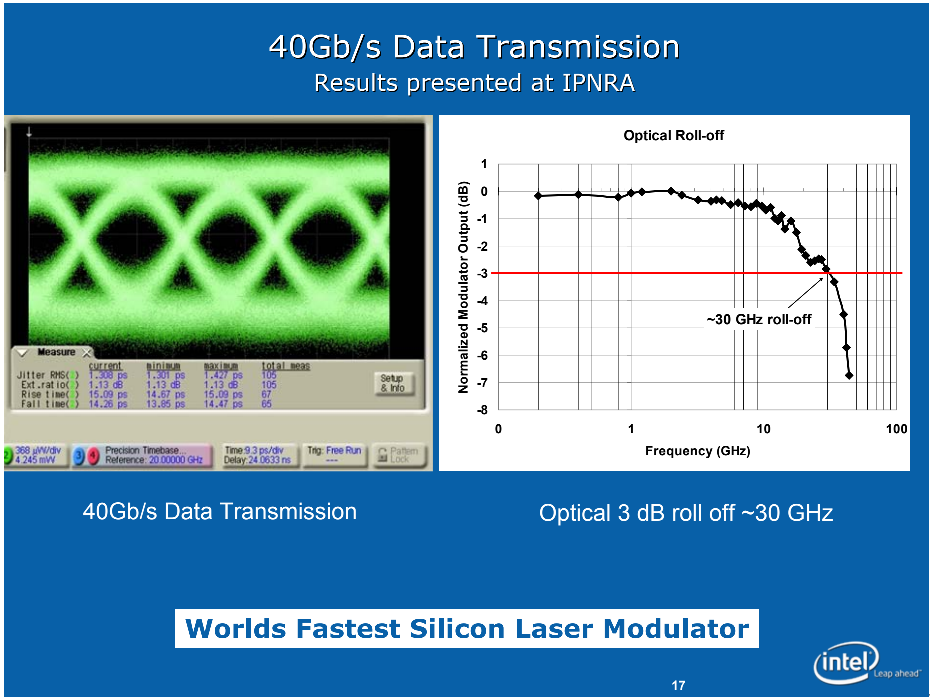
- Laser sources including Ar, Ti:Sapphire, Nd-YAG, KrF excimer; semiconductor tunable lasers in S & C band and pump lasers for optical amplification.
- Commercial and in-house developed **test equipment for waveguides and fibres characterization**, **microcavities** analysis, materials spectroscopy.

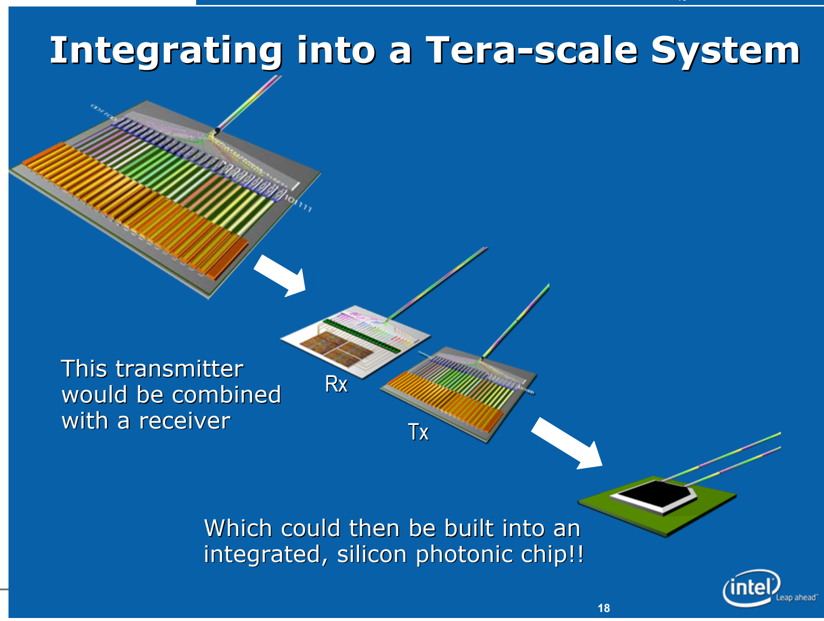
Class 100 clean room

Silicon based modulators

- **Extremely attractive**
  - reduced power consumption and dimensions
  - possibility to embed in the readout chip
  - available in ~5 years ?







A proposed silicon module layout

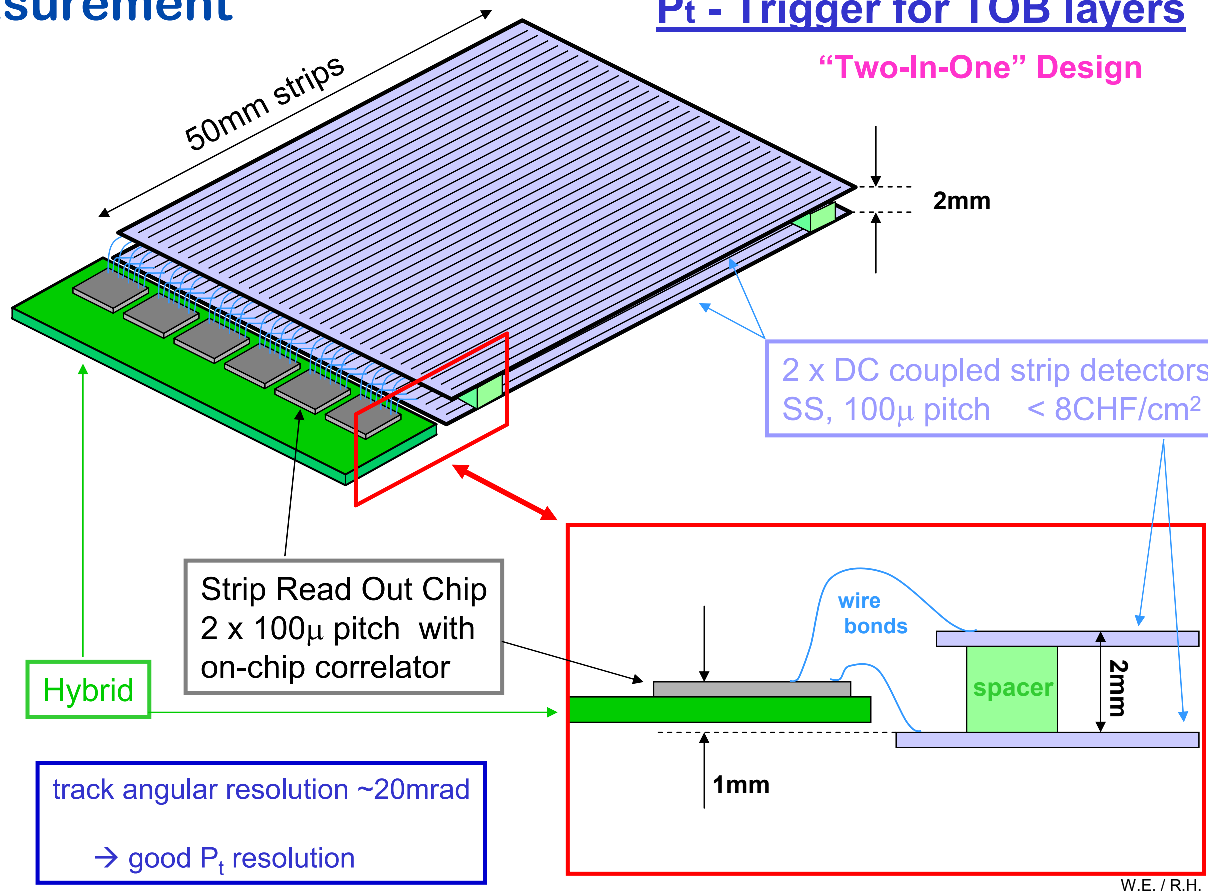
Two step approach

1. Cluster width local reduction
2. Track stub measurement

W. Erdmann
R. Horisberger

Pt - Trigger for TOB layers

"Two-In-One" Design



track angular resolution ~20mrad

→ good P_t resolution

Associative memories evolution

- Long history
  - 1990: Full custom VLSI chip - 0.7 μm (INFN-Pisa), 128 patterns/chip: high pattern density, not easy design
  - FPGA approach 1998: easier design but fewer density
  - A good compromise is the standard cell approach currently used for the SVT CDF upgrade: J. Adelman et al., Nuclear Science Symposium, 2005 IEEE, vol. 1, 2005, p. 603.
    - 0.18μm (INFN-Pisa), 5000 patterns/chip, 6 buses input lines, 50 MHz/bus, 18 bits/bus
      - produced by UMC (Taiwan) - design time ~8 months + 2 months production
- Forecast for 2013:
  - 90 or 65 nm technology would allow higher density pattern
  - Factor 4 higher clock speeds achievable
  - All in all: allow to reach ~30K patterns/chip with 200 MHz/bus speed

Who is proposing FTK & schedule

FTK

University of Chicago

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Istituto Nazionale Fisica Nucleare Roma 1

M. Rescigno

- R&D Proposal to work on TDR: presented in July. Approved Feb 2008
- 1 year to produce the TDR (2008)
- 3 years to build the system (2009-2011)
- first data taking with baseline LHC (~ when lumi 10E34 $cm^{-2}s^{-1}$)
- upgrade for SLHC with possible extension @ level 1

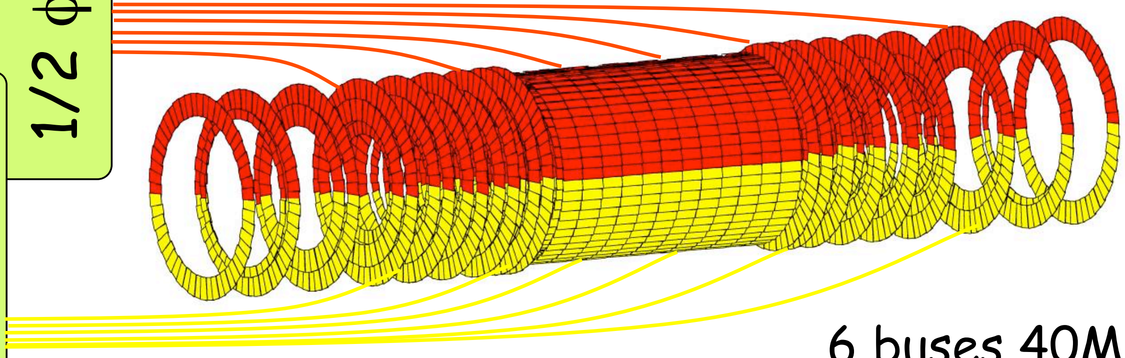
Feeding FTK @ 50KHz event rate

FTK

1/2 φ AM

1/2 φ AM

ATLAS Pixels + SCT



Divide into φ sectors

Allow a small overlap for full efficiency

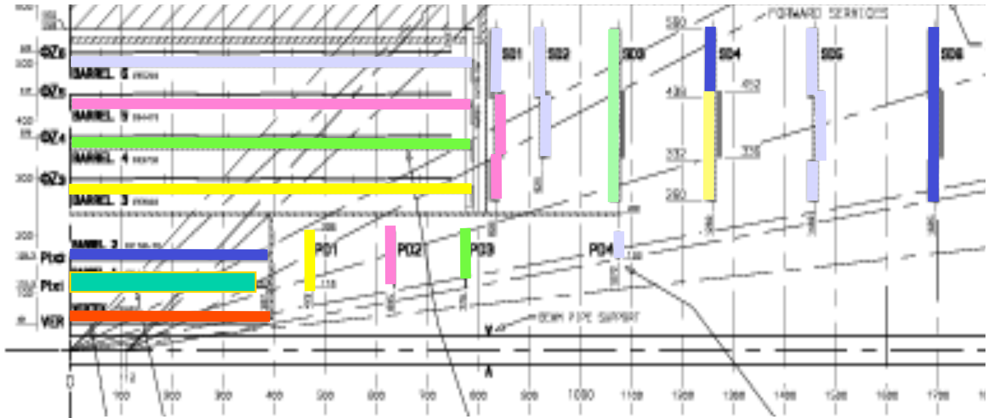
6 buses 40MHz/bus

7+4 Logical Layers:
full η coverage

~350MHz cluster/layer
(10E34 $cm^{-2}s^{-1}$ lum, 50kHz ev.)

ATLAS-TDR-11

10 φ sectors



Pixel barrel SCT barrel Pixel disks