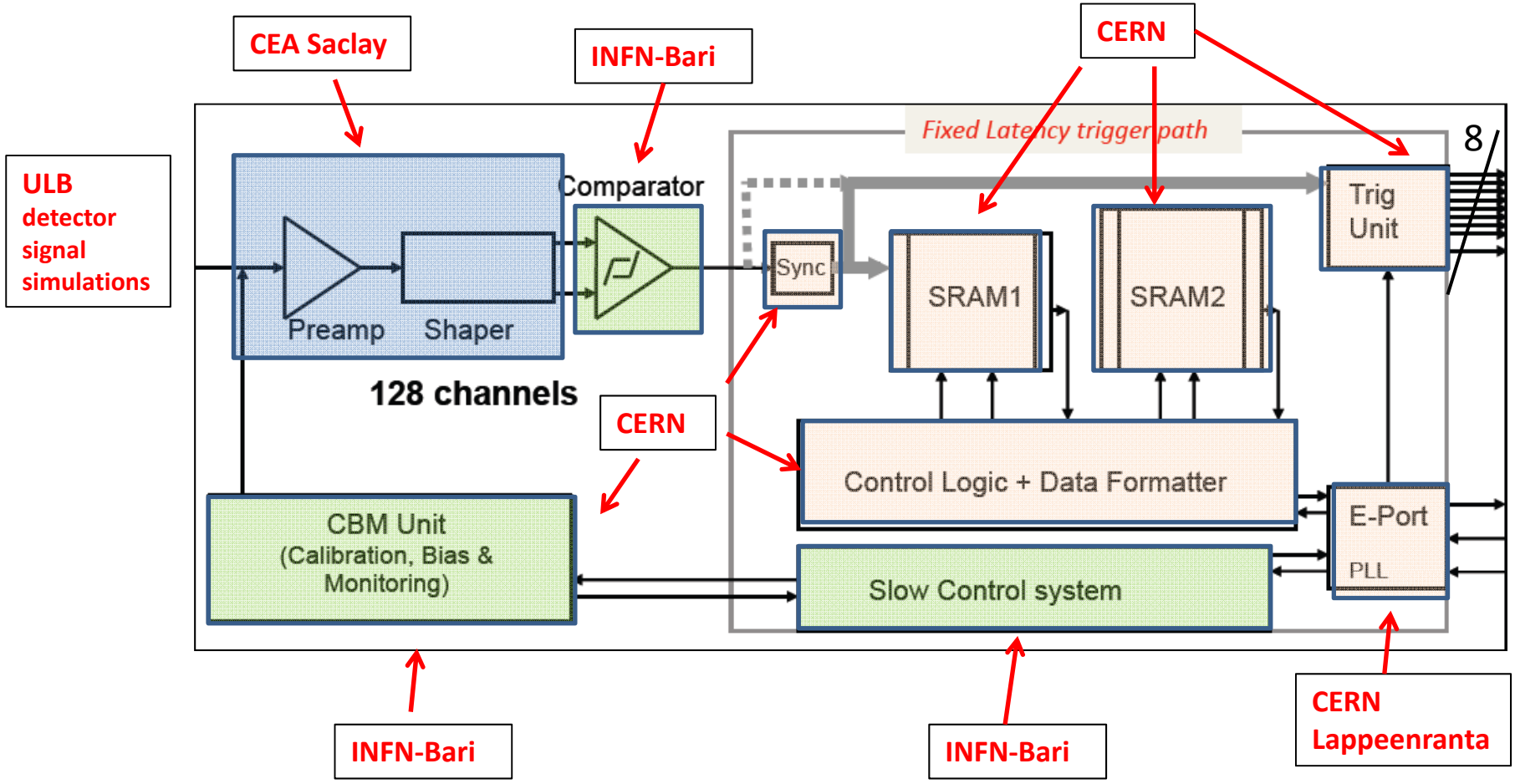
VFAT3 Status

F. Loddo
INFN-Bari

VFAT3 block diagram



Project coordination: Paul Aspell, CERN

Technology: IBM 130 nm

Detector studies & timing resolution (ULB)

Timing resolution determined by detector.

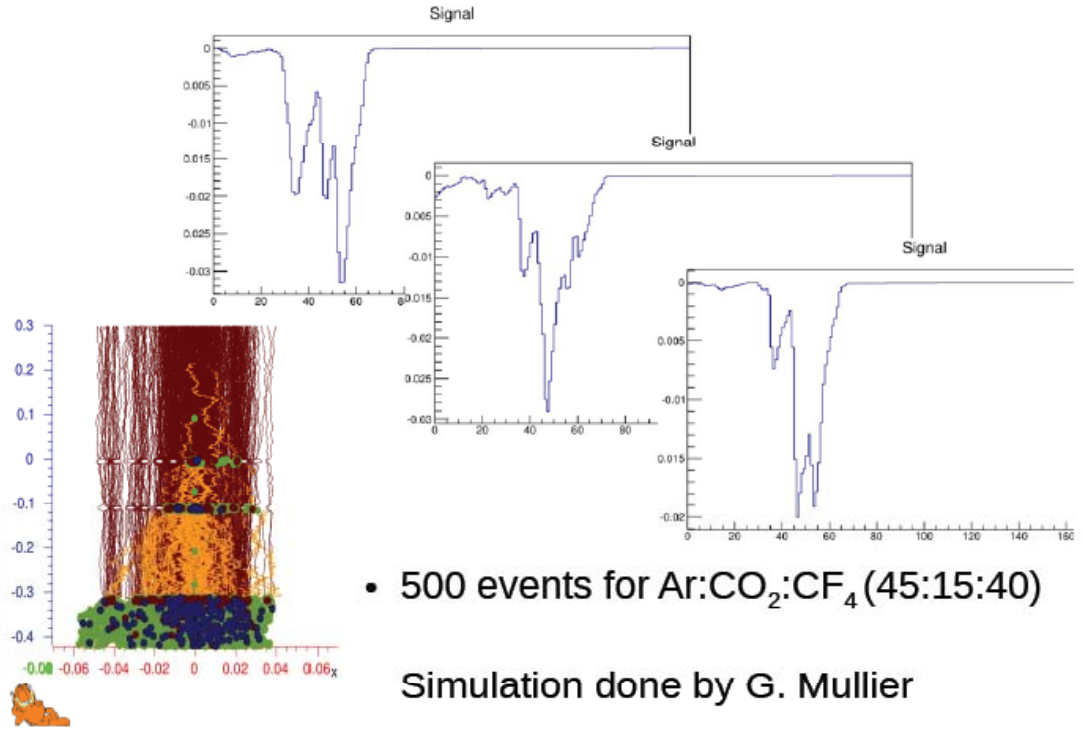
Fast shaping (as with VFAT2) give good timing resolution (<6ns) but bad signal to noise due to ballistic deficit.

Slower shaping times give better S/N but worse timing resolution due to time walk.

VFAT3 analog discriminator would use CFD or TOT to correct time walk and recover timing resolution.

ULB

GARFIELD simulations



- 500 events for $Ar:CO_2:CF_4$ (45:15:40)

Simulation done by G. Mullier

2

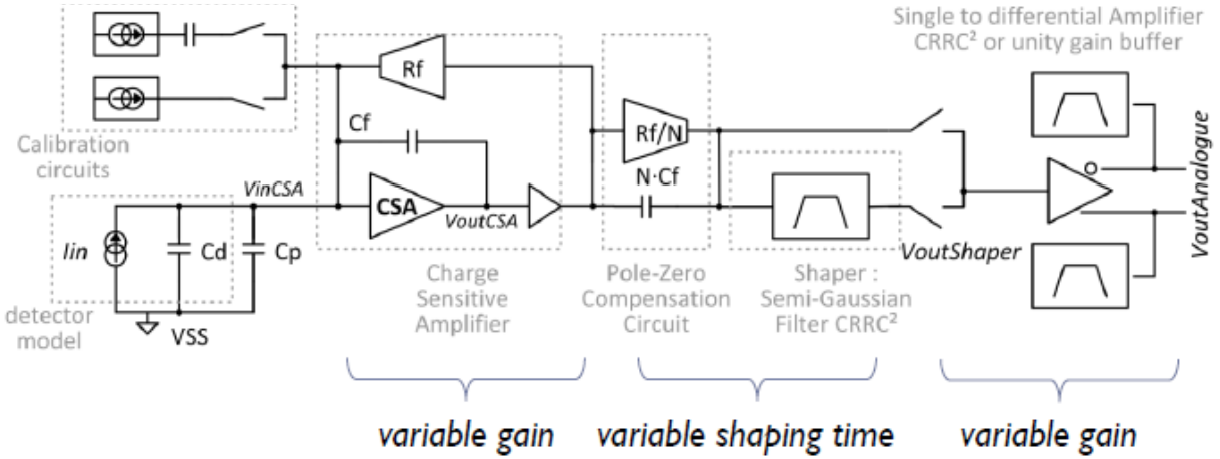
Simulations showed that both methods are suitable for improving the timing resolution when Tpeak > 25 ns

- Time Over Thresholds method takes longer to compute and requires LUT
- Constant Fraction Timing was chosen for VFAT3

T.Maerschalk, ULB

Front-end (F. Guilloux, CEA Saclay)

Parameter	FE (VFAT3/GdSP)	unit	Remarks
Input capacitance *	5 – 10 -30 – 60 – 80	pF	Simulation cases
Shaper peaking times	25 – 50 – 75 – 100 – 200 – 400	ns	programmable
Shaper order **	3rd order		
Input Leakage current compensation	10	nA	
Sensitivity ***	From 1.25 to 50	mV/fC	programmable
Polarity	dual		
Dynamic range	200 (400 for dimuon)	fC	
Linearity Error : small charges	<1	%	up to 100 fC
Linearity Error : high charges	<5	%	up to 200 fC
Power consumption	<2	mW/chan.	
Power supply voltage	1.5	V	
Noise	1100	e-	@ Tpeak = 100 ns @ 2 mW/chan @ Cin = 30pF
Technology	IBM 130nm		



Front-end simulation cases

(F. Guilloux, CEA Saclay)

Case 1: VFAT2 mode (Tp = 25 ns)

Detect. cap.	Noise (ENC)	Tpeak (ns)	Gain (mV/fC)	
10 pF	560 e-	23.5	14.5	
30 pF	1085 e-	26.7	14.1	
ENC slope	26 e-/pF	3.2	-0.4	Absolute variation
ENC0	298 e-	+13.6%	-2.8%	Relative variation

Case 2: TPC mode (Tp = 50 ns)

Detect. cap.	Noise (ENC)	Tpeak (ns)	Gain (mV/fC)	
10 pF	704 e-	54.2	9.79	
30 pF	999 e-	55.6	9.71	
ENC slope	15 e-/pF	1.4	-0.08	Absolute variation
ENC0	556 e-	+2.6%	-0.8%	Relative variation

Case 2: TPC/GEM mode (Tp = 75 ns)

Detect. cap.	Noise (ENC)	Tpeak (ns)	Gain (mV/fC)	
10 pF	668 e-	77.9	9.78	
30 pF	898 e-	78.4	9.72	
ENC slope	12 e-/pF	0.5	-0.06	Absolute variation
ENC0	553 e-	+0.6%	-0.6%	Relative variation

Case 2: TPC/GEM mode (Tp = 100 ns)

Detect. cap.	Noise (ENC)	Tpeak (ns)	Gain (mV/fC)	
10 pF	641 e-	107.7	9.86	
30 pF	905 e-	108.3	9.81	
ENC slope	13 e-/pF	0.6	-0.05	Absolute variation
ENC0	509 e-	+0.6%	-0.5%	Relative variation

Calibration test pulsing

2 options:

Step voltage – series capacitor (delta-like current pulse)

- Programmable amplitude (-2fC to 63 fC and +2fC to -64 fC)
- Programmable polarity
- Programmable phase, steps of 3.125ns (i.e. 25ns / 8)
- Single channel/More channels at the same time (reduced accuracy)
- Internal/external test pulse

Current pulse (DC-coupled to preamp)

- Programmable amplitude (-64 fC to 64 fC)
- Programmable polarity
- Programmable phase, steps of 3.125ns (i.e. 25ns / 8)
- Programmable pulse duration, 1,2,3,4 clock periods
- Single channel
- Pile-up, ballistic deficit studies

Bias & Monitoring

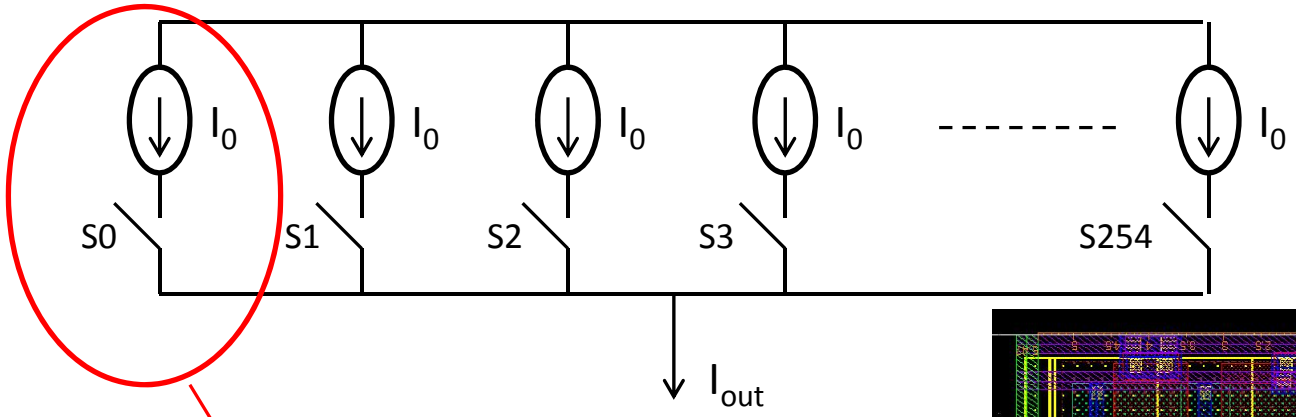
- All the bias currents/voltages will be remotely controlled
  → Internal 8-bit DACs

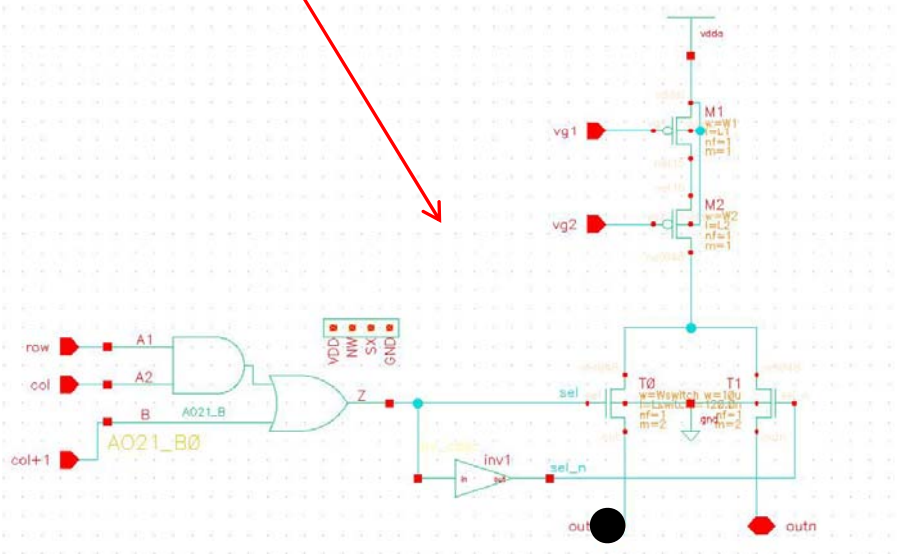
- All the bias currents/voltages will be remotely monitored
  → Internal ADC

- Internal temperature sensor

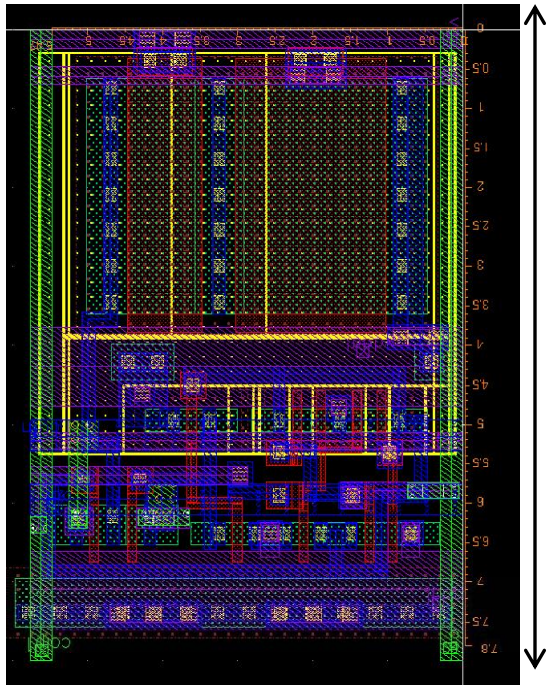
8-bit Current DAC

Thermometer coded: 255 “identical” unit current sources connected to output node through switches controlled by a binary-to-thermometer decoder





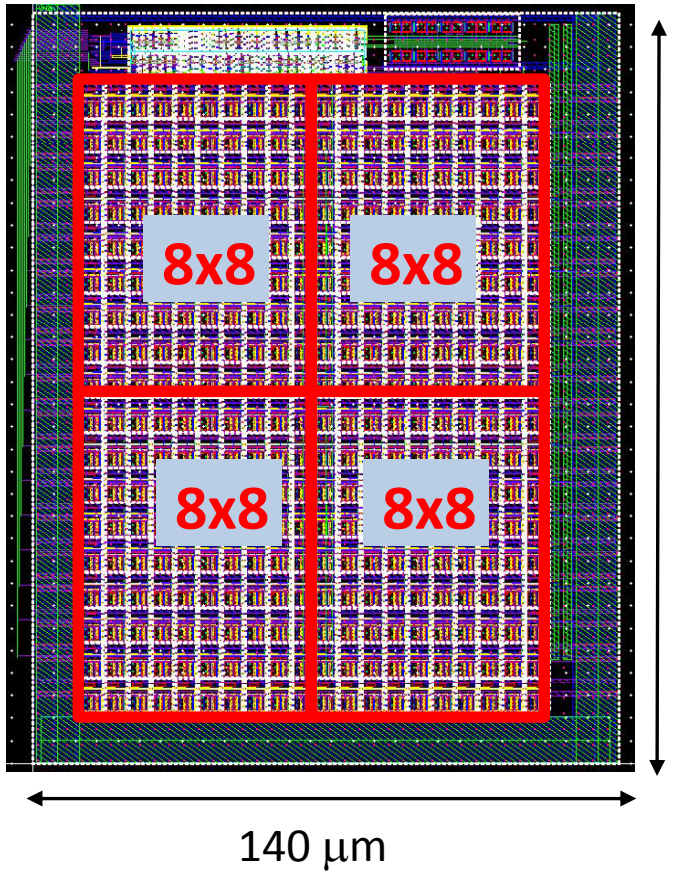
Vout



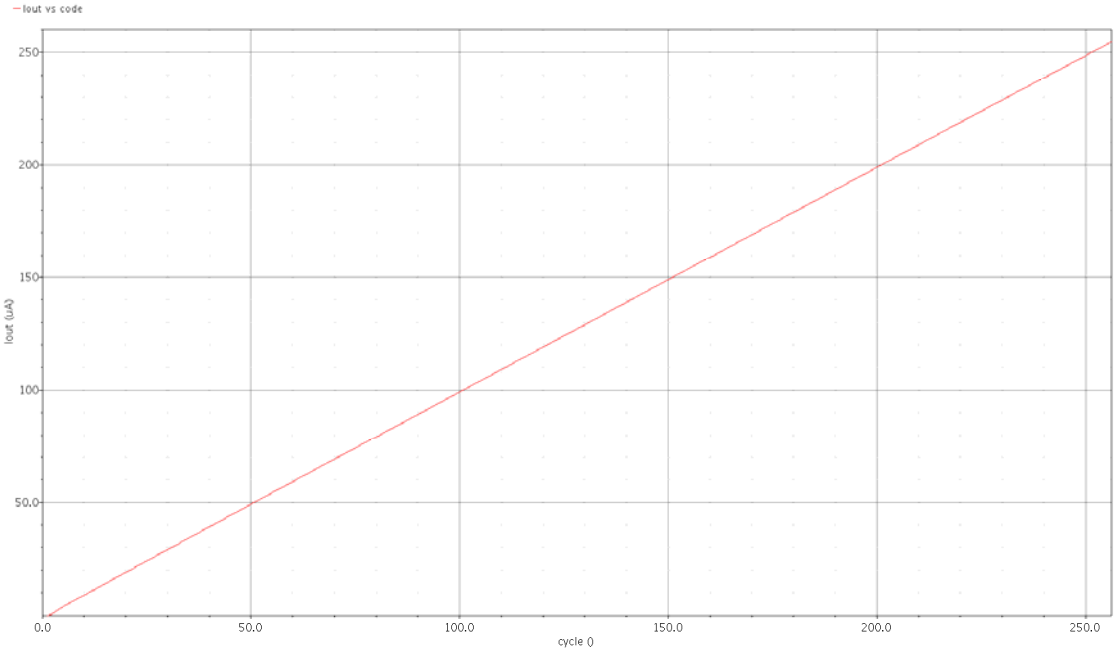
7.8 μm

5.5 μm

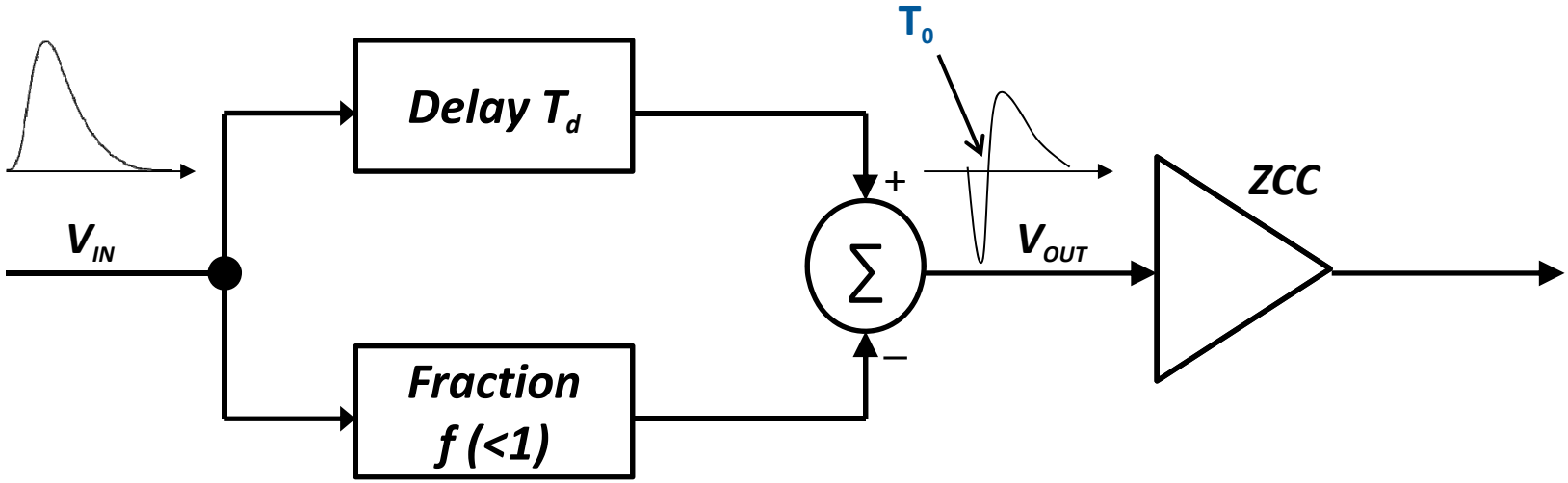
8-bit Current DAC



I_{out} vs input code



Constant Fraction Discriminator: principle of operation



Creation of a variable threshold tracking the signal always at a certain fraction of its amplitude

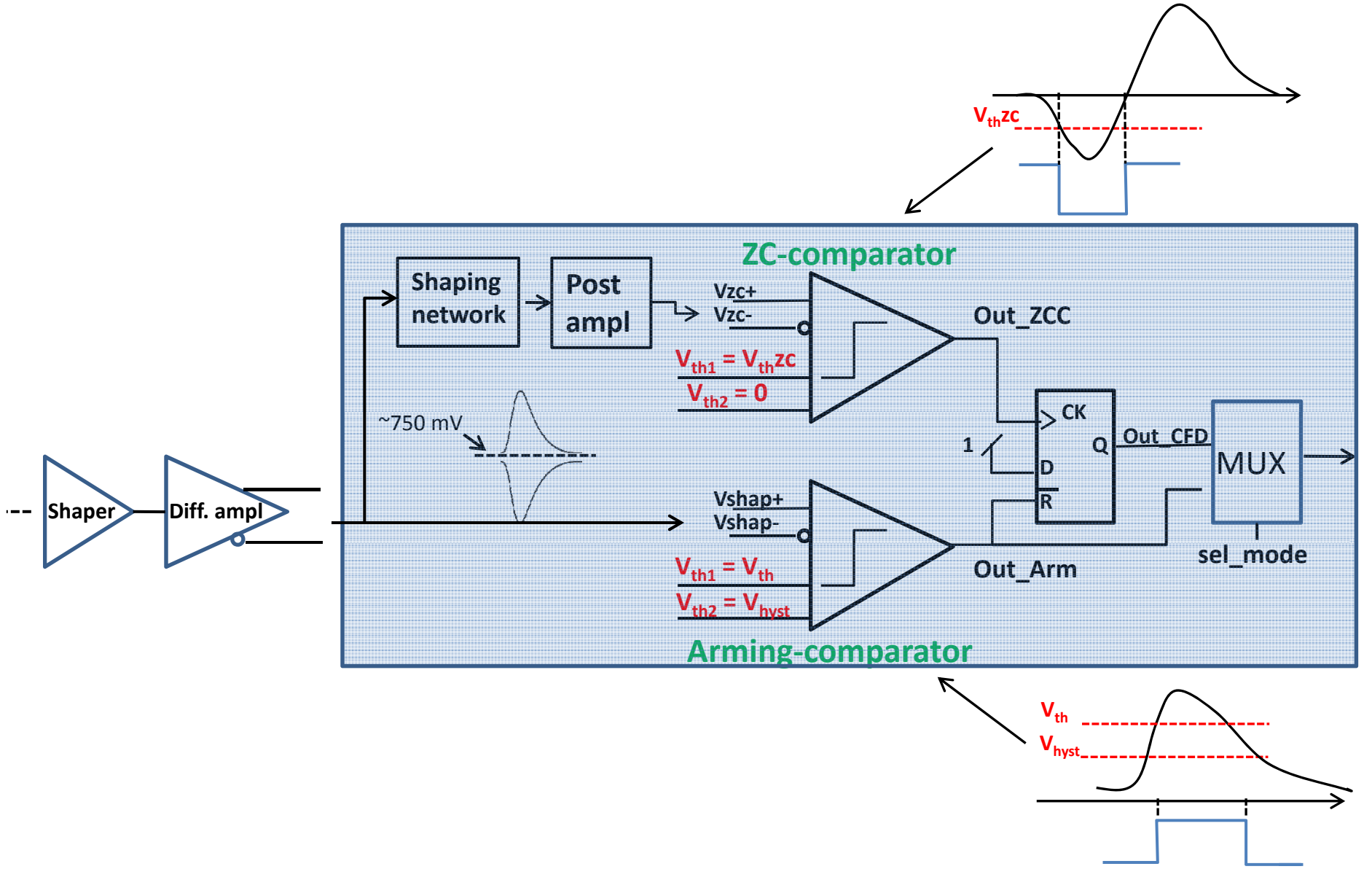
$$V_{OUT}(t) = V_{IN}(t - T_d) - f * V_{IN}(t)$$

The output bipolar signal has a zero crossing time T_0 depending only on network parameters (T_d, f)

$T_d > (1\text{-}f) * T_p$ ***TRUE CONSTANT FRACTION TIMING TCF***

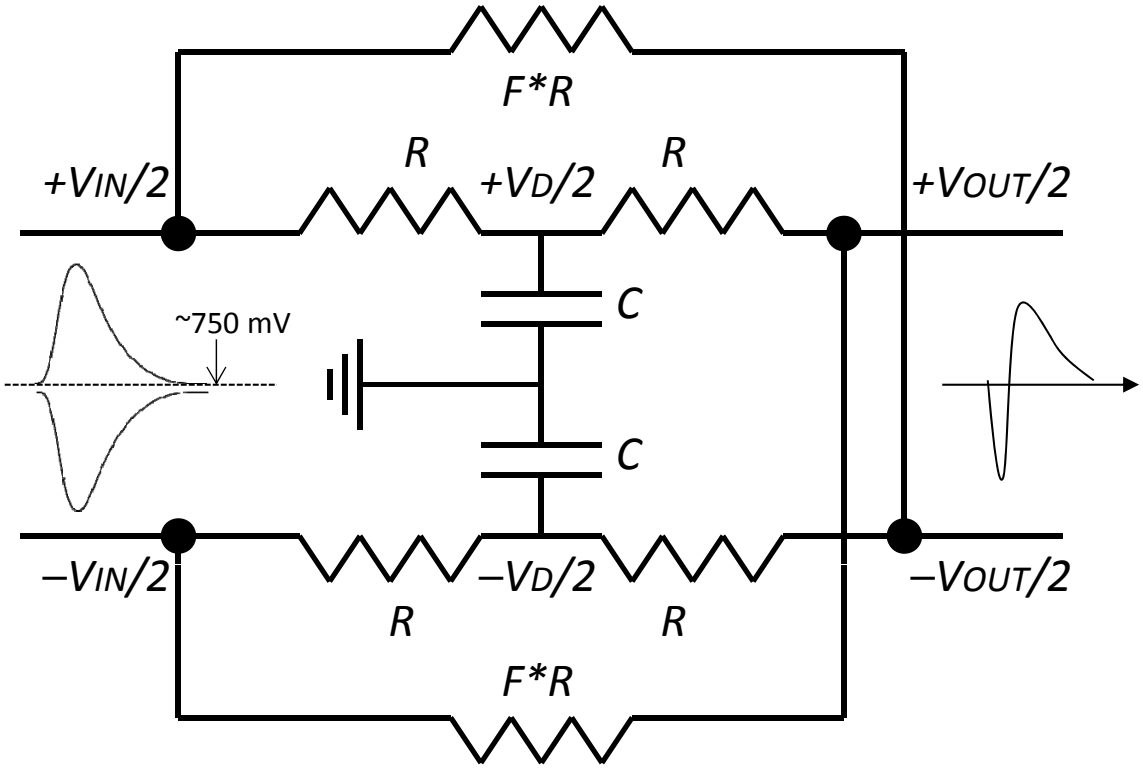
$T_d < (1\text{-}f) * T_p$ ***AMPLITUDE AND RISE TIME COMPENSATED TIMING ARC***

Constant Fraction Discriminator



Shaping network

Cross coupling topology



Main Advantage :

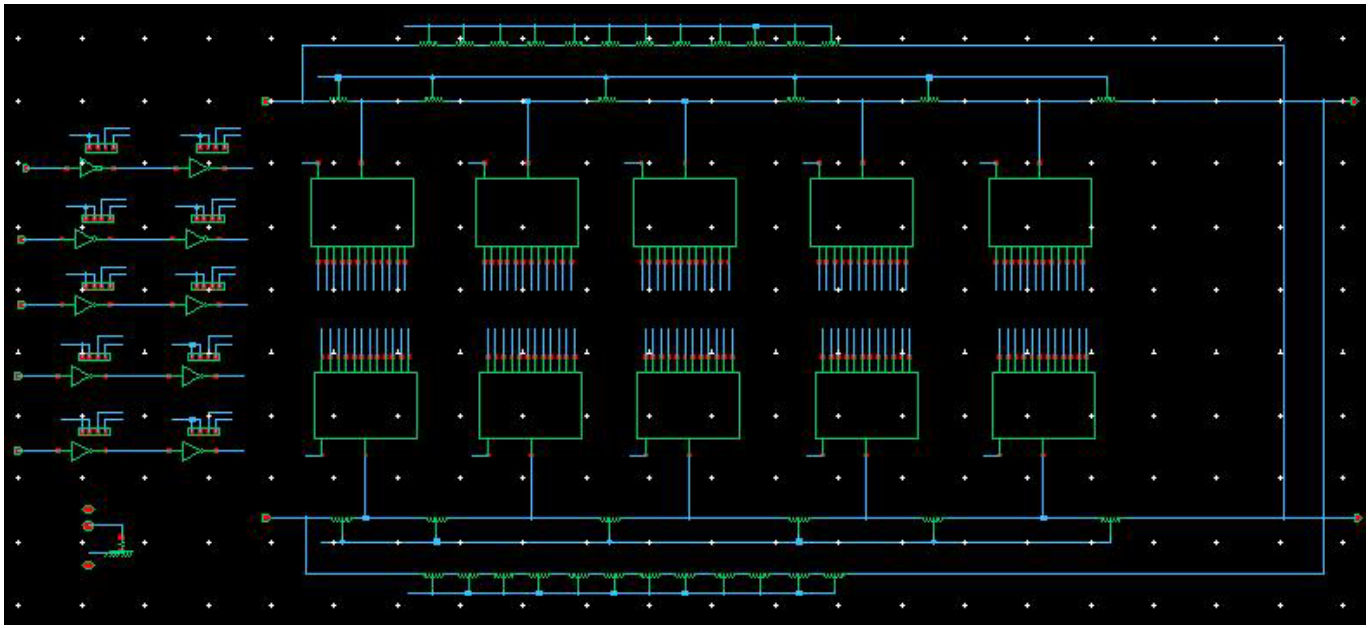
The fully differential structure provides very good rejection of common mode noise injected in the substrate by the switching digital logic

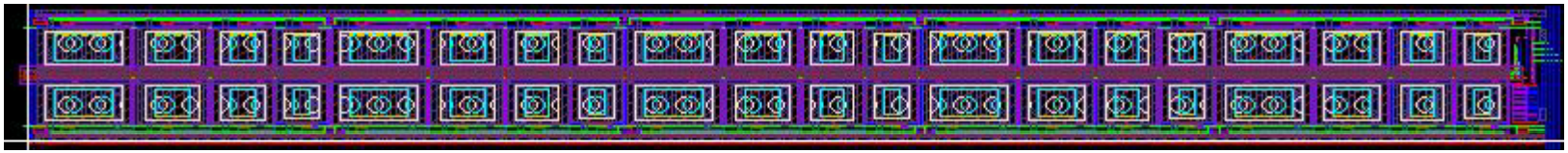
S. Garbolino, S. Martoiu and A. Rivetti

Implementantion of Constant-Fraction-Discriminators (CFD) in Sub-micron CMOS Technologies

2011 IEEE Nuclear Science Symposium Conference Record

Shaping network

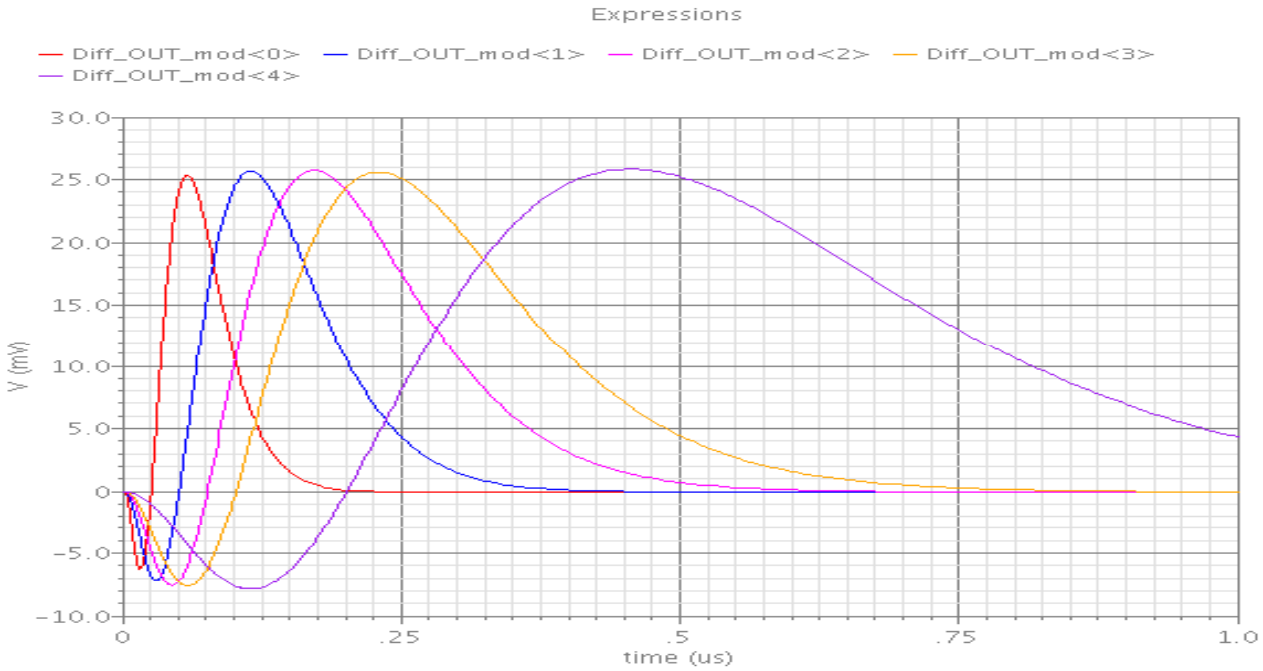




900x76 μm^2

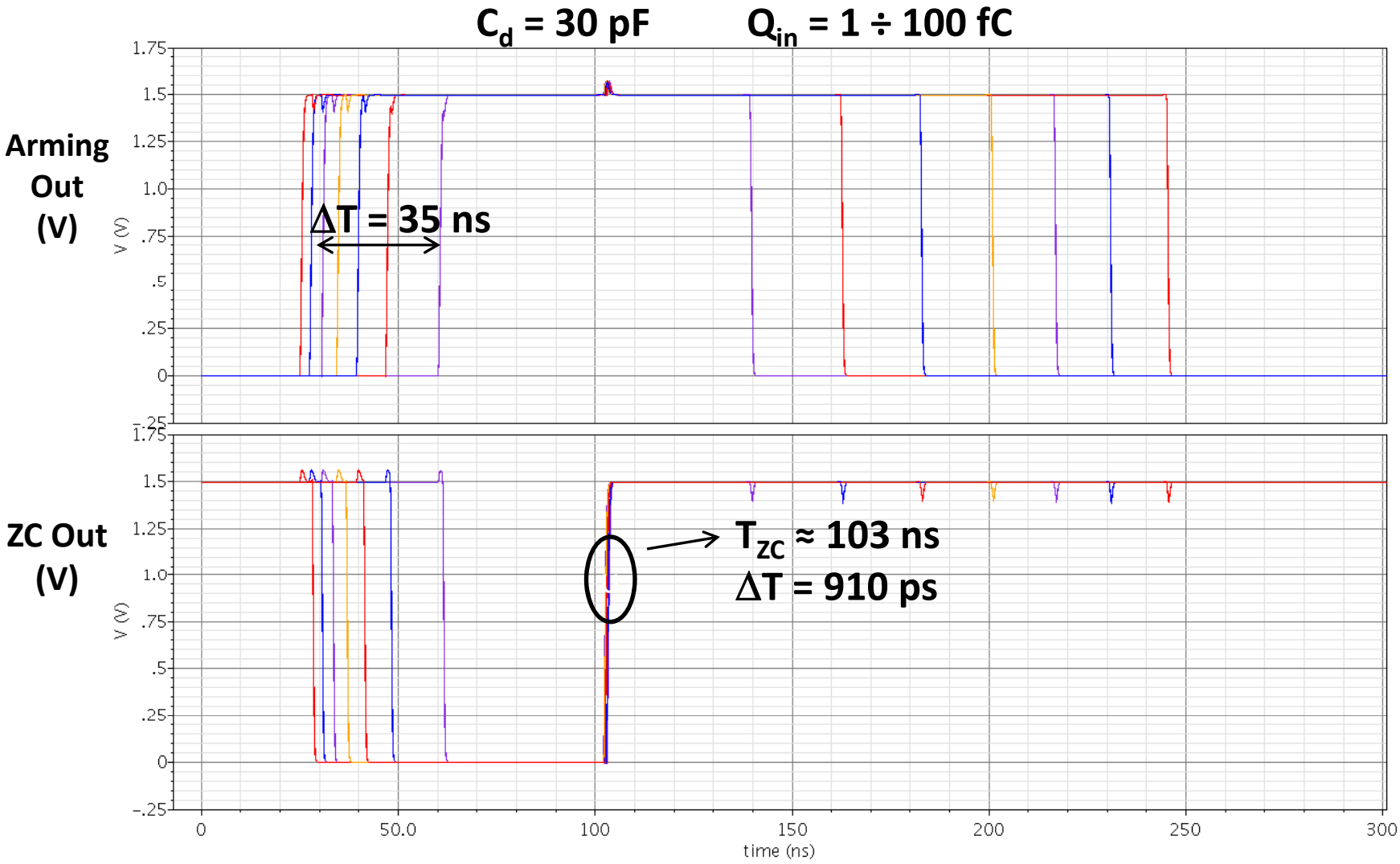
- Selectable time constant, to optimize S/N → Jitter according to Tpeak

Shaping network



T_p [ns]	Crossing Time T_0 [ns]	Delay Time T_d [ns]	Fraction Factor	ΔT_0 [ns] (10 ÷ 1000 mV)
25	24.75	15	0.393	0.07
50	49.77	29.07	0.416	0.07
75	75.12	43.41	0.422	0.14
100	100.45	57.82	0.424	0.1

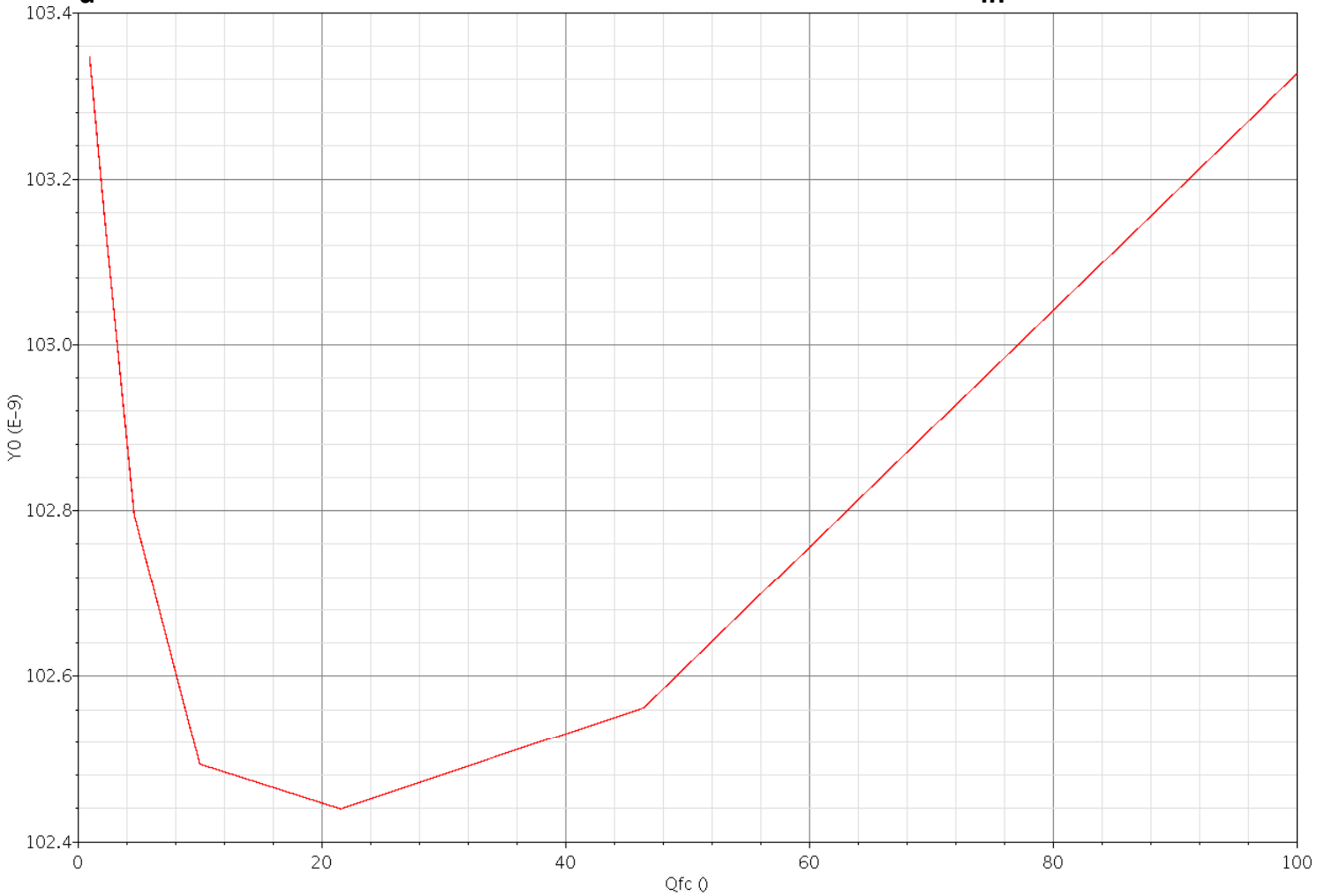
Post layout CFD simulations (T_p = 50 ns)



Post layout CFD simulations (T_p = 50 ns)

C_d = 30 pF FE gain = 10 mV/fC Q_{in} = 1 ÷ 100 fC

T_{ZC} (s)



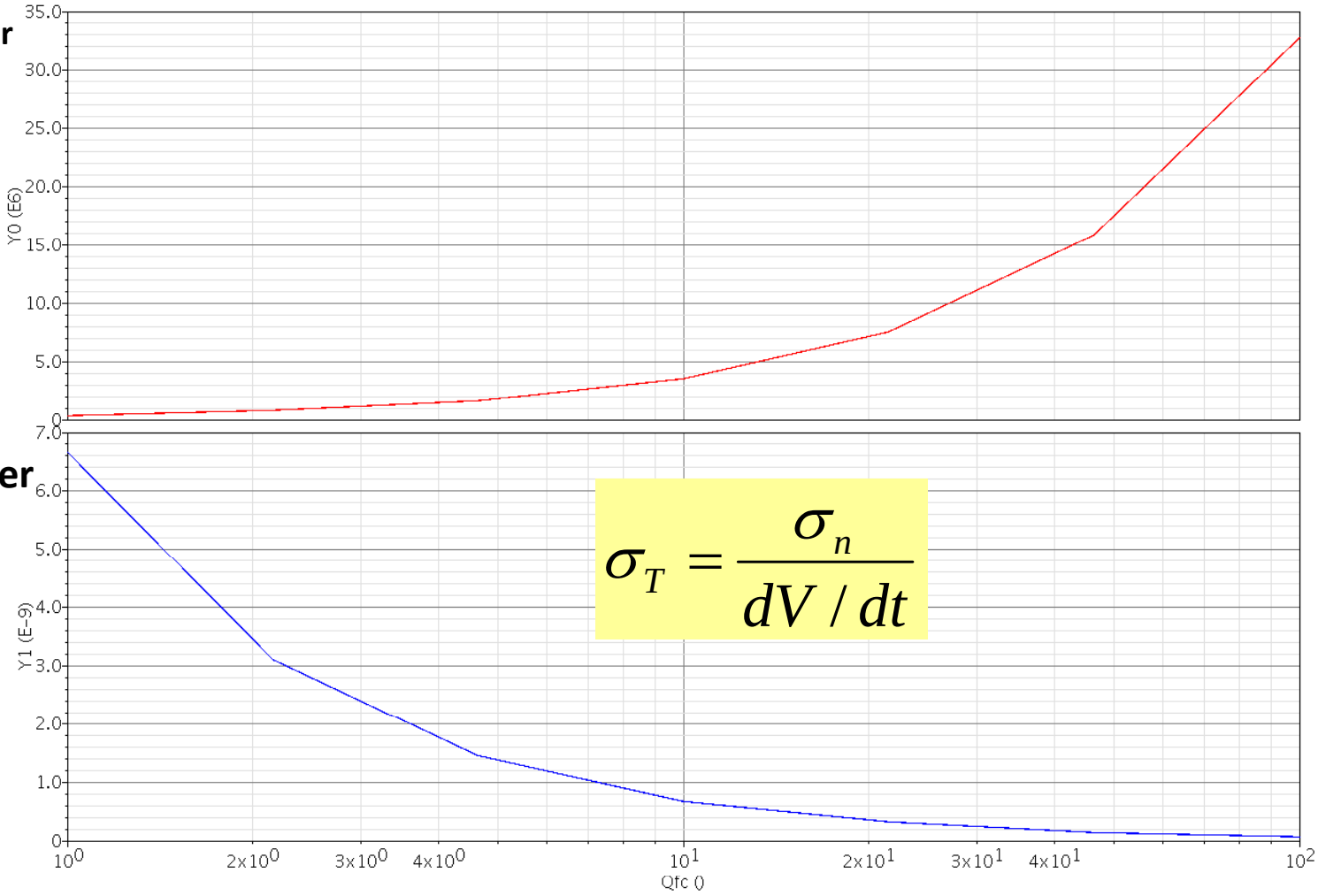
Time walk ~ 910 ps

Post layout CFD simulations (T_p = 50 ns)

C_d = 30 pF **FE gain = 10 mV/fC** **Q_{in} = 1 ÷ 100 fC**

Post Amplifier Slew Rate (V/s)

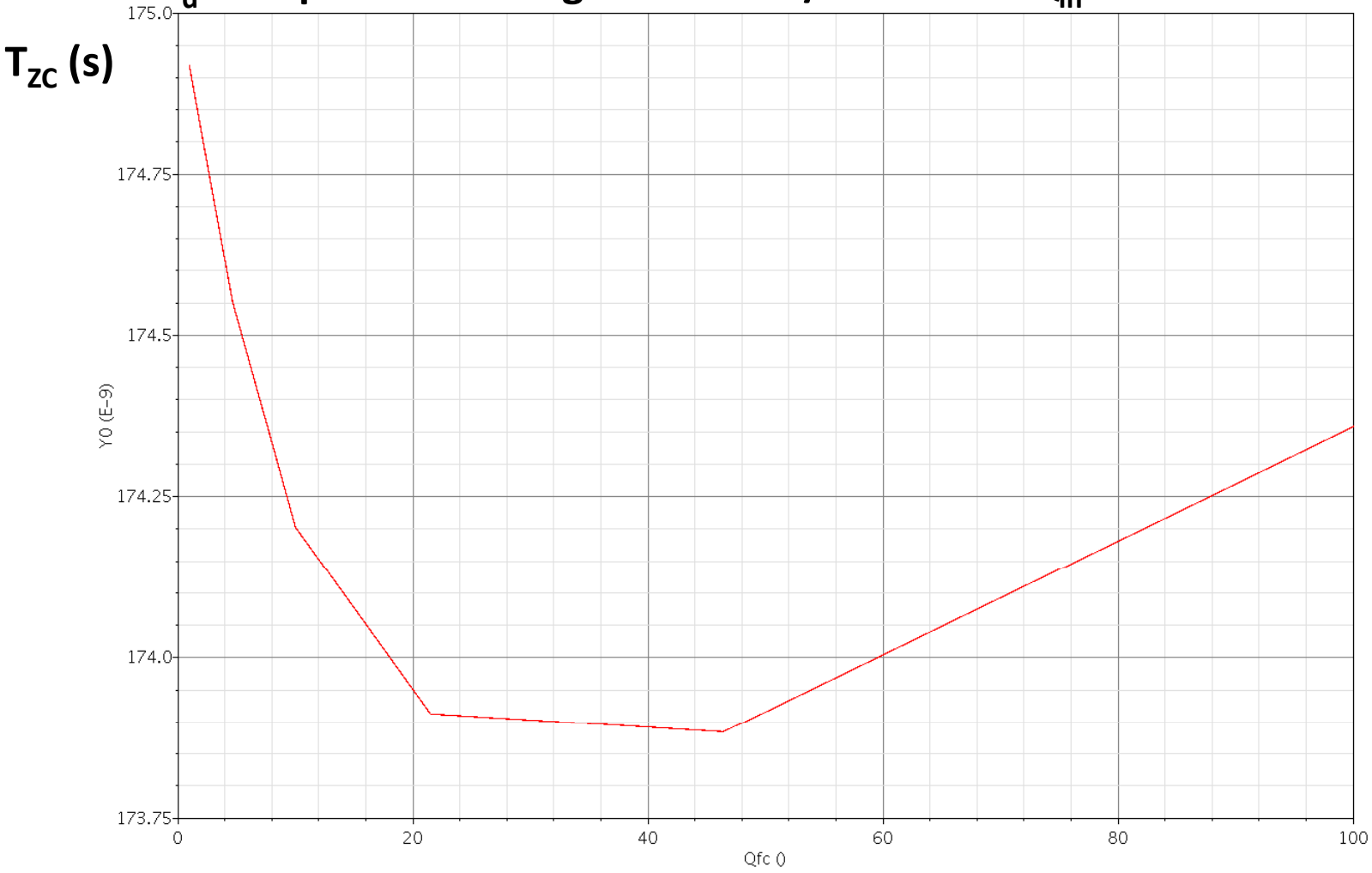
Post Amplifier Jitter (s)



$$\sigma_T = \frac{\sigma_n}{dV/dt}$$

Post layout CFD simulations (T_p = 100 ns)

C_d = 30 pF FE gain = 10 mV/fC Q_{in} = 1 ÷ 100 fC



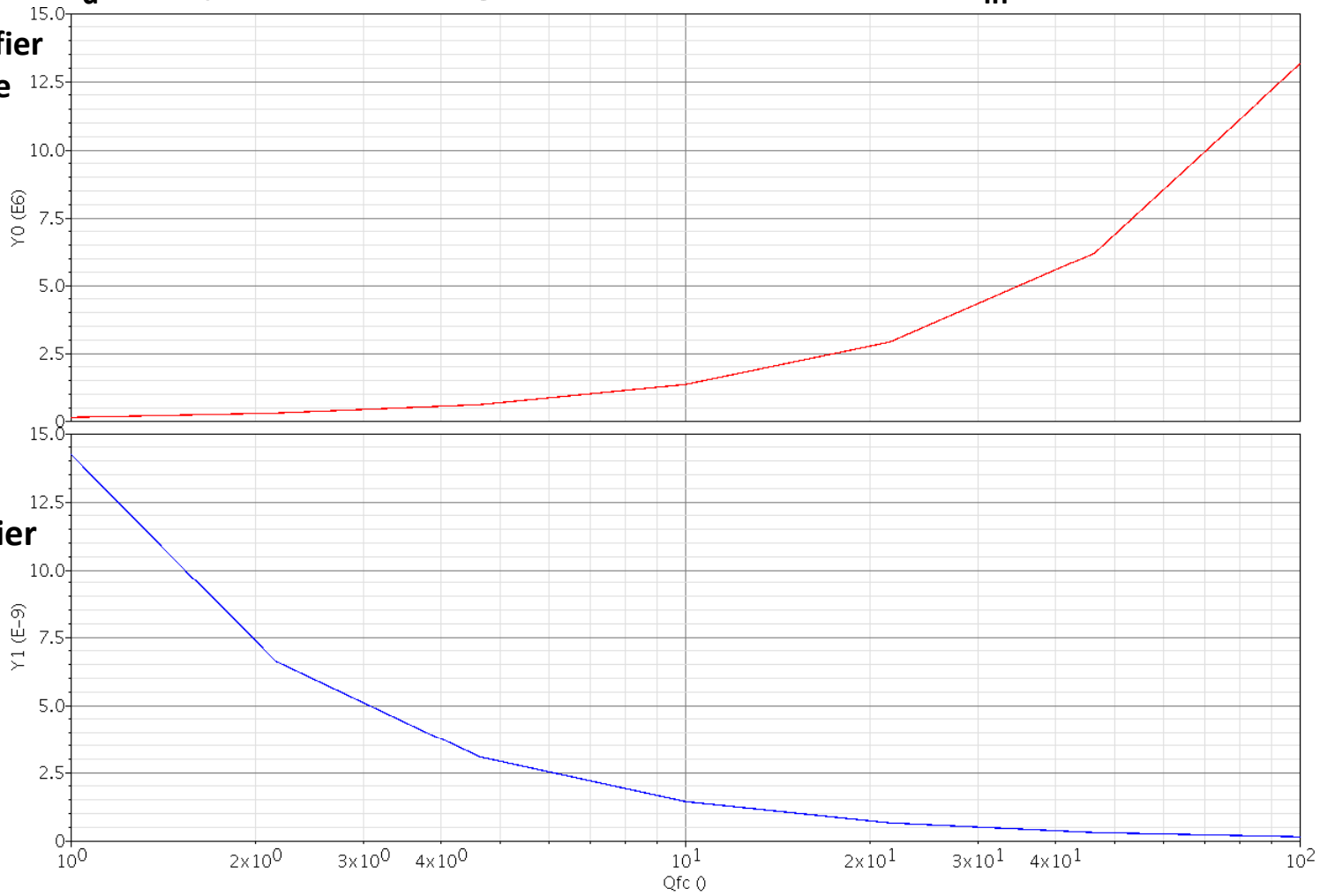
Time walk ~ 1 ns

Post layout CFD simulations (T_p = 100 ns)

C_d = 30 pF **FE gain = 10 mV/fC** **Q_{in} = 1 ÷ 100 fC**

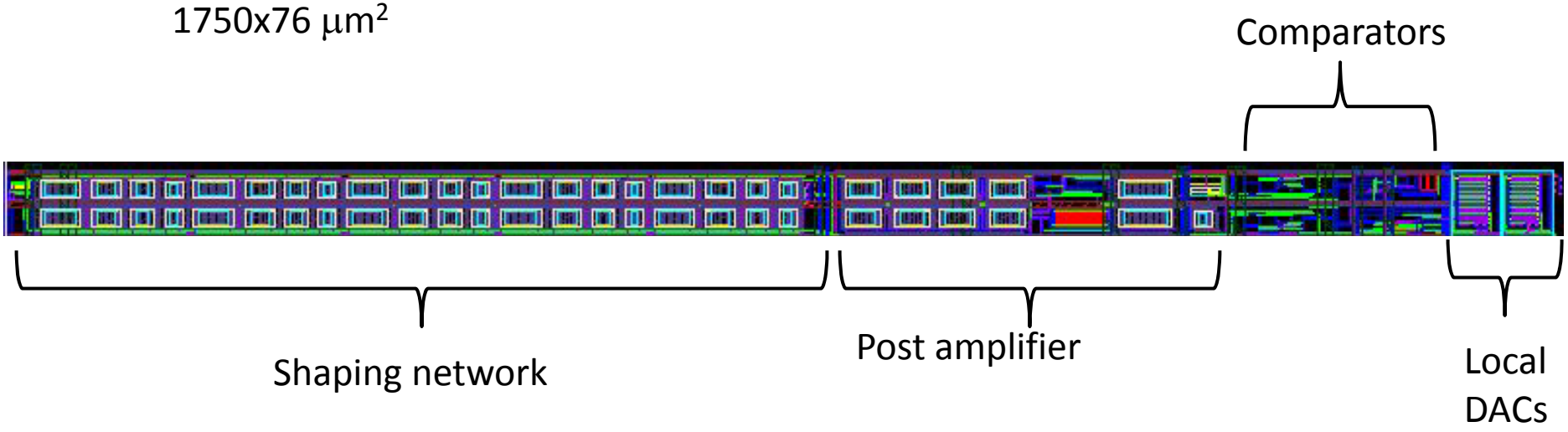
Post Amplifier Slew Rate (V/s)

Post Amplifier Jitter (s)



CFD layout

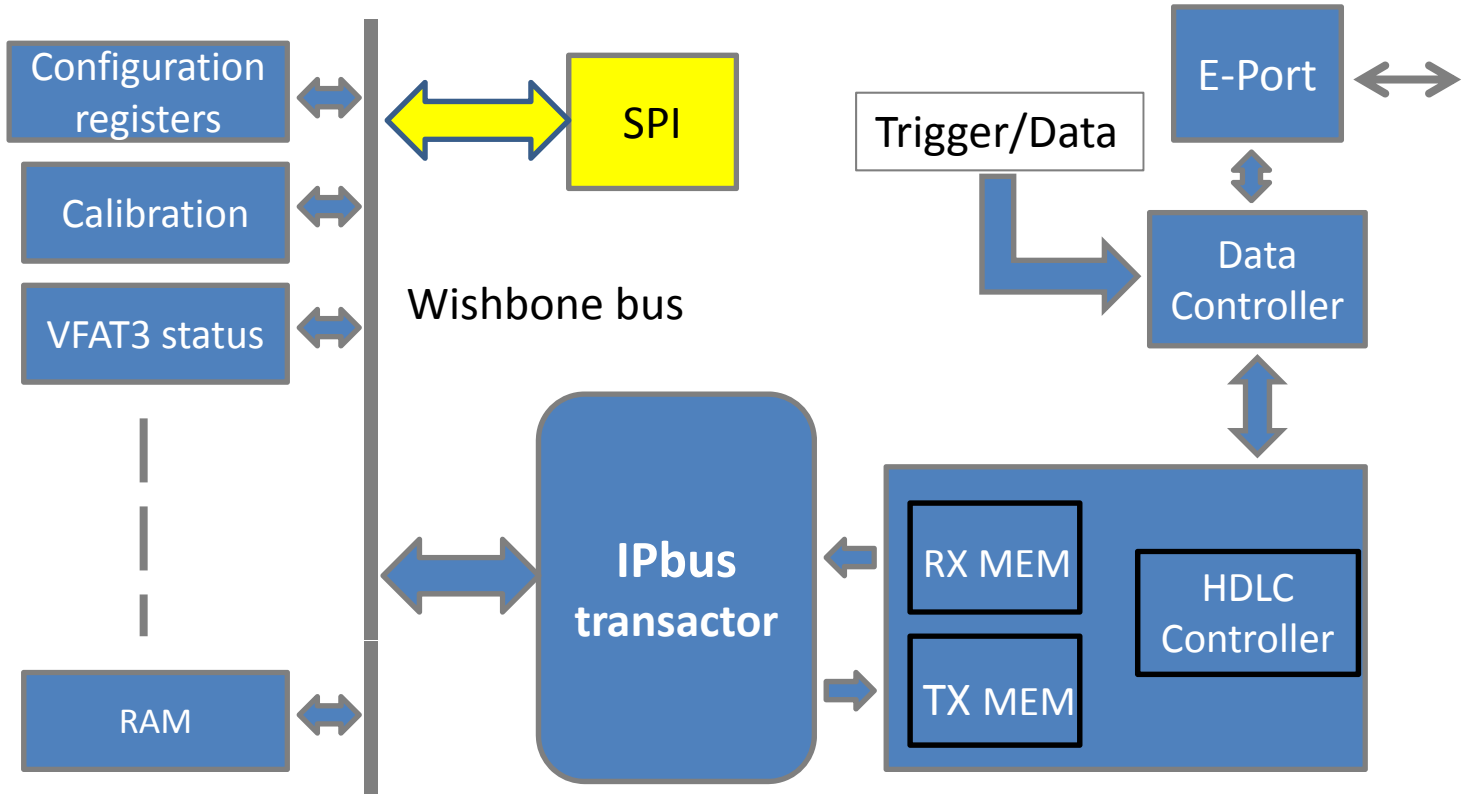
1750x76 μm^2



- Local DACs:
  - (6+1) bits fine arming Thr
  - (6+1) bits fine ZCC Thr

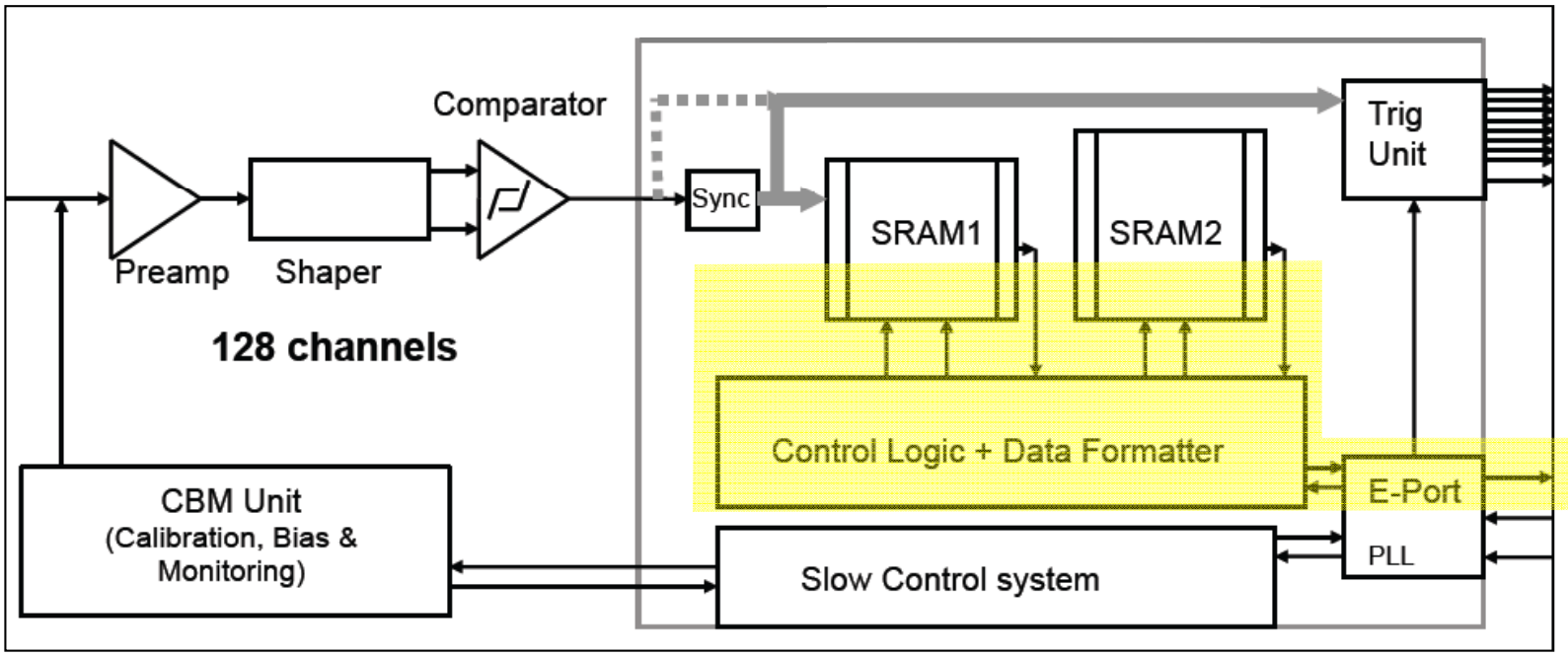
} 14 bits/channel

Slow control block diagram
(G. De Robertis)



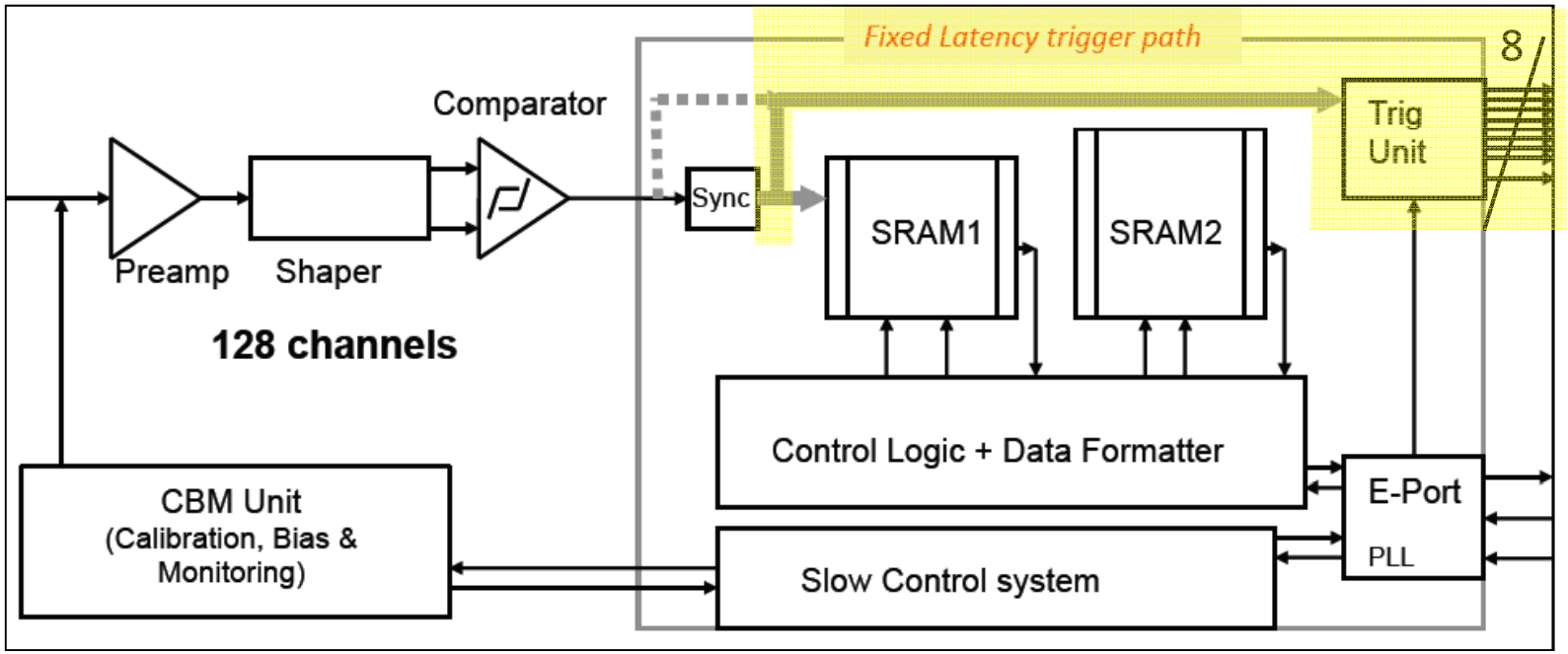
- **Large programmable register bank with read/write access with hardwired default value**
- **IP-bus communication protocol**
- **Delivered through e-links and E-port, with backup SPI interface for test purpose**

Variable Latency Data Path



- Full granularity via e-port
- Data are read upon LV1A arrival
- SRAMs size according to LV1A max. latency (3.2 us → 20 us) and rate specification
- Data are transmitted with timestamp to identify the BX
- Data Types:
    1. Lossless
    2. SPZS (Sequential Partition Zero Suppression): zero suppression, packet size depends on the number of hits, highest transmission rate, but in case of high occupancy some losses may occur

Fixed Latency Trigger Path



- Fast hit information synchronous with LHC 40 MHz clock (does not contain time stamp)

- 8 SLVS output pairs @ 320 MHz → 64 bits/BX

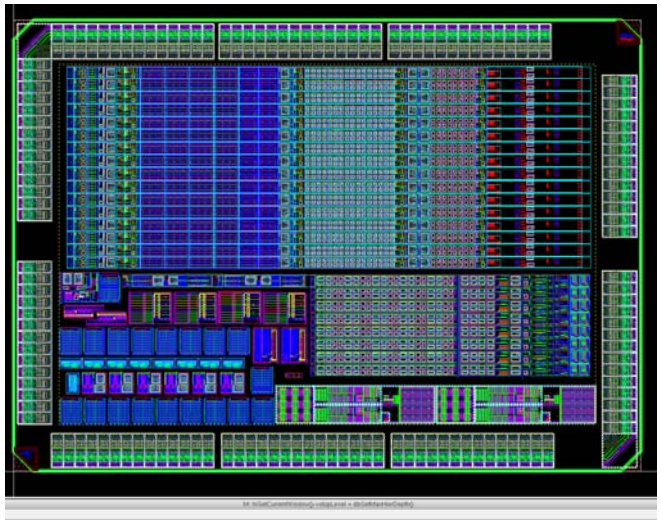
- Programmability:
    1. Fast OR: Granularity = 2 channels (or 4 channels)
    2. SPZS (Sequential Partition Zero Suppression): Fully granularity (in case of high occupancy some losses may occur)

Status of VFAT3

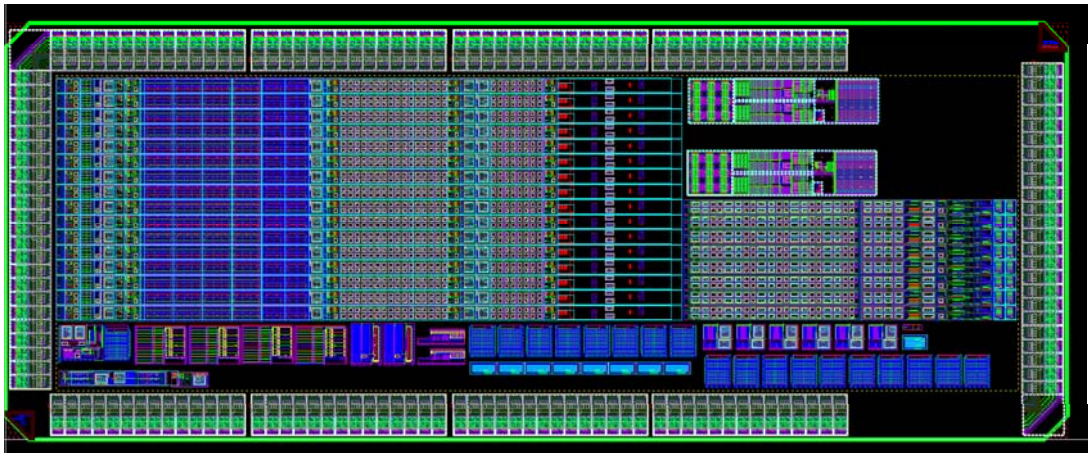
- The design of the Front-End, CBM and CFD is almost done

- On Feb.2014 the 1st prototype (namely **CFE**) will be submitted to foundry
- It will house only the analog blocks (8 channels + 4 test channels) and a simple slow control interface, in order to check the amplifier (analog outputs) and CFD performance

- Soon after, the design of the first 128-channel VFAT3 will start



or



CFE floorplans