LAR PHASE II

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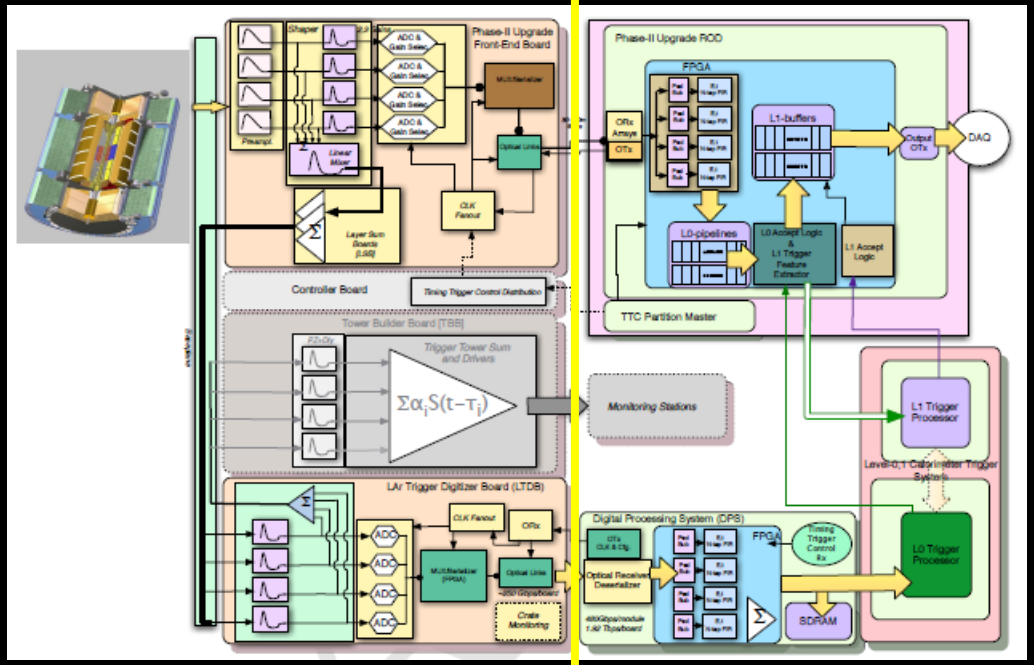
Phase II Upgrade of LAr Cal Readout

Front end



Back end

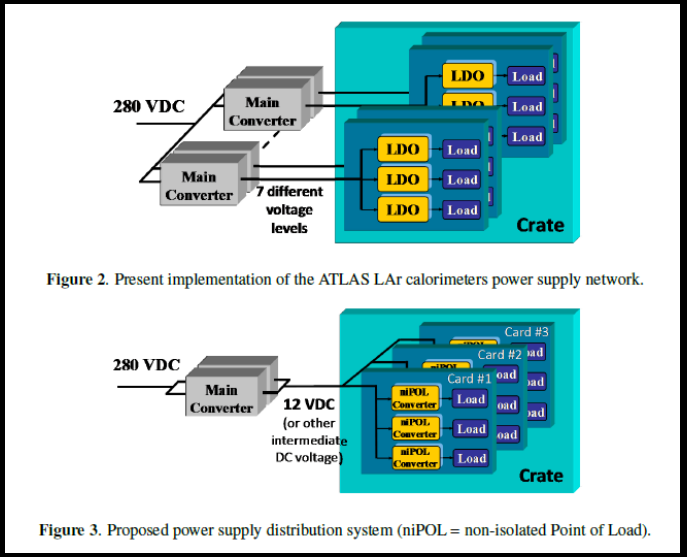
- Ageing and radiation tolerance of front-end electronics limit longevity of present system
- Limited on-detector pipelines prevent application of more advanced trigger algorithms
- Free-running readout of all 182468 channels with 40 MHz front-end ADCs and optical transmission to back-end → total bandwidth 140 Tbps
- Front-end with more radiation tolerant components→ trigger buffers will be off-detector
- Upgraded trigger read-out foreseen in LS2 will be used for low-latency Level-0 trigger in Phase II

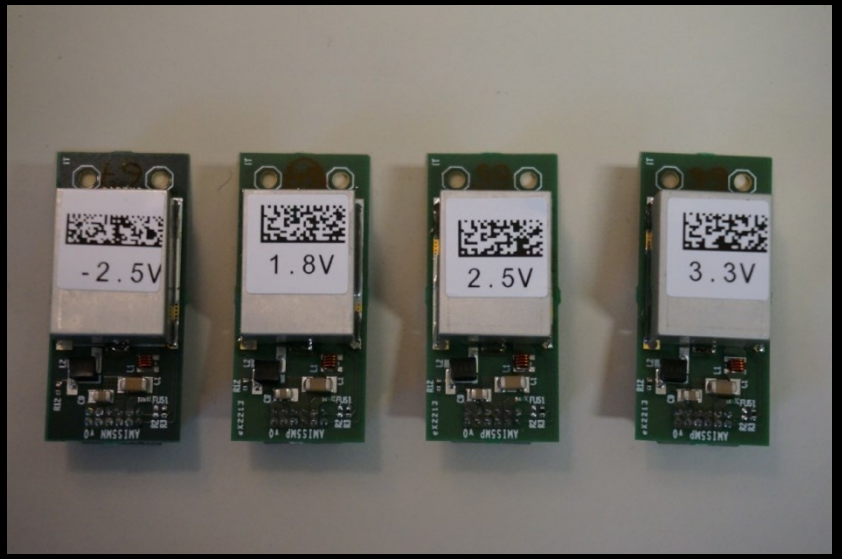
Front-end electronics

- Front-end electronics outside the LAr cryostat is foreseen to be replaced (except new Phase I electronics) → radiation tolerance for 3000 fb-1 and system longevity
- Replace all FEBs (→FEB2)
- Design a new pre-amplifier + shaper integrated in a single ASIC:
  - Low noise, 16-bit dynamic range, followed by low power differential shaping stages
  - SiGe BiCMOS technology
    - Investigations performed with IBM 8WL

Power distribution

- New scheme to distribute power to on-detector electronics (FEBs, LTDBs, …)
  - AC/DC converter located in USA15 which provides a 280 V output
  - 58 main DC-DC converters (LVPS)
- Present system:
  - generating 7 output voltages from -7V to +11 V
  - followed by low drop-out (LDO) regulators
- Future system:
  - generating an intermediate voltage (eg, 12V)
  - Followed by non-isolated Point of Load (POL) DC-DC converters.
- Need to select components rad-tolerant and that can operate in a magnetic field
- We are developing this approach for LTDBs for Phase I upgrade and then will extend it to rest of the FE electronics
- We are now testing in Milano some POLs designed at CERN (V_{in}=12V, various V_{out}, I_{out}=4A max)





Back end

- Interest in participating to the implementation of algorithm on the digitized data from the FEB2
- The data are received using serial optical links on multi-fiber ribbons. The conversion to electronic signal will be performed by commercial components and deserialization will be handled by fast FPGA transceivers.
- The Pre-Processor boards will apply digital filtering using FPGAs to calculate calibrated energy deposits together with the signal time for each LAr cell as well as signal quality criteria. (takes electronic and pile-up noise into account and, adjustable to the expected high-luminosity conditions)
- The processed data will be buffered in digital memory blocks.
- The data from the individual LAr cells are further processed by the Pre-Processor boards in order to provide input to the Level-1 hardware trigger. The signal processing may go beyond simple sums of cell energy, ET,…
  - more complex algorithms like the extraction of features of EM shower shapes, fast tagging of $\pi^0 \rightarrow \gamma\gamma$,...