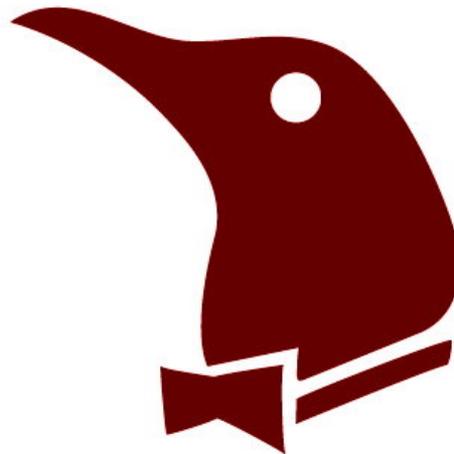


Detector review: **Photon vetoes**

Matthew Moulson
Frascati/CERN

NA62 Collaboration Meeting
Ferrara, 4 September 2014

LAV construction & installation status



NA62 - LNF

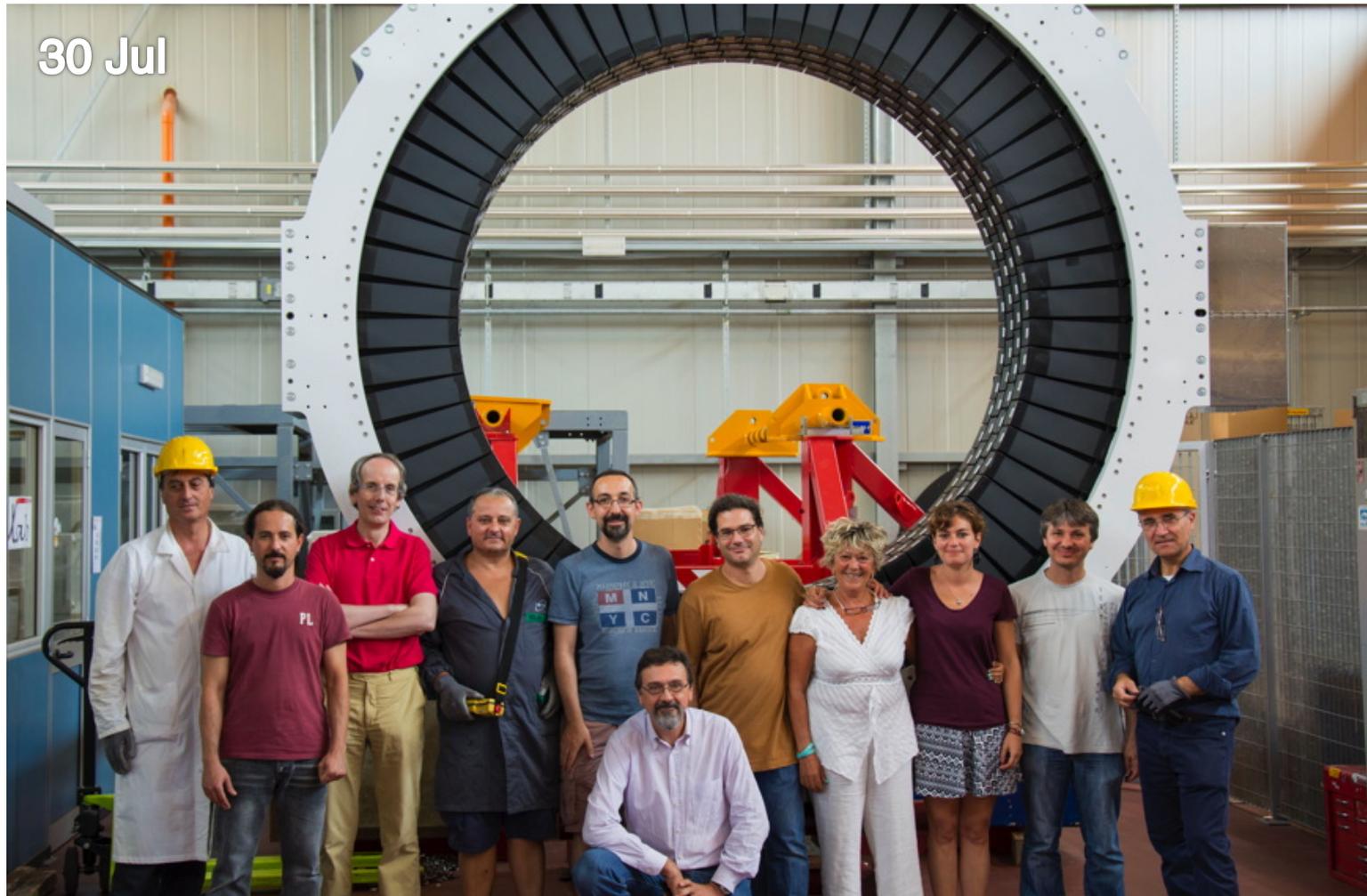
Matthew Moulson for the LAV Working Group
NA62 Photon-Veto Working Group Meeting
Ferrara, 03 September 2014

Since last meeting:

- 09-13/06** **Installation V26, V28 tubes, A10 & A11**
Minor problems adapting old feet to one of the new vacuum tubes, otherwise smooth
- 23/06-04/07** **Finish cabling A6-A8**
Crate installation A9-A11
- 05-07/08** **A12 delivered to CERN**
- 18-29/08** **Installation of cable trays A9-A11**
Cabling A9-A11
- 25-29/08** **Installation of A12**

Plus: Continuous effort by F. Gonnella to configure crates and install FEE throughout the summer

Rotation and cradle test for A12



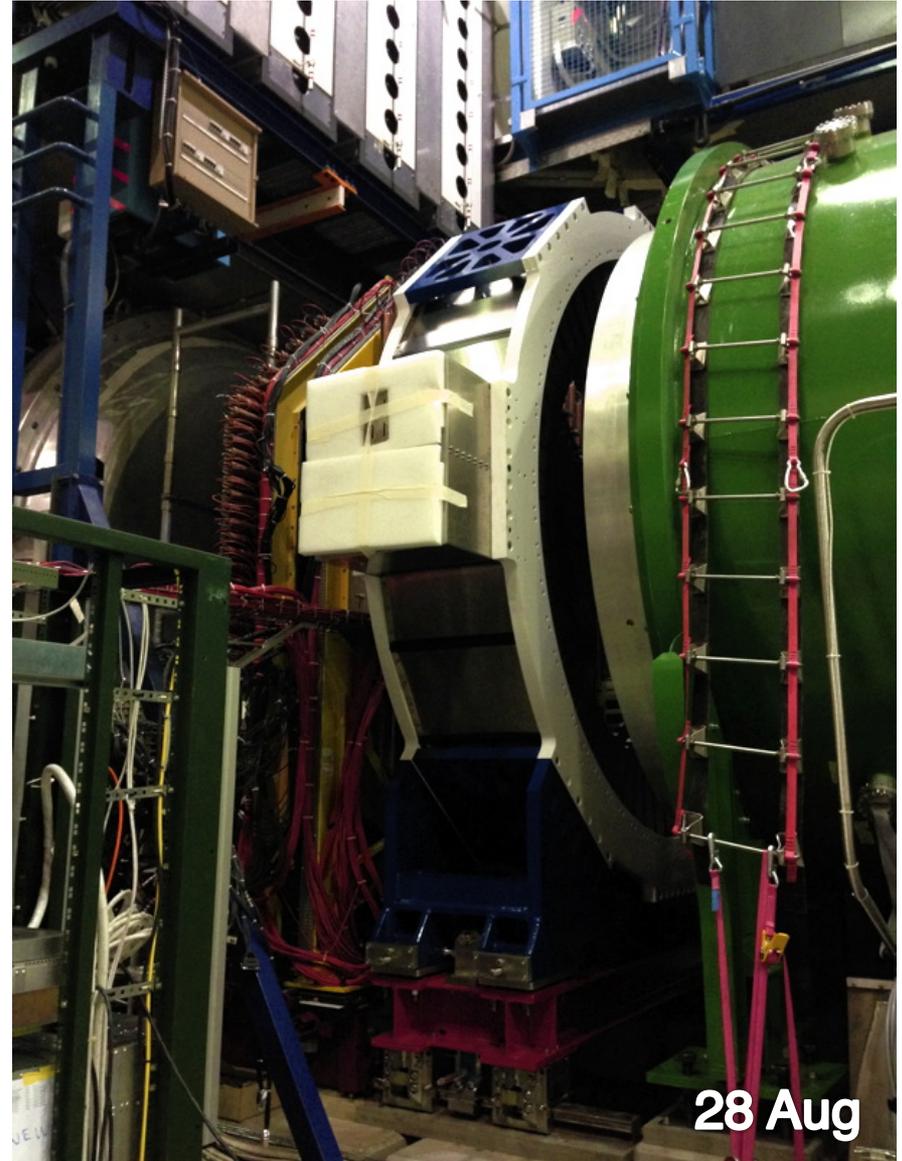
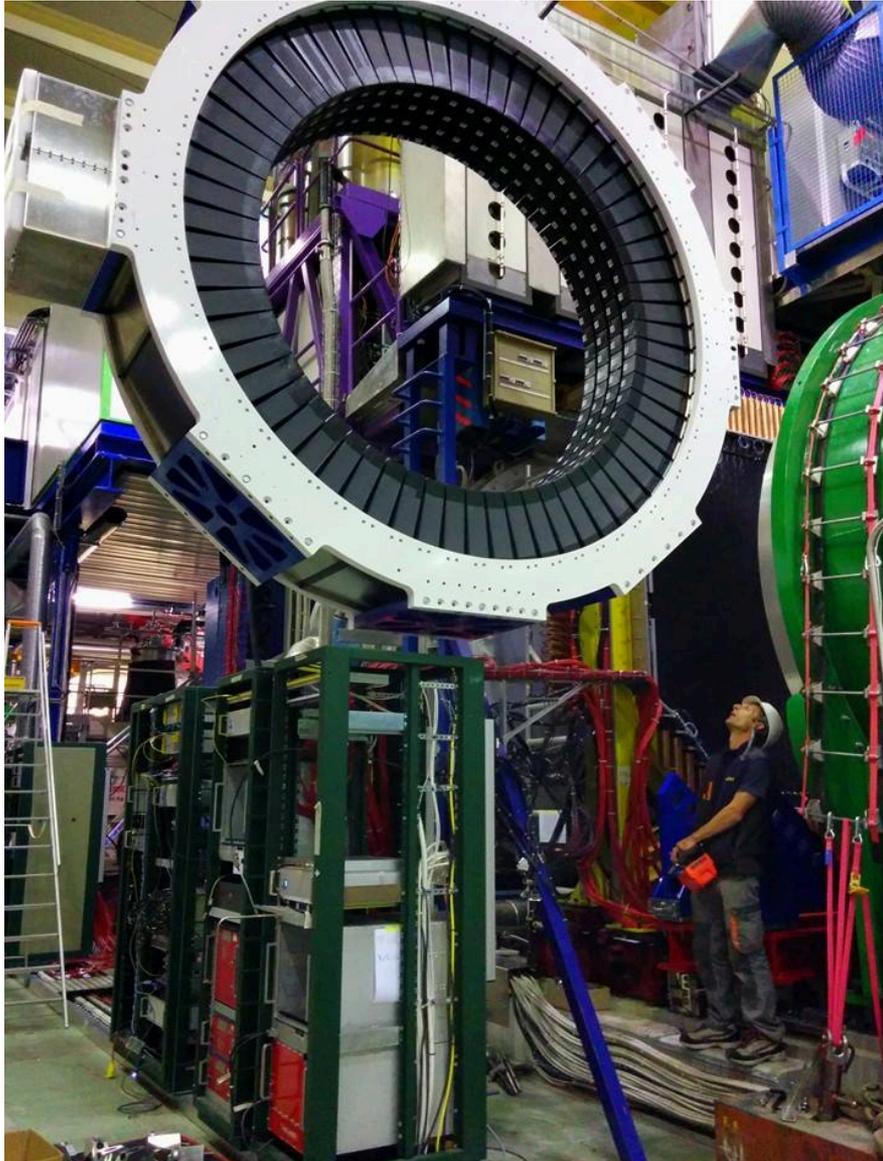
A12 placed on cradle; fine-positioning mechanisms tested

A12 transport to CERN



A12 ready to leave Frascati, 5 Aug

A12 installation



A12 installation

27 Aug: Remachined feet of A12 support in Bldg 108 workshop

- Move 4 threaded M16 holes 8 mm closer to center for each foot
- Welded threaded rod into original holes to close
- Elongate 4 unthreaded holes on each foot
- 12 hours of work in machine shop, mainly by Luca Berretta (Pisa)

28 Aug: Second attempt to install cradle went very smoothly



LAV front-end board test

Silvia Martellotti, Francesco Gonnella

Photo Veto Working Group

3 September 2014

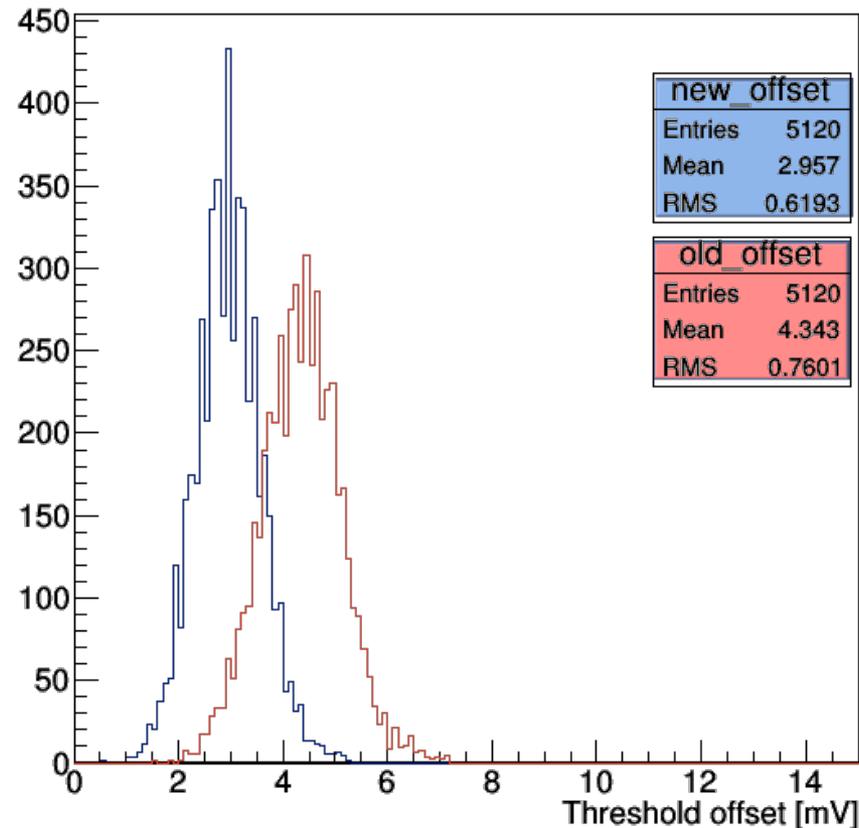
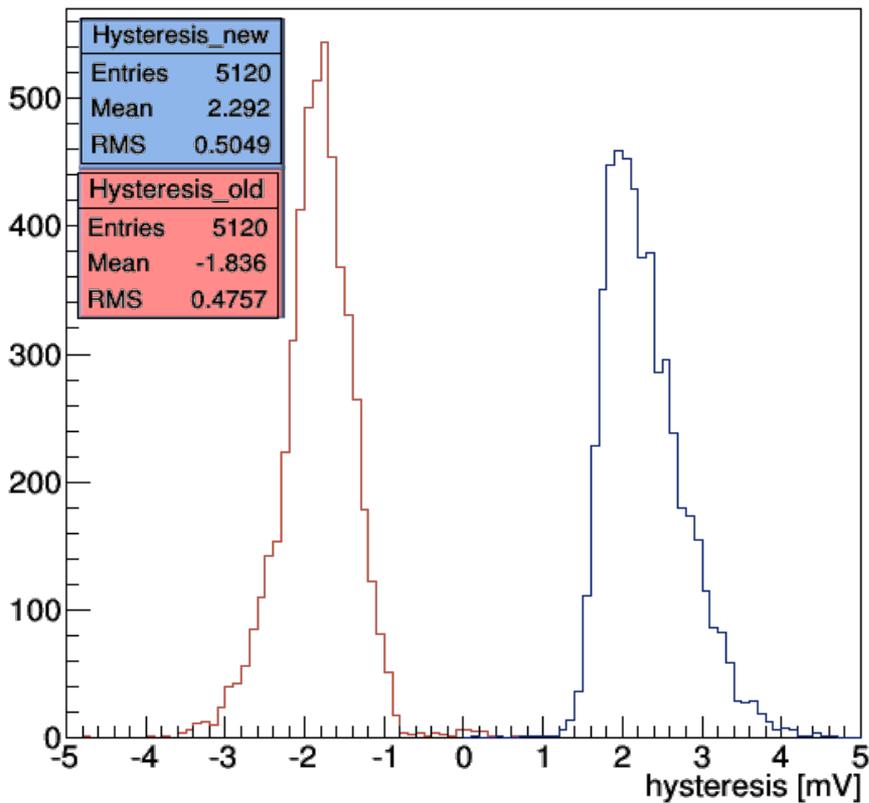


Test stand at CERN



- ▣ The LAV front-end electronic test stand has been moved to CERN to allow in situ calibration and testing of the boards
- ▣ Test of all the 86 boards have been performed at CERN by F. Gonnella, V. Kozhuharov, S. Martellotti, M. Moulson
- ▣ The facility will be also used to characterize the boards we have provided to CHOD and CHANTI

Hysteresis and threshold offset

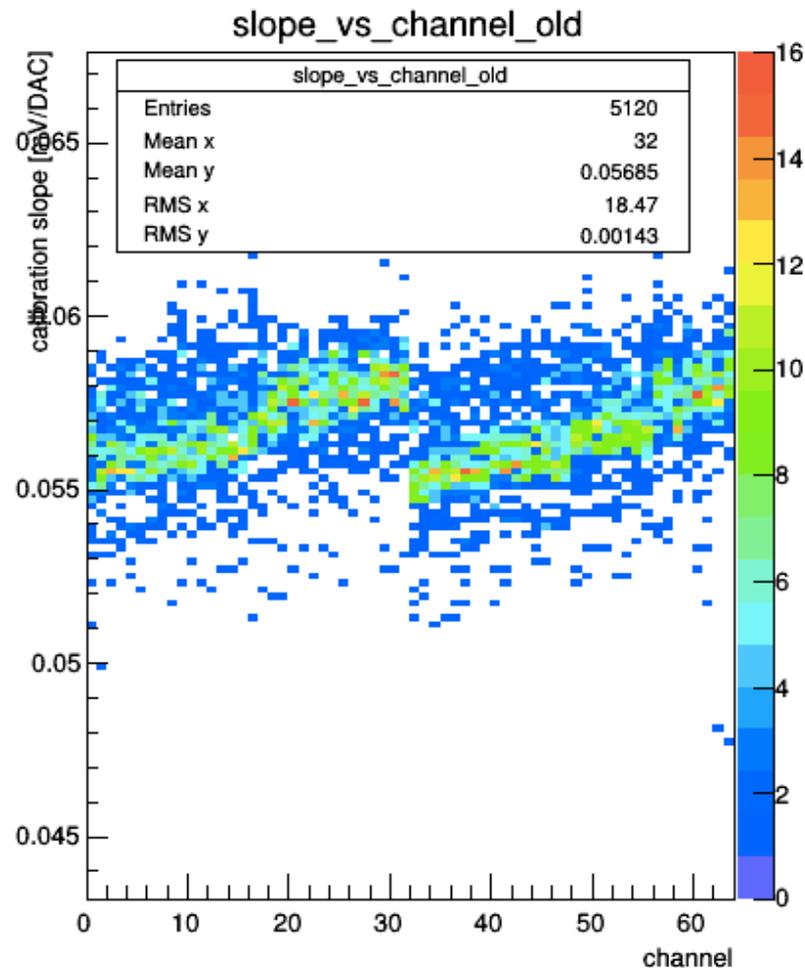
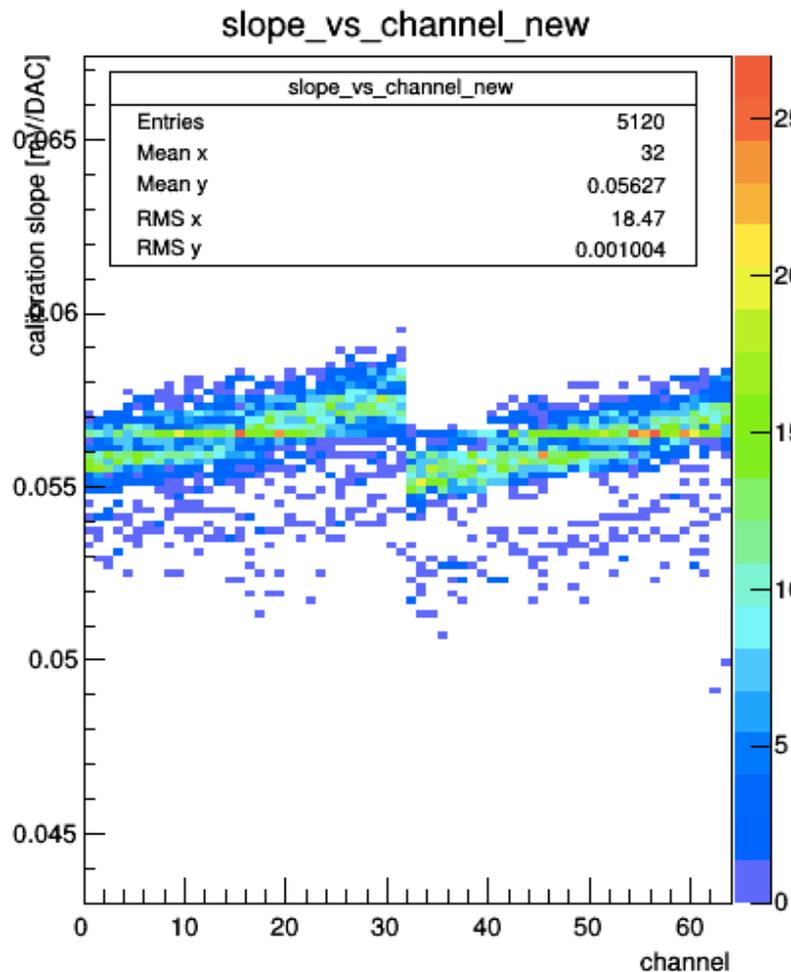


▣ The hysteresis has been correctly modified

▣ The new threshold offset is lower

▣ we gain some mV in sensitivity

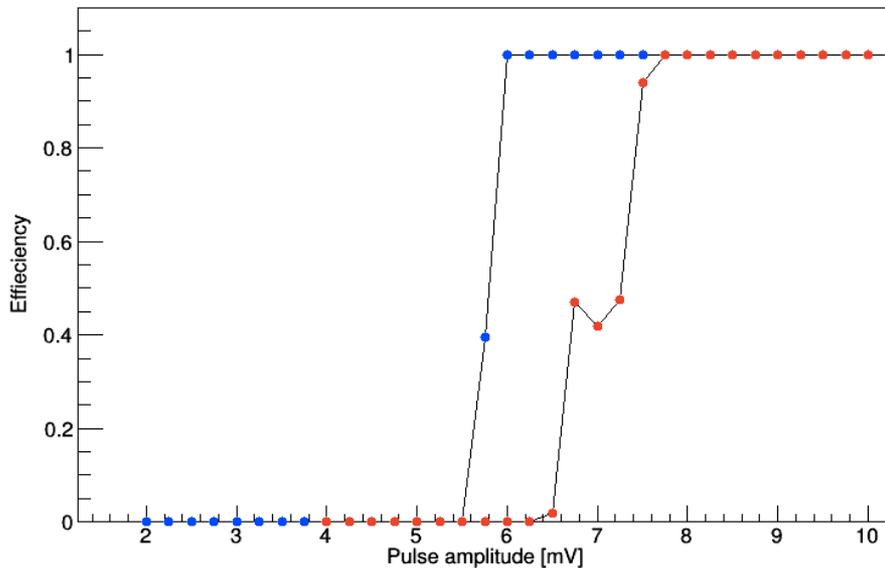
Calibration slope vs channel



- ▣ The amplification is dependent on the channel number, i.e. on the track length

Efficiency drop

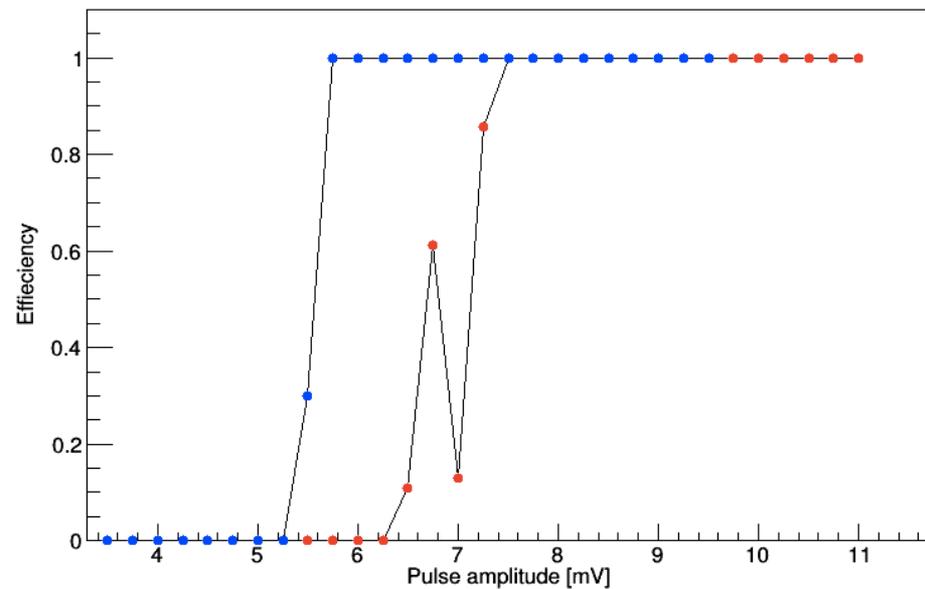
Pulse amplitude [mV] vs efficiency



- Before hysteresis modification: there were a drop in the efficiency curve for 18% of channel in leading only and 20% of channel in leading and training

- After hysteresis modification: the drop in all the efficiency curves disappeared!

Pulse amplitude [mV] vs Leading and Trailing efficiency



Conclusions

- ▣ Boards were modified, re assembled and tested in time
- ▣ We have 81/81 installed boards and 2 spares
- ▣ We will work to repair the 5 boards with some problems
- ▣ The performance is improved, not only the hysteresis:
 - ▣ Efficiency drops disappeared
 - ▣ We can now safely go down in threshold to 5 mV (even 4 if we smartly swap high and low threshold)

LAV front-end and readout status

Francesco Gonnella

Photon Veto Meeting

NA62 Collaboration Meeting

Ferrara 1-5 September 2014



LAV status summary

	Crate	PS	HV	Rasp	TEL62	Cabling	Platform	FEE	DCS
1	yes	yes	yes	yes	old	redo	-	5	ready
2	yes	yes	yes	yes	old	redo	-	5	ready
3	yes	yes	yes	yes	yes	yes	-	5	ready
4	yes	yes	yes	yes	yes	yes	-	5	ready
5	yes	yes	yes	yes	yes	yes	-	5	ready
6	yes	yes	yes	yes	yes	yes	yes	8	ready
7	yes	yes	yes	yes	yes	yes	yes	8	ready
8	yes	yes	yes	yes	no	yes	yes	8	ready
9	yes	yes	yes	yes	no	yes	no	8	ready
10	yes	yes	yes	yes	no	yes	no	8	ready
11	problem	yes	offline	yes	no	yes	yes	8	ready
12	yes	yes	offline	yes	no	no	-	8	ready

TDCB cabling is painful

- ❑ In all the crates with a new tel62 board (A3, A4, A5, A6, A7) we have connected TDCBs and LAVFEE boards.
- ❑ This is NOT an easy task, as there are plenty of noisy and dead channels.
- ❑ The situation is not stable as, apparently, problems might be solved (in lucky cases) just by “massaging” the cables...
- ❑ We managed to get rid of noisy channels in LAV3, 4, 5
- ❑ According to me, this will be a constant problem during the run, and we will be forced to mask noisy channels, that will fill up the buffers and prevent the DAQ to work properly.

LAV station	Noisy channels	Dead channels
Anti-A3	0	1
Anti-A4	0	1
Anti-A5	0	0
Anti-A6	1	?
Anti-A7	3	?

Plan for next weeks

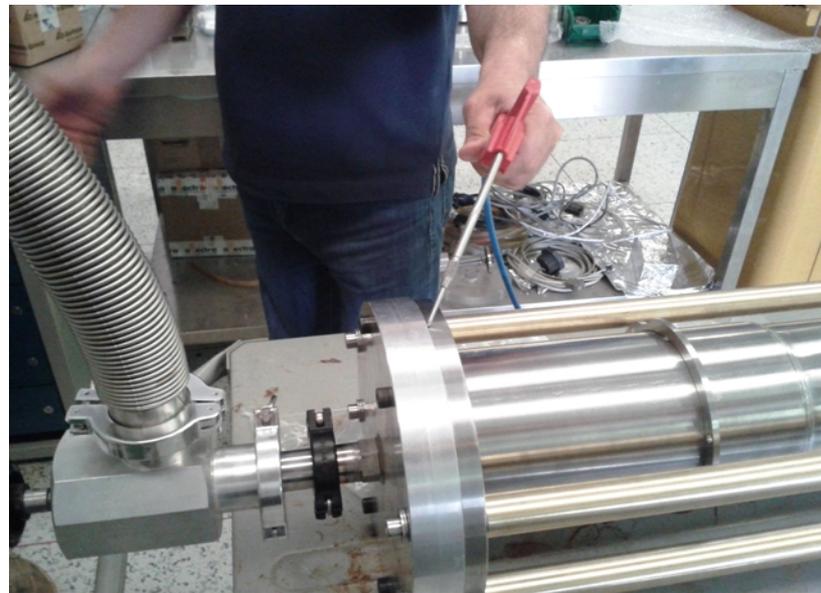
- As soon as new TEL62s arrive: installation cabling: and dead/noisy channel hunting
- Upgrade the fw in all LAVFEE and prepare DCS calibration files with Raspberry Pis
- Cosmic data taking using as many stations as possible should be done and analysed before the run
 - Need to do Ethernet Cabling: 5 ~4m-cables per station
 - Setup and test self-trigger or use Torino L0TP

SAC and IRC status

Venelin Kozhuharov
for the SAC/IRC working group

Photon veto WG meeting
3.09.2014

IRC tube certification



$< 10^{-9}$ mbar.l/s with He
leak detector

18 hours @ 1.5 bar

$$P_{\text{start}} = 10^{-2} \text{ mbar}$$

$$P_{\text{end}} = 0.5 \text{ mbar}$$

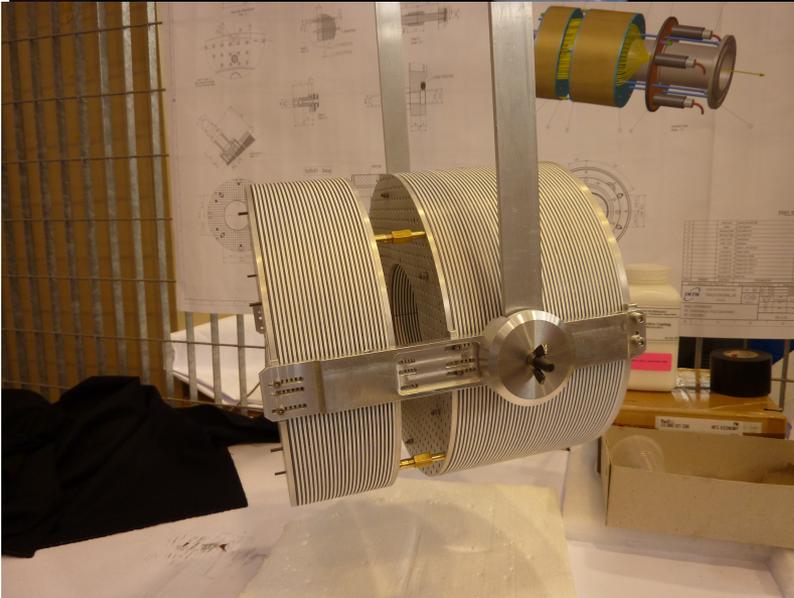
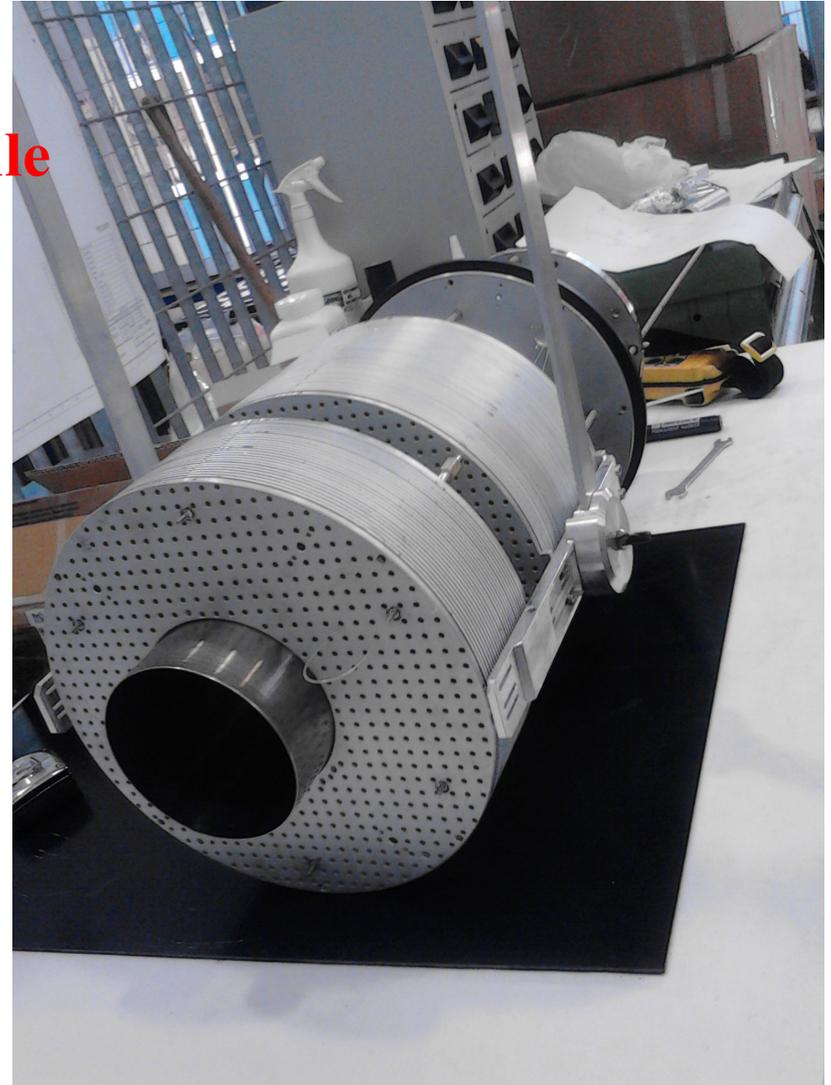
No visible damage to the tube, no high pressure degradation

<https://edms.cern.ch/document/1398122>

Modules assembly



DS module



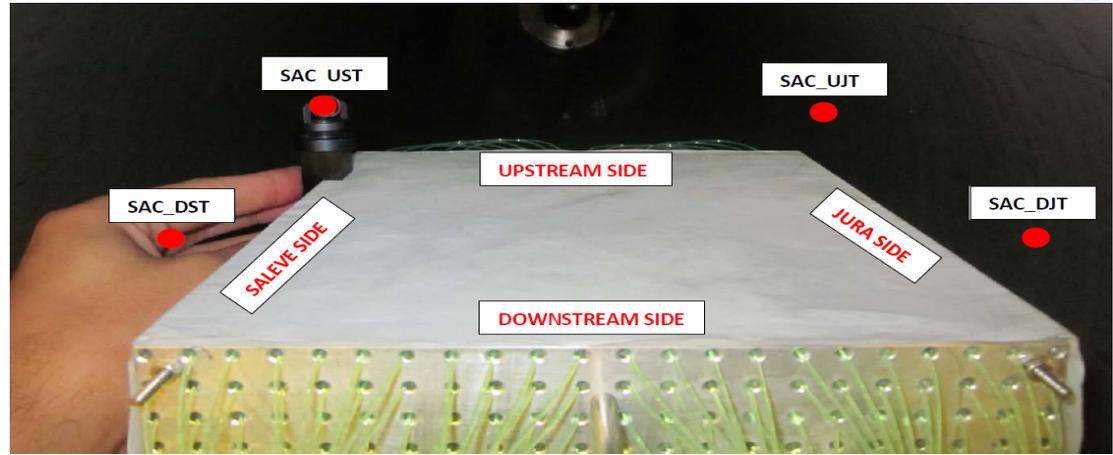
IRC assembly



Part of the team :)



SAC survey



Points on the top of the SAC detector in m		
	X	Y
SAC_DJT	0.1074	0.1371
SAC_UJT	0.1030	0.1372
SAC_UST	-0.1021	0.1380
SAC_DST	-0.0983	0.1378

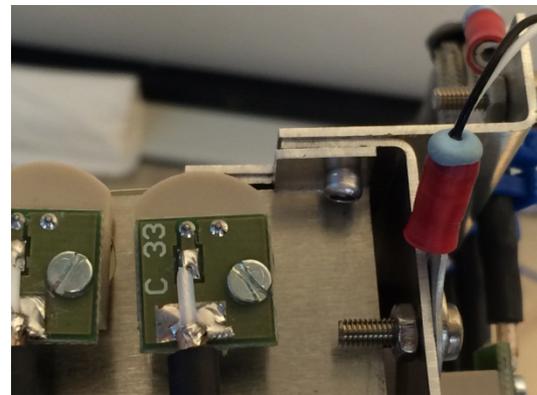
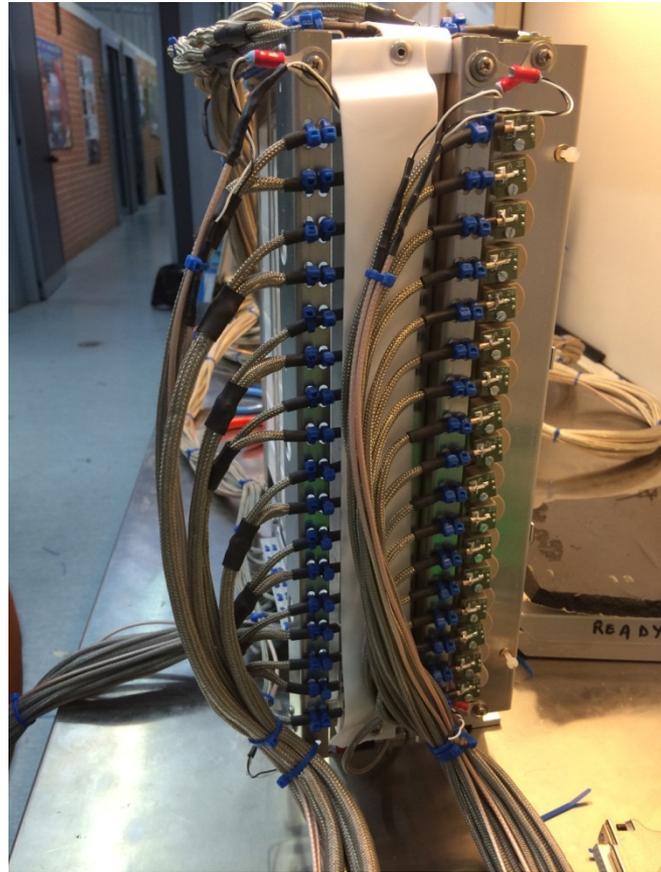
- Nominal upstream: ± 0.1025 m for X and $0.1025_{\text{det}} + 0.0350_{\text{target}} = 0.1375$ m for Y
- Rotation angle: 23mrad (minimal necessary: 15 mrad)

- IRC assembly completed and the detector is ready for installation
 - **Work to be done after installation**
 - Wrapping of the active part
 - PMT installation, cabling, HV sources to be chosen
 - Final checks on the detector: light tightness, cosmics
- SAC was positioned with 0.5% precision in X,Y; rotation angle of 23 mrad
- DAQ system installation in progress
 - Implementation in the central NA62 TDAQ ongoing
 - Communication to RunControl and PCfarm tested and verified
 - Connection to RO PC: USB at the moment, no optical connection
 - Firmware missing on GANDALF:
 - circular buffer for event storage until L0
 - zero suppression, event formatting and custom packing
 - In addition: optical data transmission to the RO PC once modules arrive
- Still a lot of work on the DAQ side ... manpower

CHANTI update

F. Ambrosino, T. Capussela, D. Di
Filippo, P. Massarotti, M. Mirra, M.
Napolitano, L. Roscilli, G. Saracino

CHANTI Construction



- All of the six stations have been fully assembled and cabled in Napoli
- All of the 300 SiPMs have been tested for functionality. A subset (25%) tested at different temperatures to compare temperature behaviour wrt Hamamatsu specs
- All of the connections with SiPMs and Pt100 probes checked before assembly

CHANTI Installation

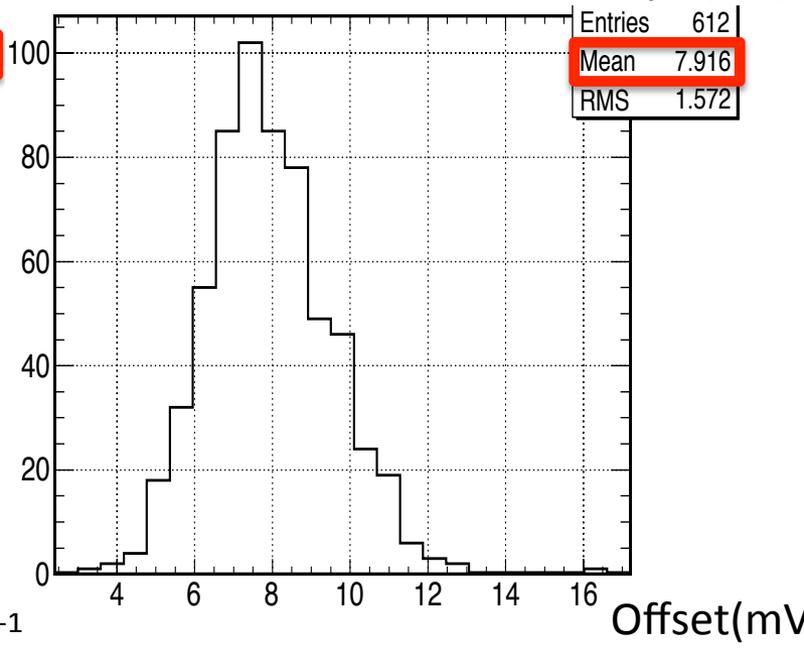
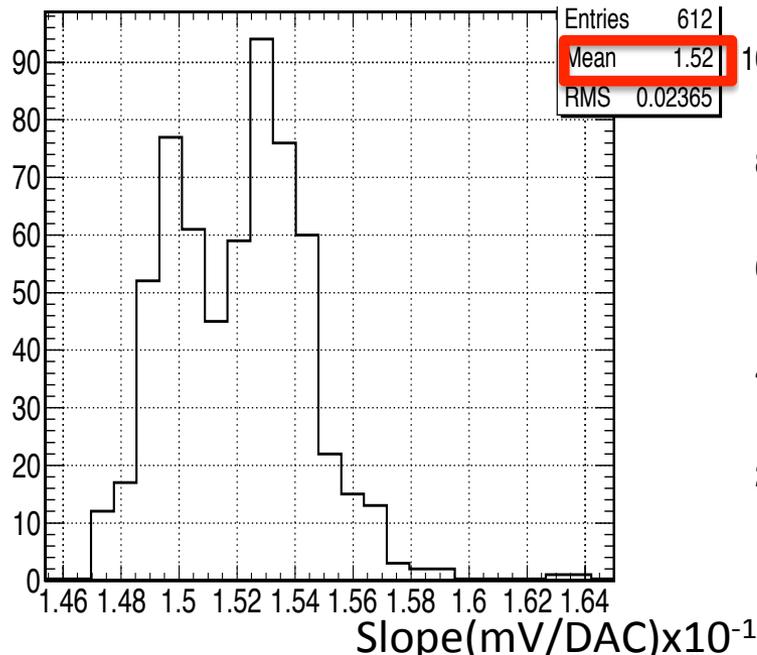
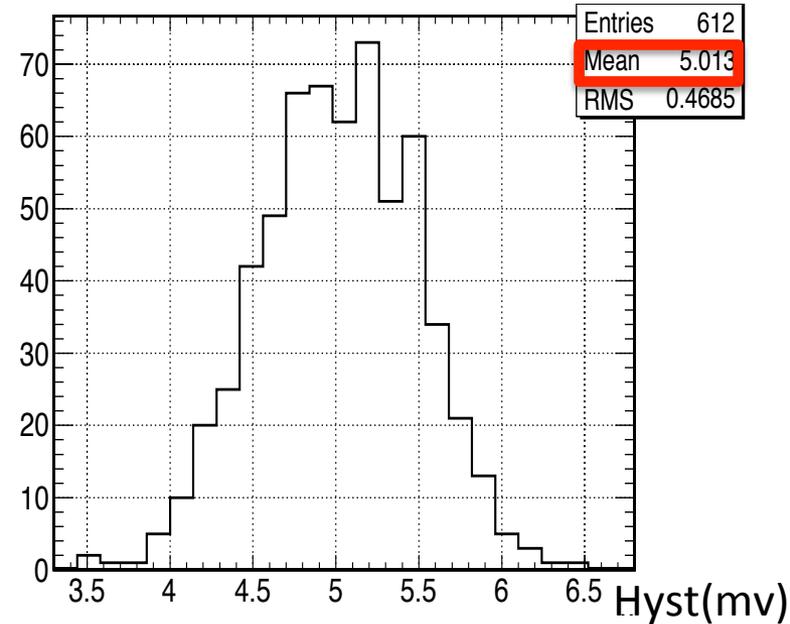


- CHANTI stations aligned in Napoli to $\pm 0,5$ mm. The last CHANTI station has adjustable feet to this aim.
- Check of alignment re-done at CERN after transportation.
- Installation on the beam line and survey successful. Typical deviation of targets from nominal position is 0,1 mm

CHANTI ToT boards test results

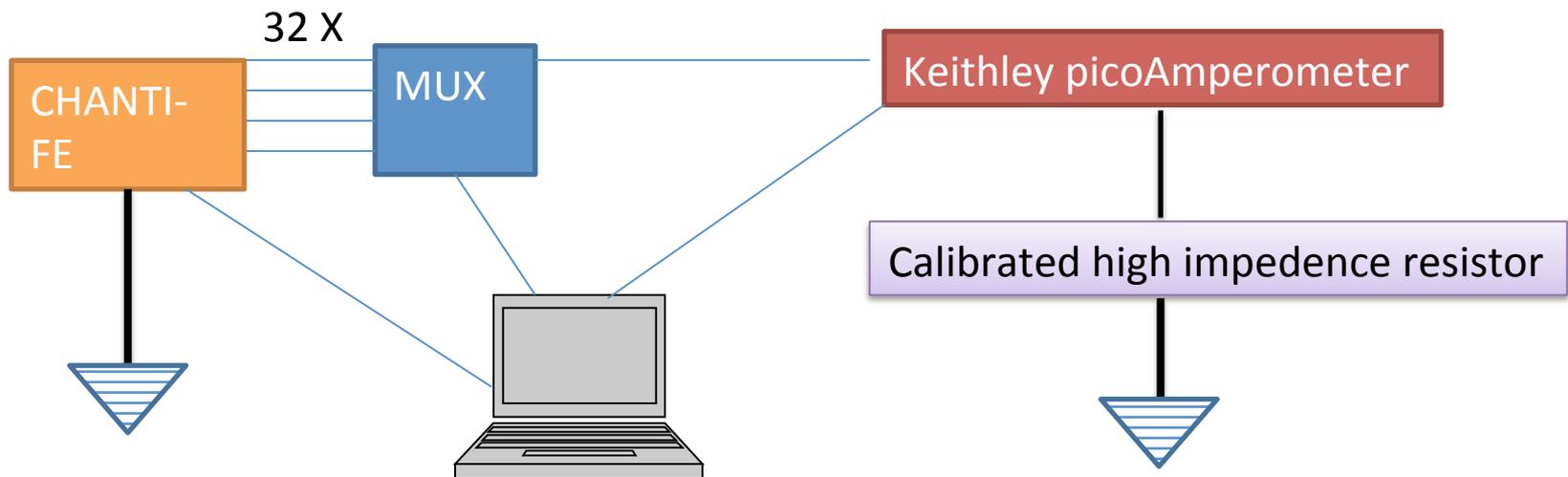
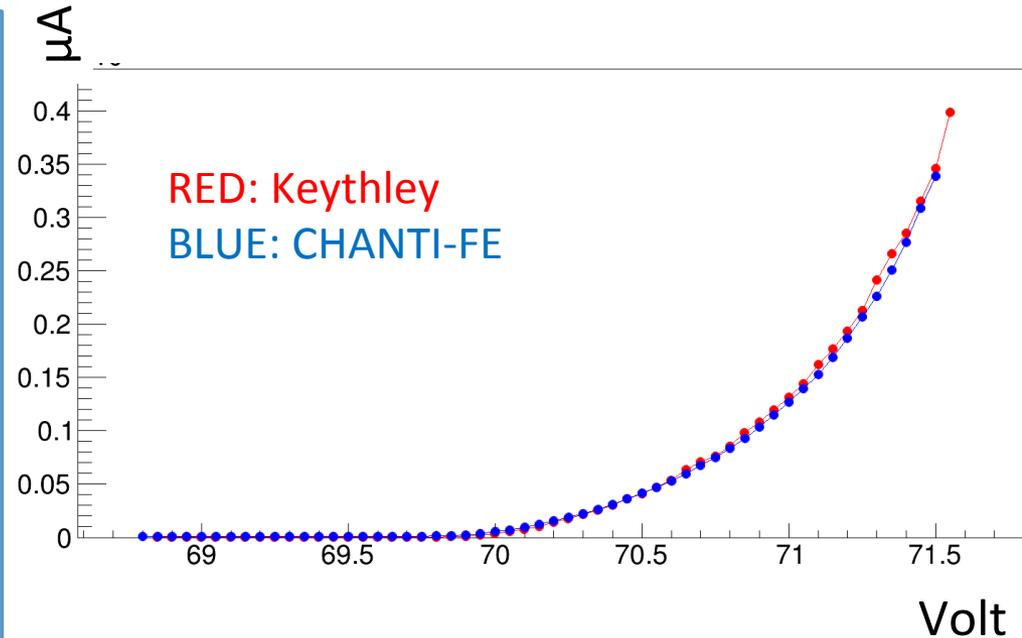
All the 160 CHANTI-TOT mezzanines, corresponding to 640 channels, have been tested.

Hysteresis, gain and offset are within expectations.



CHANTI-FE CALIBRATION

All channels of all CHANTI-FE boards calibrated using a picoAmperometer and a calibrated high impedance resistor . Both the **DAC voltage** value (read and set by CHANTI-FE) and the **DAC current** value (read by CHANTI-FE) are calibrated this way. Calibration checked by comparing SiPMs I-V curves measured with Keythley device (used as source meter) and CHANTI-FE.



CHANTI DCS

Slow control status

Low level DCS ready:

- Standard panels for the wiener crates
- ToT board are the same of the LAV so we can use the same panels to power up and setup threshold and monitor board status
- Chanti FE software ready: channel power up, bias voltage setting, calibration constant loading. The full chain was tested with one board on the can bus.

Now we can start working on the “High” level DCS: state machine, etc.

No integration in general fw up to November (at least...).

Also alternative /backup solution based on raspberry pi is under consideration

SiPM monitoring panel

Channel	Setup	Actual	Req	VSet,V	VMon,V	IMon,uA
1	On/Set Off	OFF ON	40.0	0.0	0.00	
2	On/Set Off	OFF ON	0.0	0.0	0.00	
3	On/Set Off	OFF ON	0.0	0.0	0.00	
4	On/Set Off	OFF ON	0.0	0.0	0.00	
5	On/Set Off	OFF ON	0.0	0.0	0.00	
6	On/Set Off	OFF ON	0.0	0.0	0.00	
7	On/Set Off	OFF ON	0.0	0.0	0.00	
8	On/Set Off	OFF ON	0.0	0.0	0.00	
9	On/Set Off	OFF ON	0.0	0.0	0.00	
10	On/Set Off	OFF ON	0.0	0.0	0.00	
11	On/Set Off	OFF ON	0.0	0.0	0.00	
12	On/Set Off	OFF ON	0.0	0.0	0.00	
13	On/Set Off	OFF ON	0.0	0.0	0.00	
14	On/Set Off	OFF ON	0.0	0.0	0.00	
15	On/Set Off	OFF ON	0.0	0.0	0.00	
16	On/Set Off	OFF ON	0.0	0.0	0.00	

Channel	Setup	Actual	Req	VSet,V	VMon,V	IMon,uA
17	On/Set Off	OFF ON	0.0	0.0	0.00	
18	On/Set Off	OFF ON	0.0	0.0	0.00	

Board information section

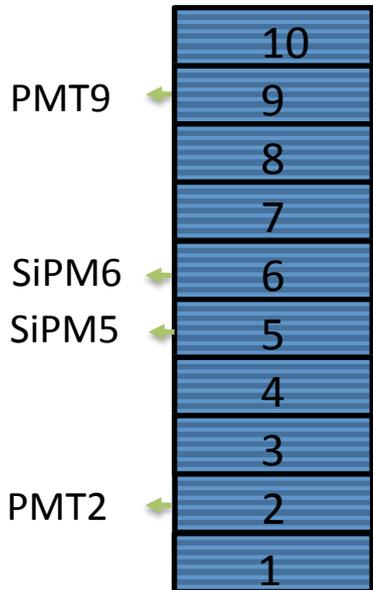
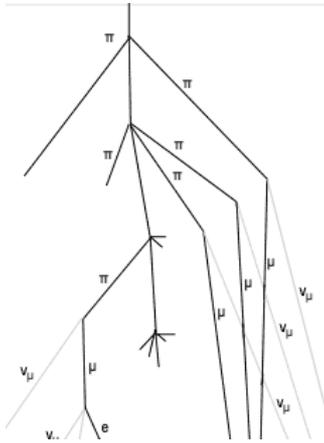
SiPM monitoring and Voltage setting

It was developed also a panel/script to load calibration constant file

New panel version contains measurement units and split the “Switch” panel in two (“On” and “Off” panels).

HASC readout evaluation with cosmic rays

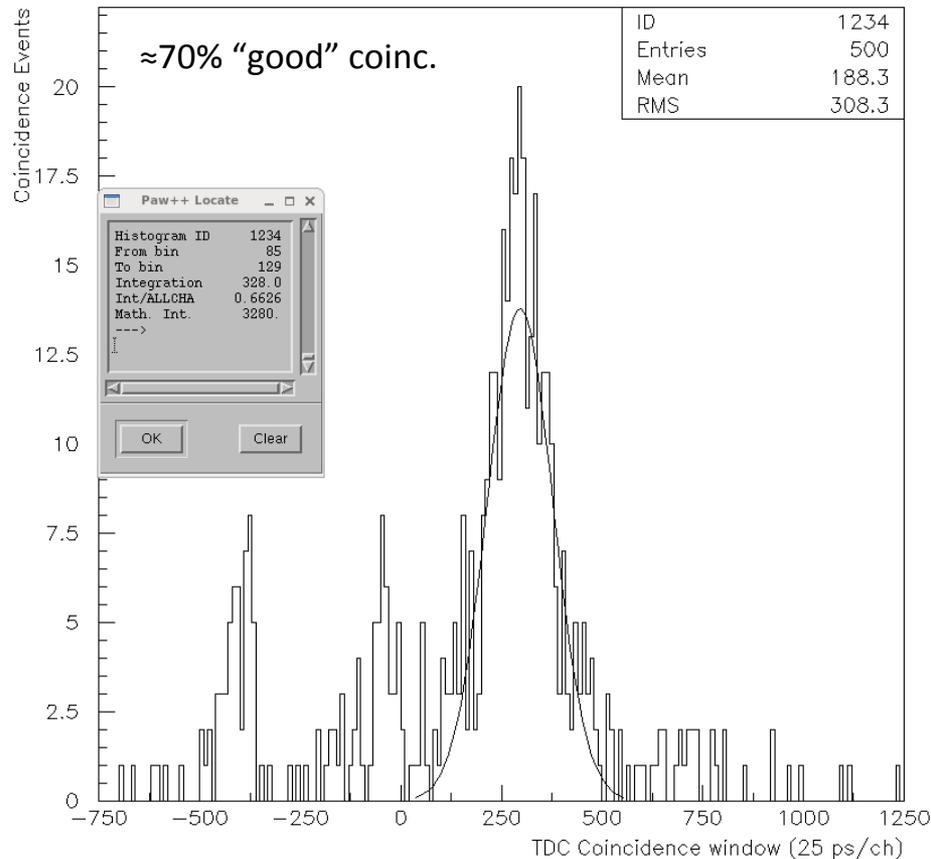
The setup



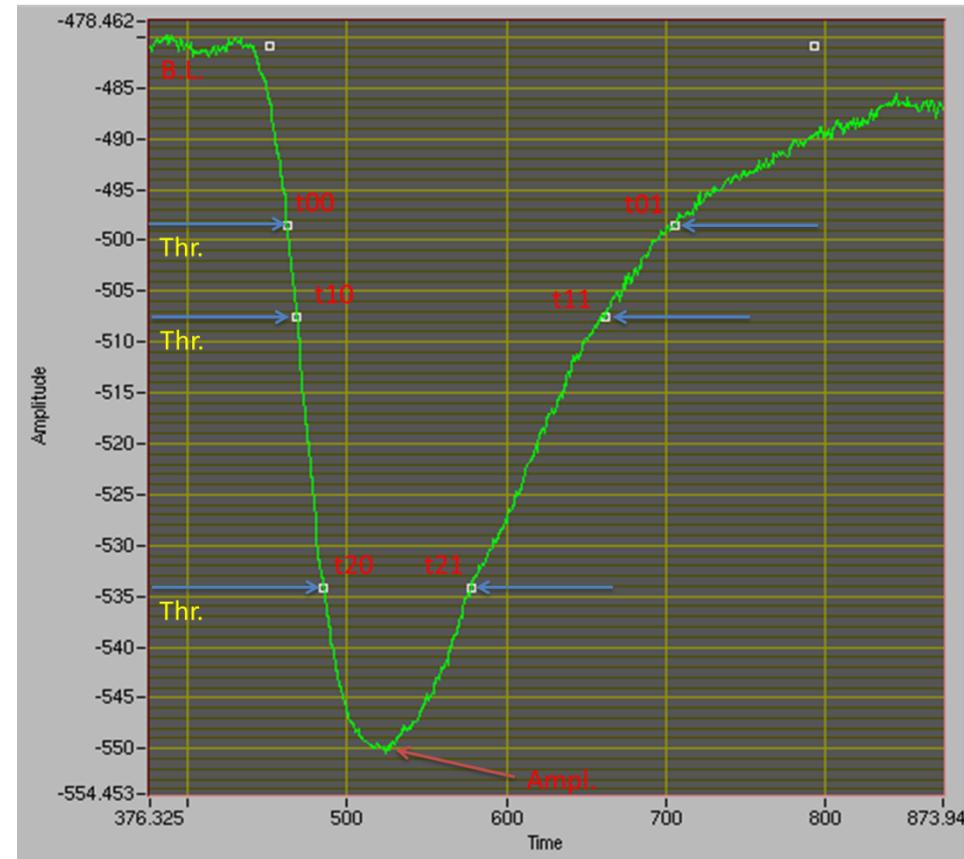
The data taking

Run length: 500 events (about 1 coincidence/ 100 sec.)

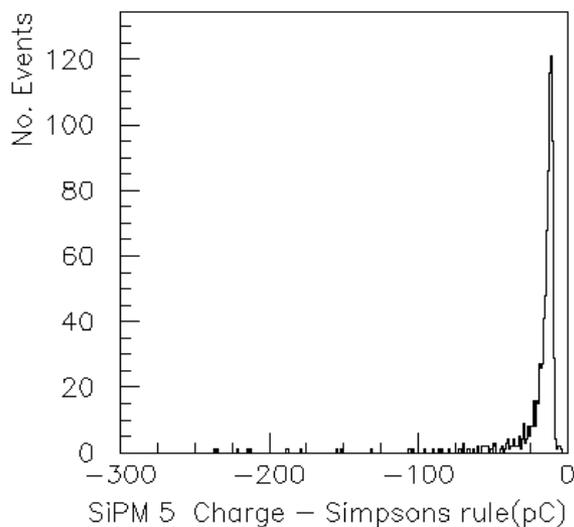
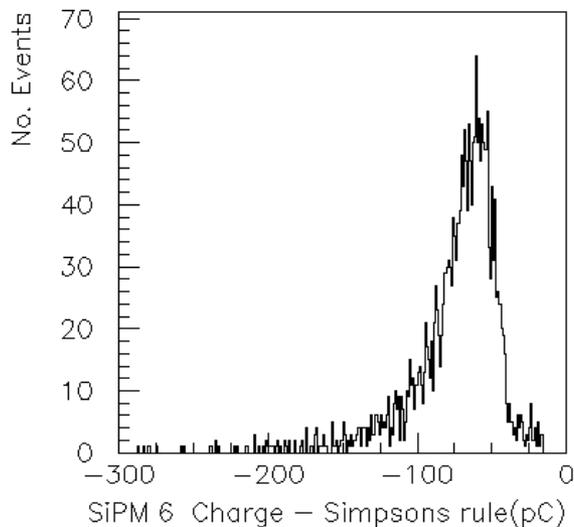
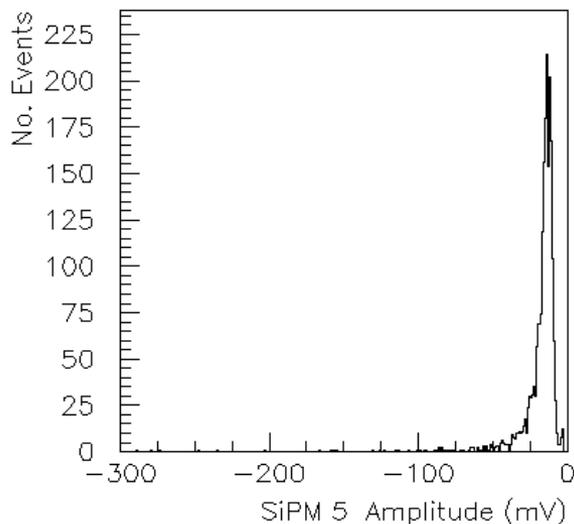
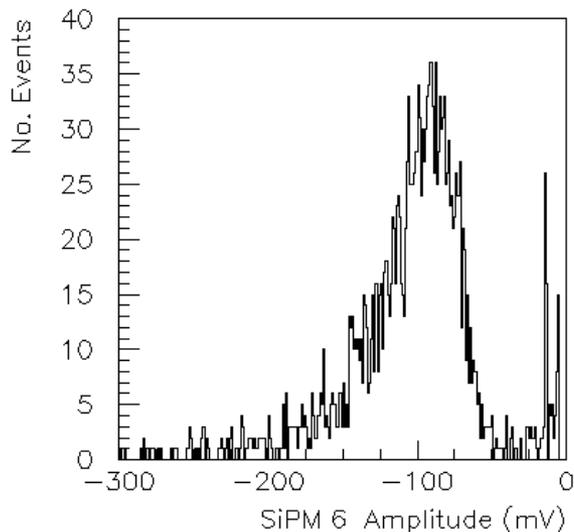
2 data files/run : TDC data, Digitizer waveforms – for off-line Digital Pulse Processing (DPP)



Custom DPP code: Pk. detect, TOT, Timing, Integration ...



DPP of SiPM signal: Amplitude, Charge integration



Amplifier & Bias boards:
SiPM 6 - $G \approx 30$ (Diego T.)
SiPM 5 - $G \approx 6$ (1st guess)

DPP results for m.i.p.

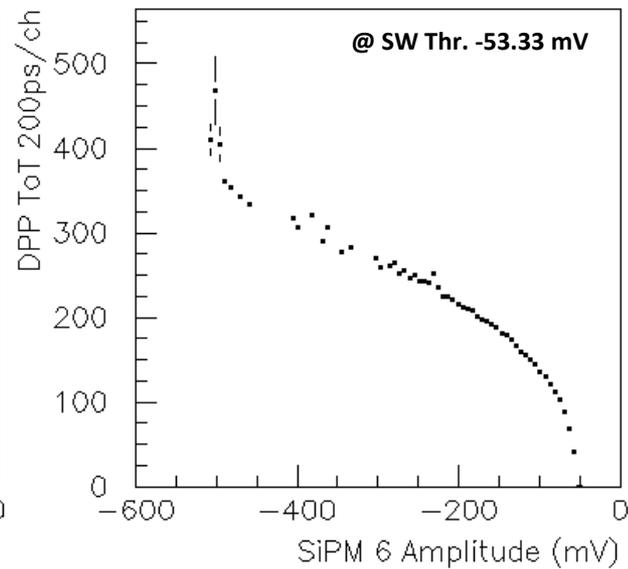
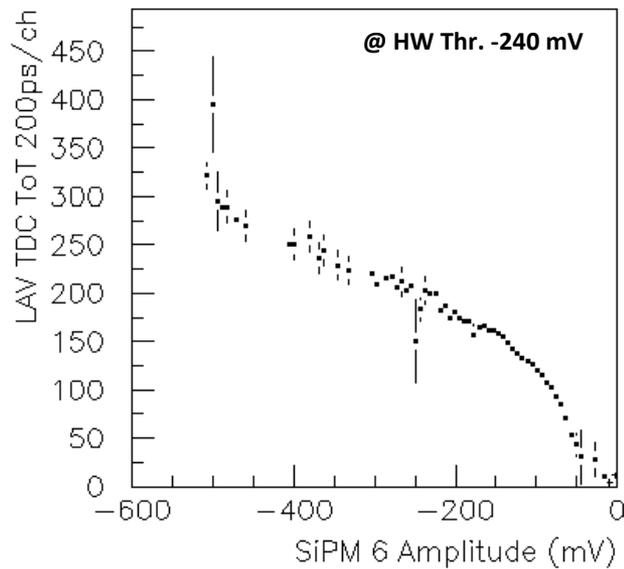
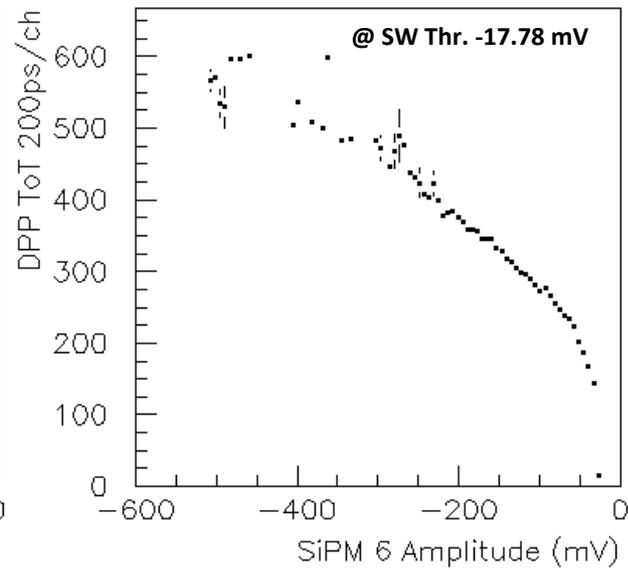
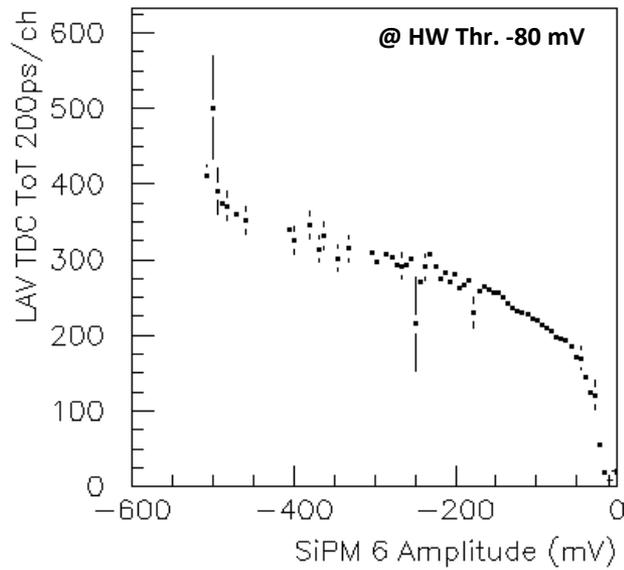
SiPM 5:
Amplitude: 90 mV
Charge: 65 pC

SiPM 6:
Amplitude: 13 mV
Charge: 10 pC

Note

- Attenuation $\approx 1.5/\text{ch.}$ due to delay cables between FIFO and Digitizer;

SiPM 6 - LAV ToT (TDC) vs. SiPM Amplitude (DPP)



HASC range scenario

M.C. Range: 5 MeV (m.i.p.) - 500MeV (pions)

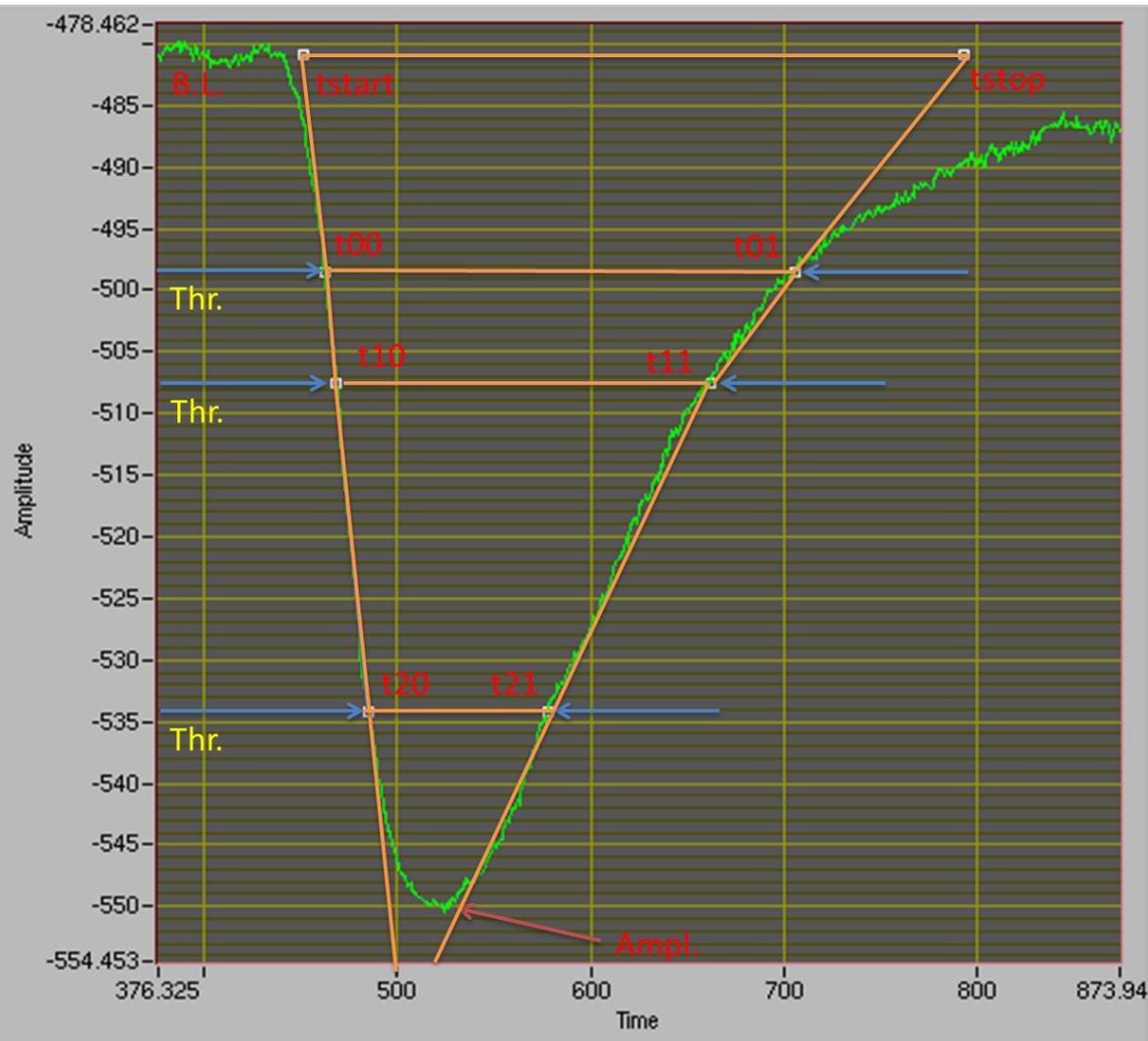
SiPM Readout Amplifier Range : 10 mV (m.i.p.) - 1000 mV (pions)

The $G \approx 6$ amplifier might fit but a $G \approx 4$ is safer

The wish: use LAV ToT board and find **a linear function to “reconstruct “ the charge**

First idea: use a **combination of HW ToT’s**

DPP of SiPM signal: Charge integration with geom. arrays



Thr 1. passed:

Charge = Array (1 Trapezoid + 1 Triangle);

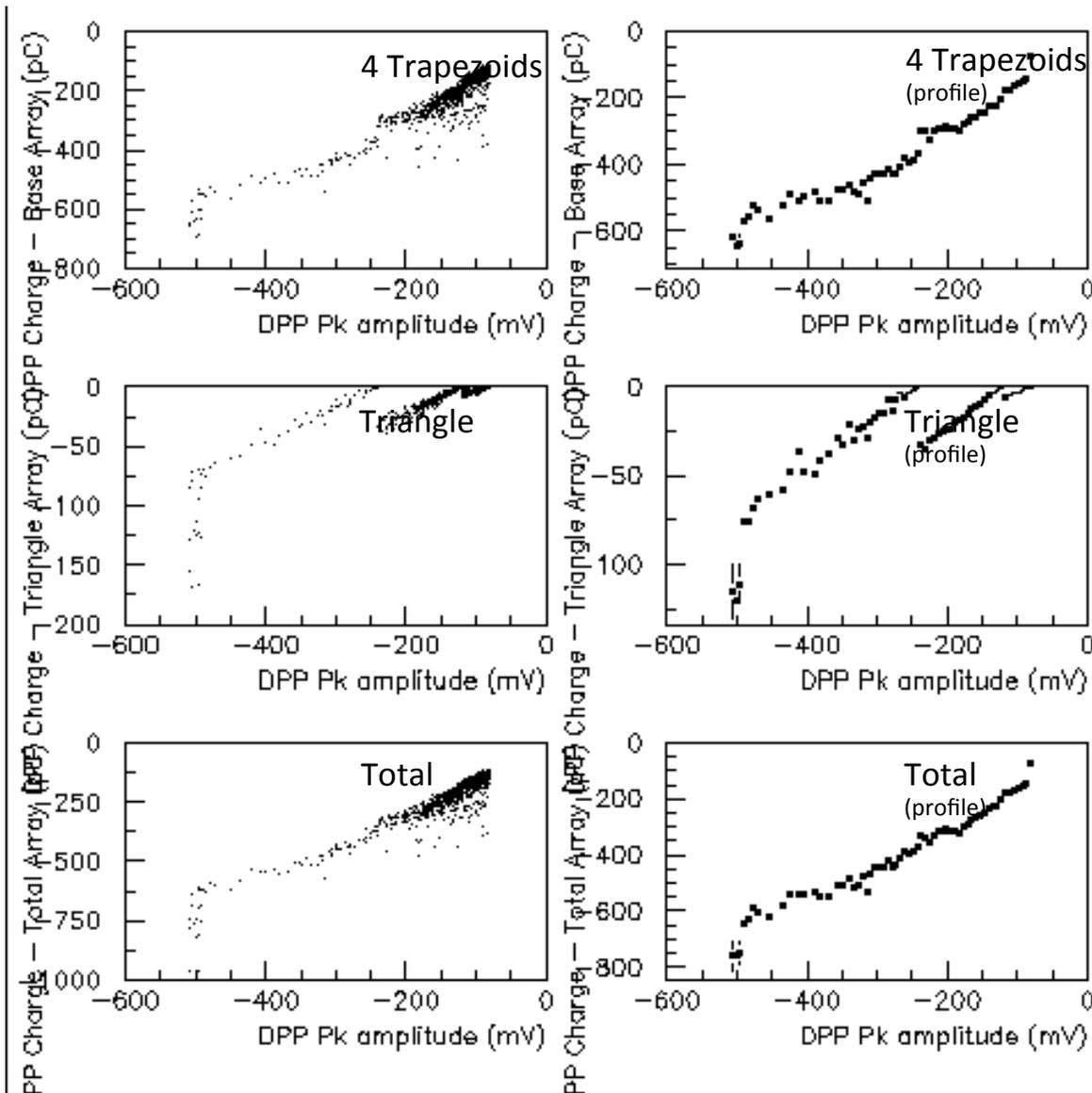
Thr 2. passed:

Charge = Array (2 Trapezoid + 1 Triangle).

To extend the linearity a 3rd and 4th threshold can be added.

Note: Picture depicts the method for 3 Thresholds

DPP Charge integration with geom. arrays



DPP @ SW Thrs.

- 10 mV
- 80 mV
- 120 mV
- 240 mV

Passing to the LAV ToT TDC data I realized that the Thr. Comparator is after the Gain 3 amplifier ... ☹

and the corresponding thresholds are 4.5 lower (1.5 X 3, Cable Atten. X ToT on-board Gain):

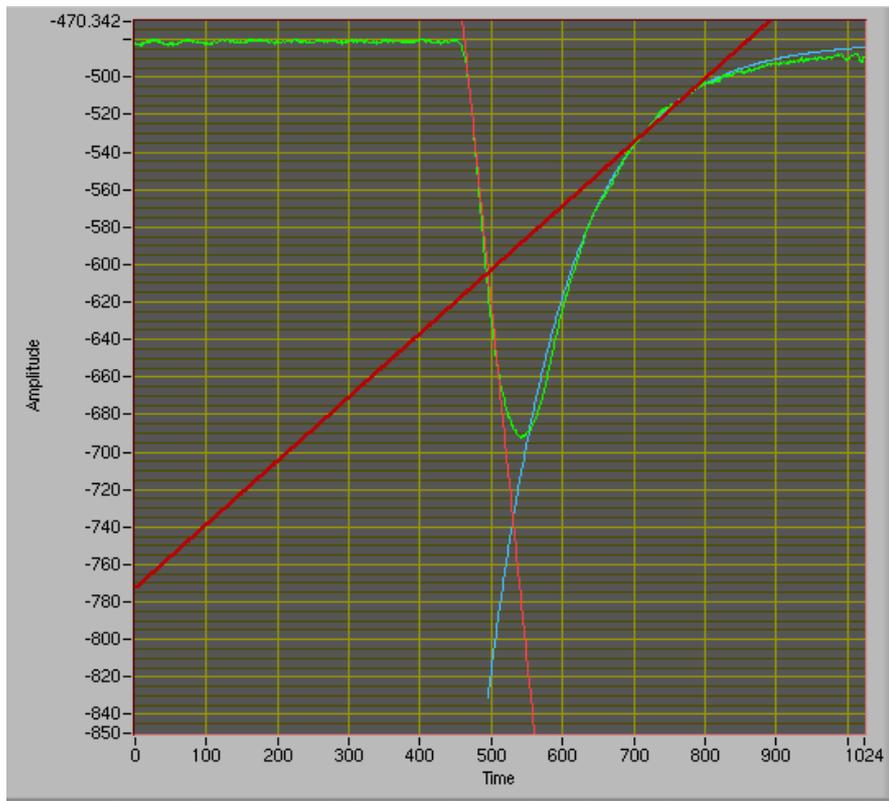
New DPP @ SW Thrs.

- 2.22 mV
- 17.78 mV
- 26.67 mV
- 53.33 mV

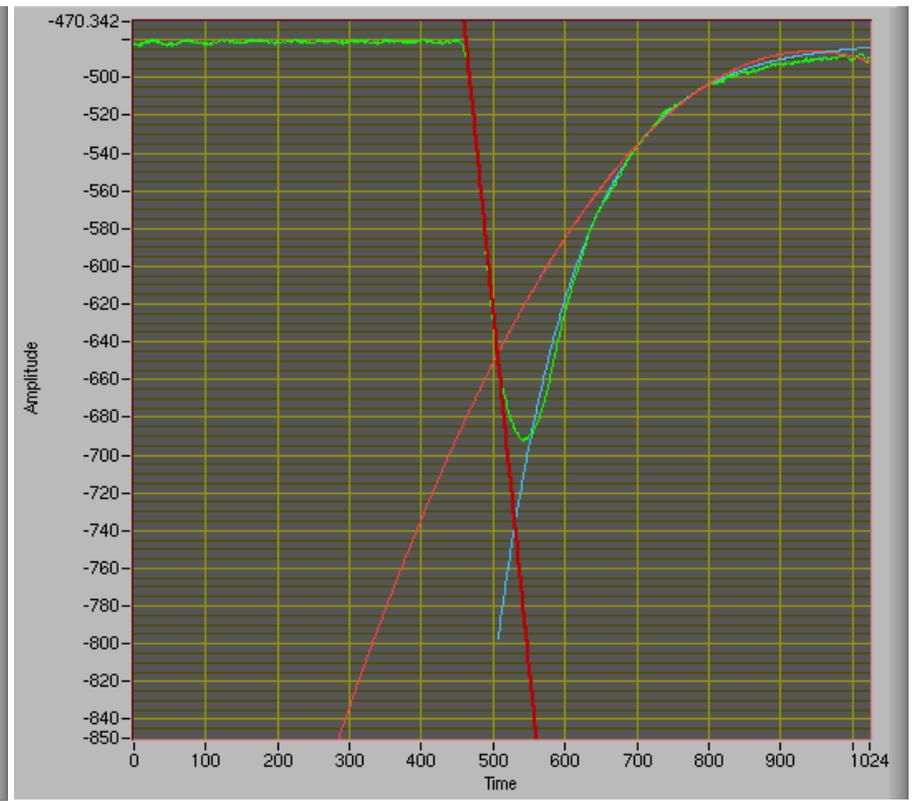
DPP of SiPM signal: Charge integration with analytical function's

Method: the signal rise is approximated as linear and the tail an exponential with fixed decay ct.

DPP: line (lead) + exp. Decay (trail)

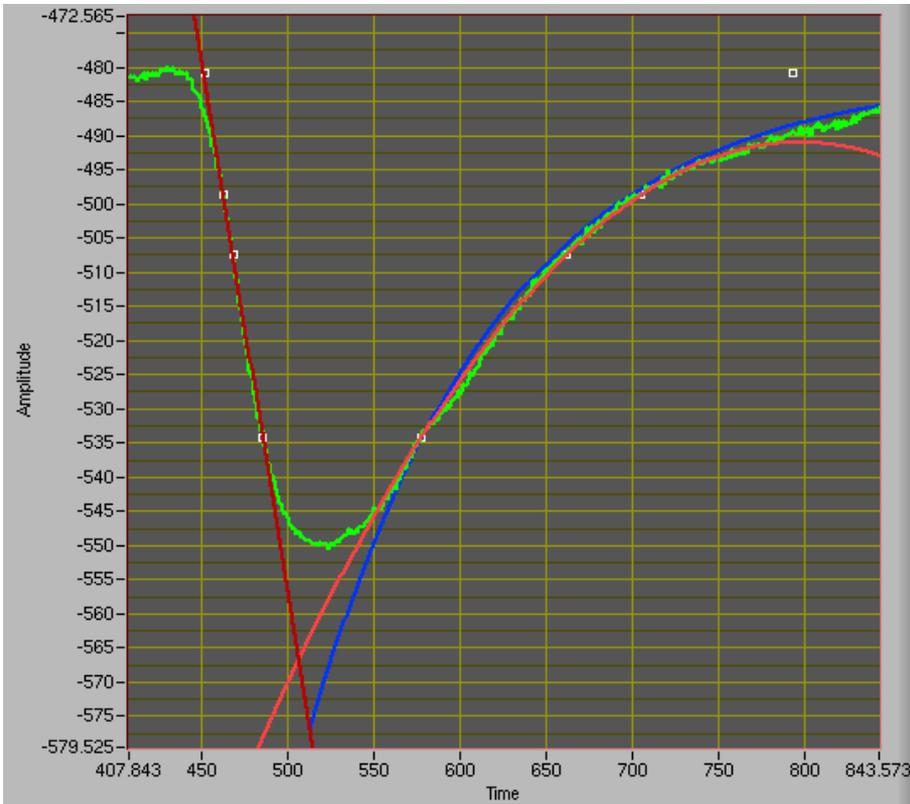


DPP: line (lead) + exp. Decay (trail)

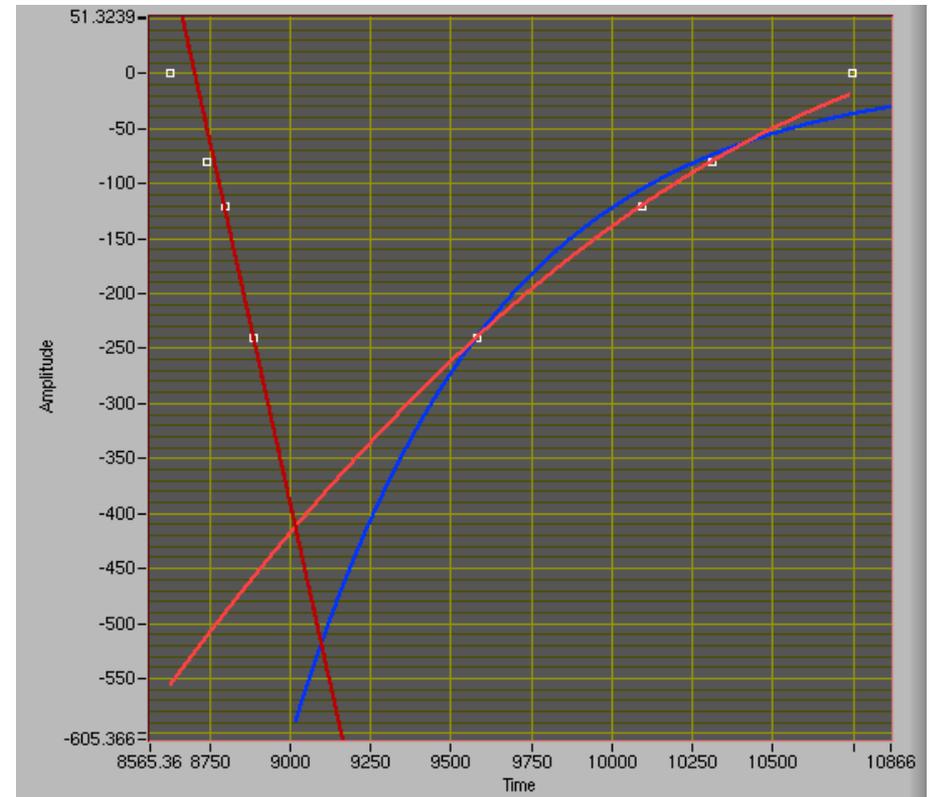


Charge integration with analytical function's: DPP vs HW ToT TDC

DPP: line (lead) + exp. Decay (trail)

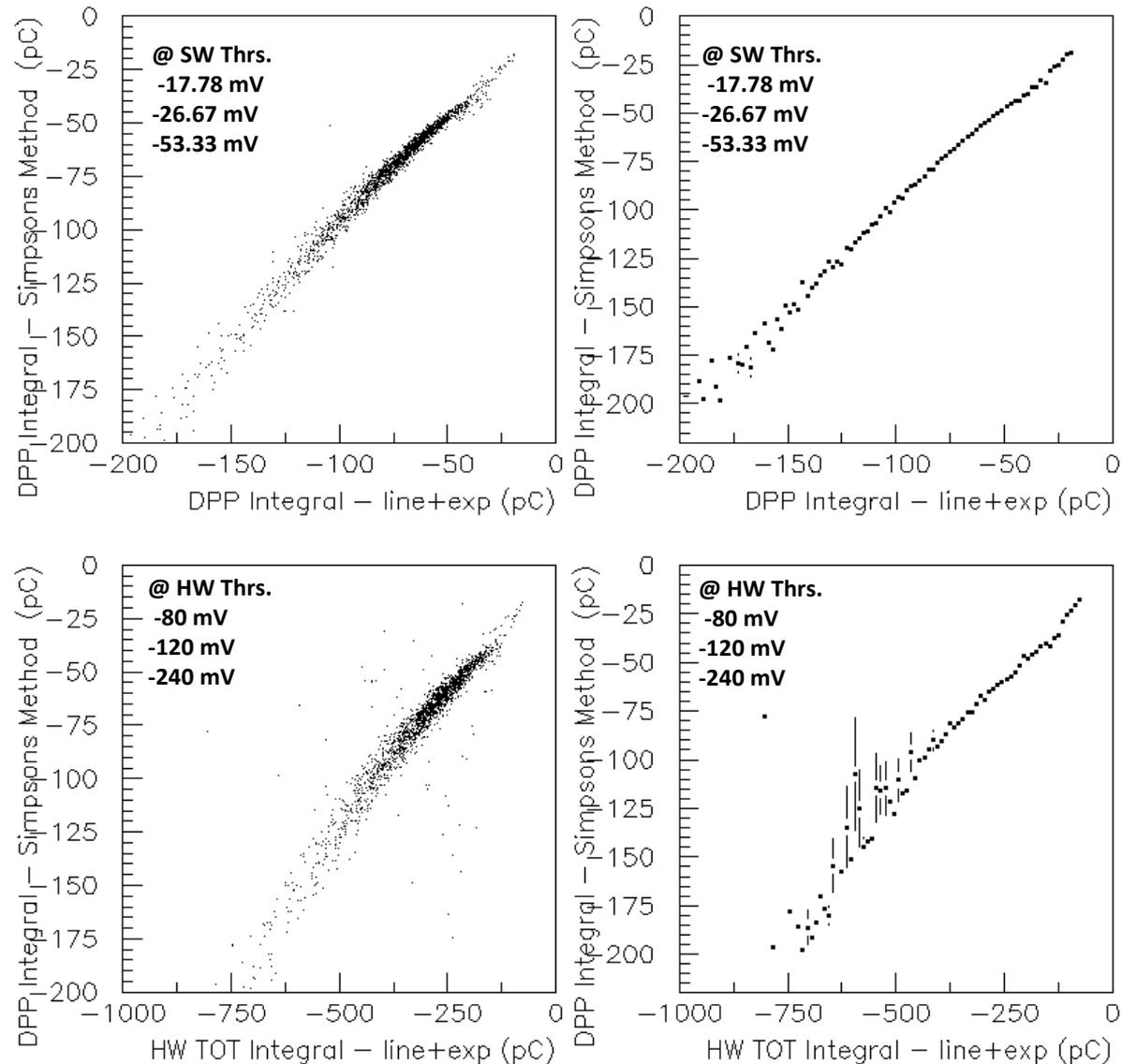


HW ToT TDC: line (lead) + exp. Decay (trail)



Charge integration with analytical function's: DPP vs HW ToT TDC

- SiPM 6 -



Remarks

Both analytical and geometrical charge integration methods delivers promising results.

The existing DPP code can be implemented in a TEL62 FPGA.

In order to achieve the linearity on the 5 MeV-500 MeV range we:

- most likely, need to use a modified LAV ToT mezzanine with NO gain on-board ;
- need to use, at least, 3 HW ToT / SiPM channel.

Congratulations to the entire working group
on detector systems completed and installed:

LAV, SAC, IRC, CHANTI

The LAV system was a particularly ambitious project.
Congratulations to all of the groups involved:

Frascati, Pisa, Naples, Rome 1

and especially to our designers and technicians:

S. Bianucci (PI), L. Berretta (PI), G. Bisogni (LNF), F. Cassese (NA),
E. Capitolo (LNF), C. Capoccia (LNF), A. Cecchetti (LNF),
G. Corradi (LNF), R. Lenci (LNF), V. Lollo (LNF), C. Paglia (LNF),
E. Paoletti (LNF), F. Pellegrino (RM1), G. Petragnani (PI),
F. Raffaelli (PI), L. Roscilli (NA), V. Russo (LNF), M. Santoni (LNF),
D. Tagnani (LNF), S. Valeri (LNF), T. Vassilieva (LNF)