Tel62
Radiation Tests

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Radiation Tests

- Motivations:
  - KTAG readout system needs to stand a high radiation level,

  ensuring stable and reliable operations over time.
- Goals:
  - Perform radiation tests of the NA62 integrated trigger and DAQ board;
- Strategy:
  - testing radiation-induced single event effects, total ionization dose

  and displacement effects;
- Location:
  - ISIS Neutron and Muon Source at STFC Rutherford Appleton Laboratory;
- Timescale:
  - Phase I: test TellOne board with muon beam (9-12/12/2013) done ✔
  - Phase II: test Tel62 board with muon beam (26-29/03/2014) done ✔
  - Phase III: test Tel62 board with neutron beam (28-30/07/2014) this talk ✔

Motivations - Muons

CEDAR Radiation Summary

Evgueni's talk at CEDAR WG Meeting on 30/3/2011

Summary

neutrons

- According to the FLUKA simulations, the expected neutron dose is ~0.04 Gy/year behind 160cm of concrete shielding, and ~0.4 Gy/year without such shielding.

muons

- According to the HALO simulations, the expected muon dose close to the Jura wall (x>4m) is 0.2-0.4 Gy/year.

ELECTRONICS DAMAGE: are neutrons more dangerous than muons?

neutrons + muons

EVGUENI'S ESTIMATION for the CEDAR RADIATION LEVEL:

PreAmp + NINO	~ **0.2-0.5** Gy/year
TEL62 **without** concrete shielding	~ **0.5-0.7** Gy/year
TEL62 **with** additional concrete shielding	~ **0.2-0.5** Gy/year

Further shielding available?

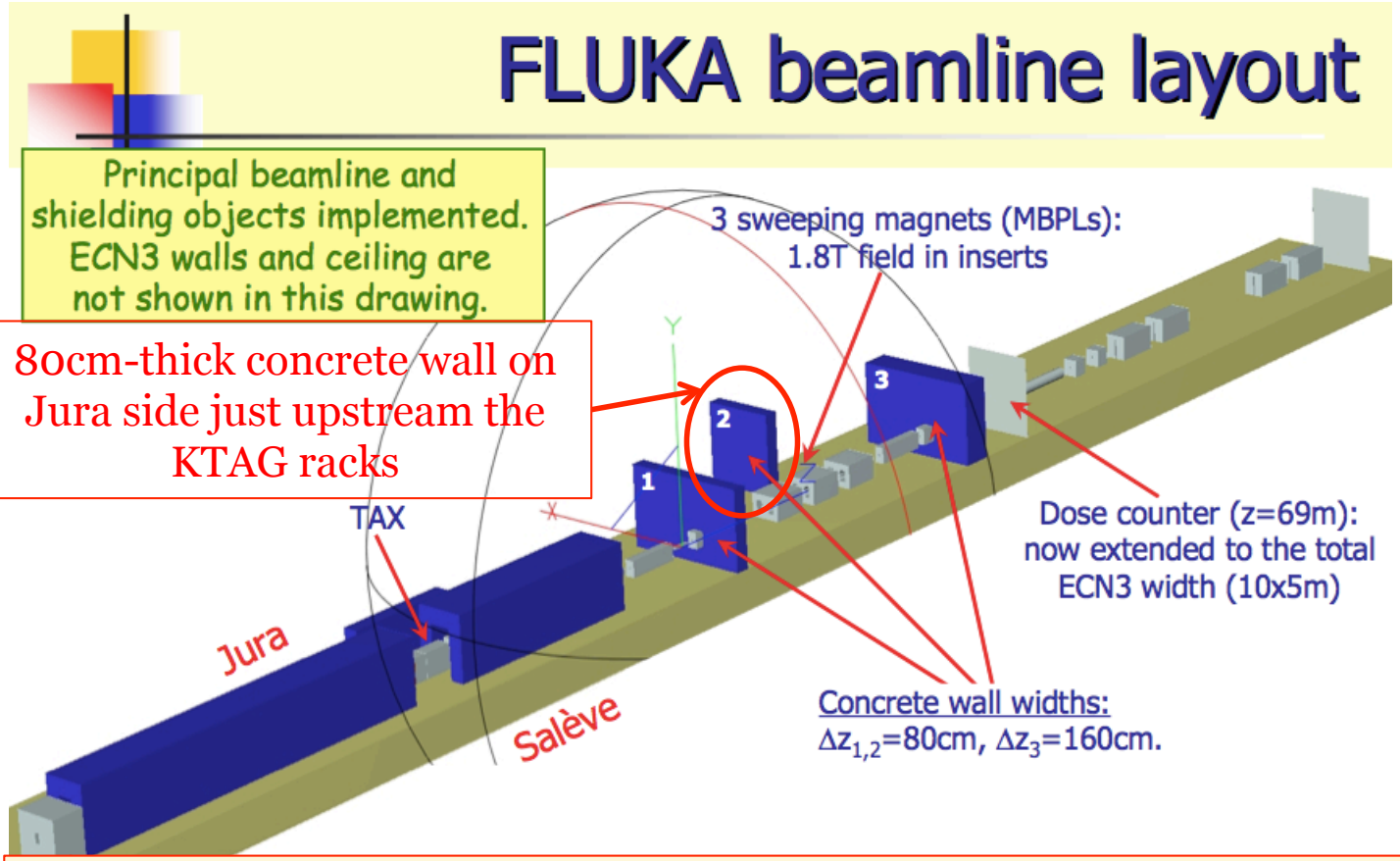
K.Massri's – TDAQ – 06.04.2011

Summary of radiation tests with muons

- Radiation tests of NA62 integrated TDAQ board with a muon beam provided by ISIS Neutron and Muon Source at the STFC RAL
- Tests performed in two visits:
  - Tell1 board with its components using a muon beam; **done ✔**
  - Tel62 (official firmware) board with its components using a muon beam; **done ✔**
- Ultimate goals are the study of radiation-induced single event effects, total ionization dose and displacement effects.
- Results achieved with Tel62 on FPGAs and DDR memory buffer after exposure to radiation level equivalent to NA62 particle fluence are:
  - NO failure/hardware damage/permanent error observed
  - P(SEE on SL) < 1.5×10^{-11} @ 95% C.L.
  - P(SEE on PP) < 1×10^{-11} @ 95% C.L.
  - P(SEE on DDR) < 1.2×10^{-11} @ 95% C.L.

A. Romano - CEDAR WG meeting - 01.04.2014

Motivations - Neutrons



The estimated neutron dose behind this wall is ~0.2-0.4 Gy/year
It could be reduced to ~0.04 Gy/year by doubling the thickness of the wall

E. Goudzovski - CEDAR WG meeting - 30.03.2011

KTAG/CEDAR
Rad-Hard Status

- Front-End Electronics:
  - **NINO ASIC**: tested at PSI in Zurich with protons @ 60 MeV, with total dose 7 krad, by ALICE experiment(*);
  - **Splitter board**: design with passive components: NO FPGAs.
- Read-Out Electronics:
  - **HPTDC** chip tested by CMS and ALICE experiments(*) at CERN and found to be functional above to 50 krad;
  - **Tel62**: design with (NO rad-hard) active components, e.g. FPGAs need to be tested for radiation exposure with expected NA62 particle fluence.

100 rad = 1 Gy

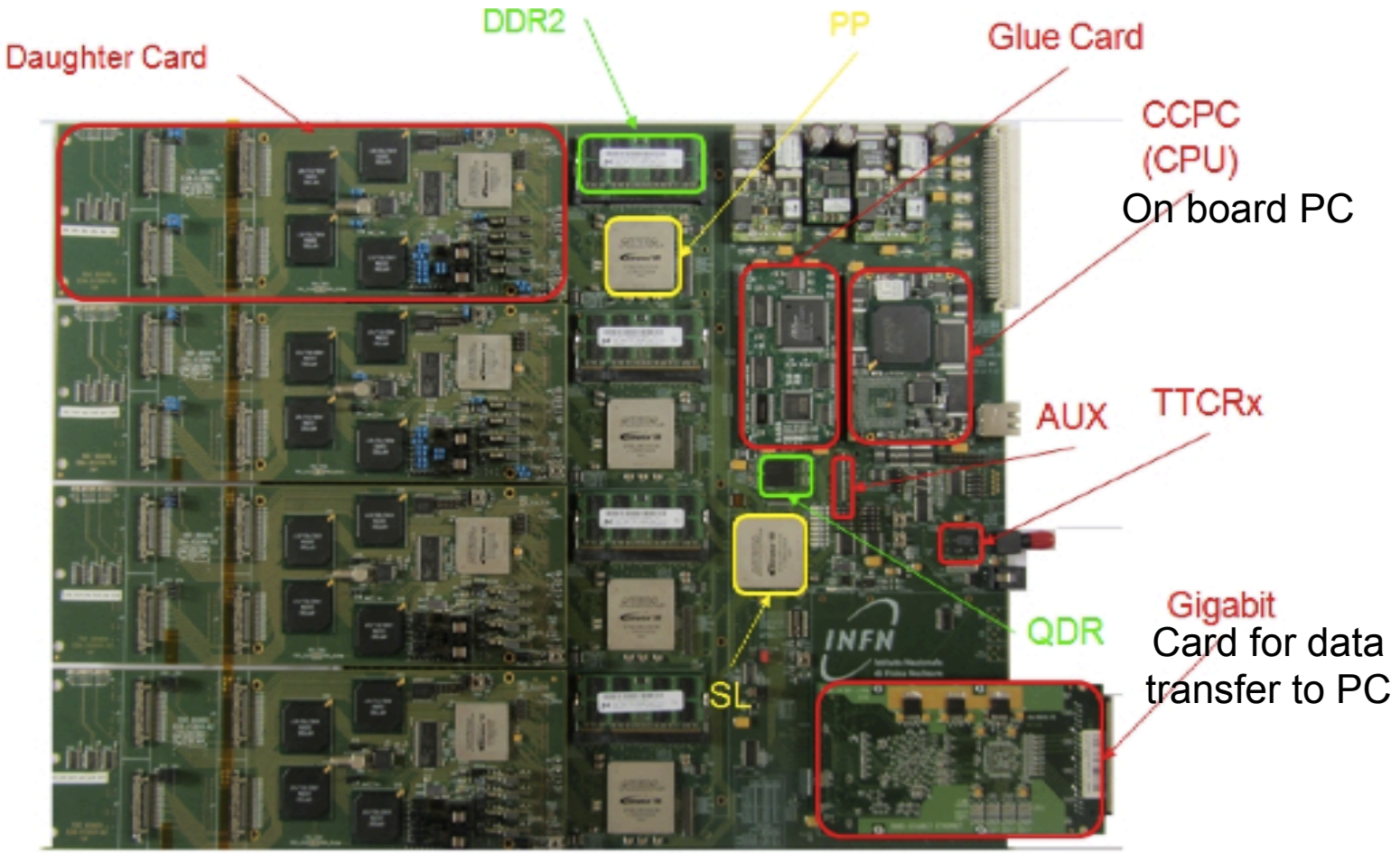
(*) info from private email exchange

Tel62 – NA62 TDAQ board

4 TDC -> Daughter Card

4 DDR2 -> new memory buffers

4 PP, 1 SL improved FPGA (Altera StratixIII (EP3SL110F1152C4N))



Goals & Strategy

- **Test Tel62 board for radiation-induced effects**:
  - Cumulative effects: FPGA performance deteriorations after the exposure to a certain level of radiation;
  - Single Event Effects (SEEs): detection of SEU/SEL (upset/latch-up) in FPGAs and memory buffers during the neutron irradiation;

- **Strategy:**
  - Online monitoring of Tel62 board performances (FPGAs + memories) under radiation exposure;
  - Investigate possible failure/hardware damage/permanent error;
  - Check data integrity flow & storage;
  - Investigate hardware and/or static errors in the firmware;
  - Detection and Measurement of SEE (SEU/SEL) cross-sections.

Radiation Test - Plan

- Irradiation of active components on the electronic board with a neutron beam provided by VESUVIO instrument at RAL:
  - Energy spectrum between: (1-10) MeV
  - Beam flux (energy dependent) estimation based on beam counter measurement: $\Phi(n) \approx 4.7\times10^{5}$ neutrons/cm^2/s -> (@ proton current of 180 uA)
  - Transverse dimensions ($\phi\approx5$cm)
- Estimated neutron flux on FPGA surfaces (~3x3 cm^2) -> $\Phi(n) \approx 4\times10^{6}$ s^{-1}
- Probability of neutron collisions ~ few %
- Average energy <E> released by (1-10)MeV neutrons on FPGA≈1.4MeV(*)
- dE/dt released by VESUVIO neutron beam -> ~6 $\times10^{4}$ MeVs^{-1}
- Assuming ~6gr of silicon and the conversion 6.24*10^{12} MeV/Kg = 1 Gy

Na62 predicted dose/year (~0.4Gy) is achieved in ~1 hours of VESUVIO neutron beam irradiation

- Three separate runs performed on PP, SL and DDR;

(*) energy released by protons produced in knock-on collisions of neutrons with absorber atoms

Measurements & Settings

Measurements:

- TDC emulator used to write known data/words on memory banks;
- Data distributed over frames with corresponding timestamps;
- Word-by-Word read/scan and comparison with expectations;
- On-line data integrity check and storage of BadWords (not matching with expectations -> radiation induced effect);
- Detection of SEE (bit flip and static error) as happening in FPGAs, in data flow and storage.

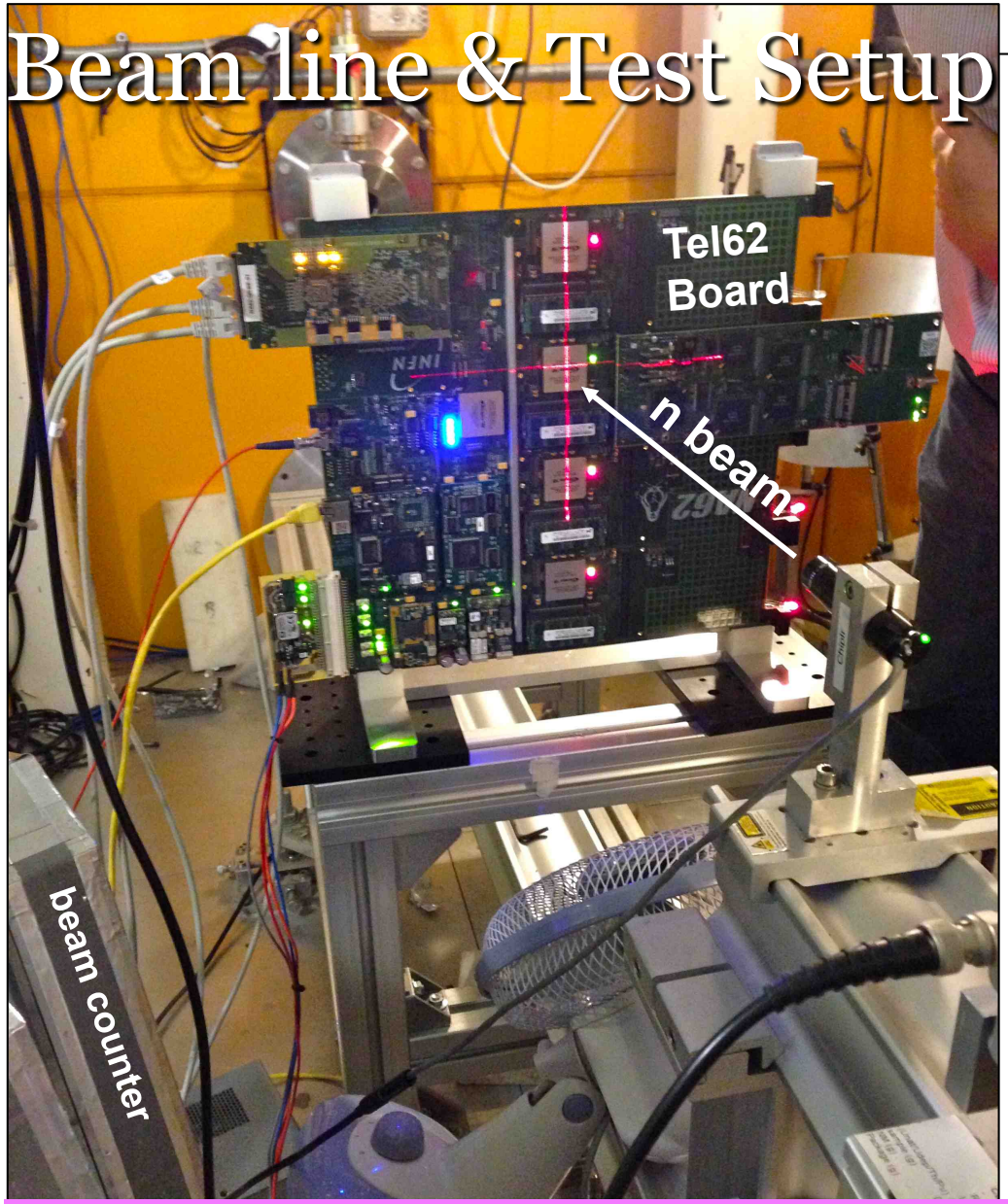
Setting (Equipment from Birmingham):

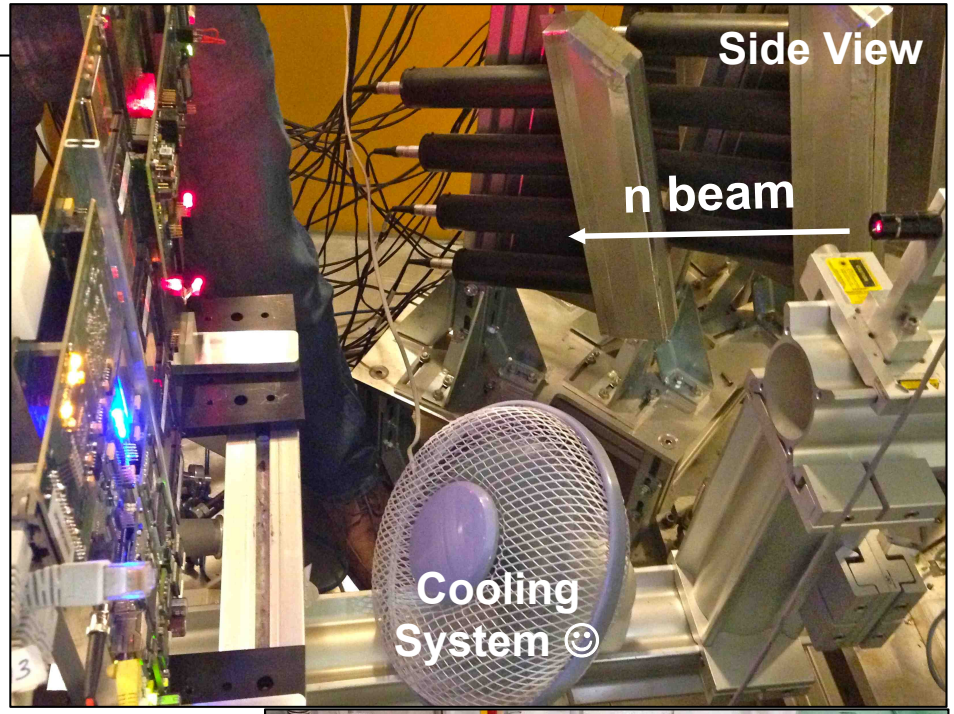
  - Tel62 board with FPGAs, TDCs and power supply;
  - LTU-TTCeX to provide clock, trigger, SOB and EOB;
  - PC to control the Tel62 board and DAQ.

Equipment from ISIS-VESUVIO facility:

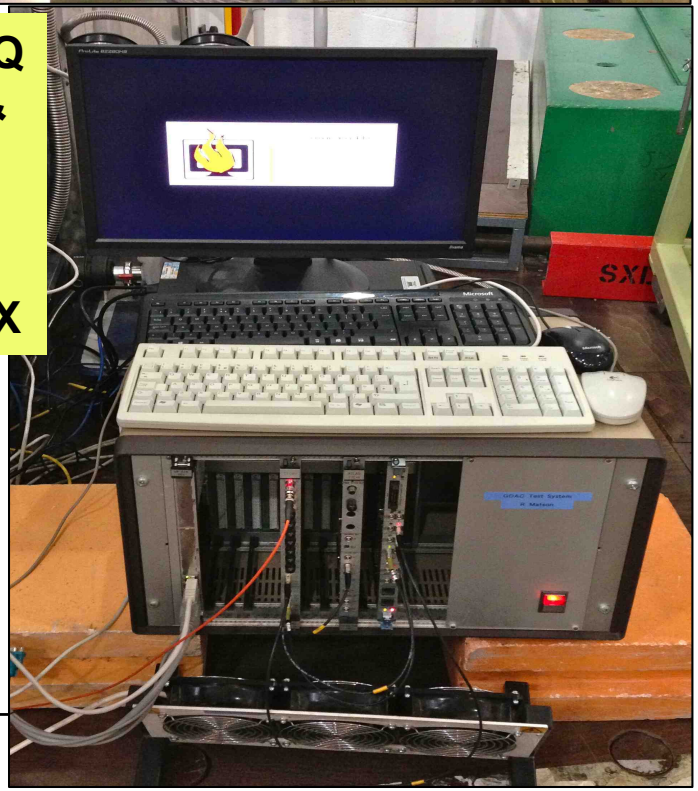
- counters to measure the particle beam flux, 6U-VME crate.

Beam line & Test Setup





PC for DAQ monitor & control + VME crate for LTU-TTCeX



Neutron beam irradiating FPGAs on Tel62board: particles produce knock-on collisions displacing absorber atoms

SEE (SEU-SEL) induced by energy deposition from displaced charged particles (protons)

Test & Results - NoRad

Pre-Test (NO beam):

- Performed in Birmingham (before March 2014);
- Used to evaluate the probability of system-dependent failure;
- ~ 16 hours of data taking;
- DAQ smooth and no need for recovery procedures;
- Cross-check on site, DAQ time = 2.5 hr; ***ok ✔***

✓ ToT = 3.2×10^{11} words acquired;

✓ Successful word-by-word scan&comparison between readings and expectations;

✓ Zero fails found -> Set upper limits (in simple case of no bkg):
- P(fail) < $3/3.2\times10^{-11}$ @ 95% C.L.
- P(fail) < $2.3/3.2\times10^{-11}$ @ 90% C.L.

Test & Results - SL

Test - I (SL-FPGA):

- Used to evaluate the probability of SEE and/or radiation-induced system failures;
- Observed Failures: SL stop working properly/Trigger counters giving random number/"DDR overflow";
- SL working fine after recovery procedures ("Board Reload") and re-initialization, "sldump" used to check configuration registers

✓ DAQ time ~30min ≈ 1/2 expected NA62 dose/year(*)

✓ Reproducibility tested the next day ..

✓ **Tel62 firmware reload** needed after a dose equivalent to ~50days of NA62 data taking;

✓ SL-FPGA reasonably working and power-cycle not needed;

✓ Frequency of recovery procedures is below "foreseen" interventions during NA62 data taking ..

(*) assuming 100 days per year of data taking

Test & Results - PP

Test - II (PP-FPGA):

- Used to evaluate the probability of SEE and/or radiation-induced system failures;
- Observed failures in random order for several runs after ~10min DAQ: word mis-matching (unexpected kind)/"DDR overflow"/ error in "DDR data arbitrer" register;
- Recovery procedure ("Board Reload") and re-initialization -> not effective – Power-cycle needed !

✓ DAQ time ~10min ≈ 1/6 expected NA62 dose/year(*)

✓ Reproducibility tested the next day .. same story ..

✓ **Tel62 board power-cycle** needed after a dose equivalent to ~15days of NA62 data taking;

✓ PP-FPGA restart well after POWER CYCLE - it lasts again 10min;

✓ PP-FPGA less performing than SL-FPGA under neutron irradiation, Why? Different firmware? More sensitive? Already damaged?

(*) assuming 100 days per year of data taking

Test & Results - DDR

Test - III (DDR-Memory):

- Used to evaluate the probability of SEE and/or radiation-induced system failures;
- DAQ smooth and no need for recovery procedures for > 1hr ☺
- Word mis-matching detected but strong similarity with PP-Run noticed -> possibly induced by radiation from beam halo on PP-FPGA ?

✓ DAQ time ~1hr ≈ expected NA62 dose/year(*)

✓ Reproducibility tested the next day .. same story ..

✓ **Tel62 board power-cycle** needed after a dose equivalent to ~100days of NA62 data taking;

✓ DDR restart well after POWER CYCLE ☺

✓ DDR memory less affected by neutrons. No SEE detected in data storage.

(*) assuming 100 days per year of data taking

Summary

- Radiation tests of NA62 integrated TDAQ board with particle beam provided by ISIS Neutron and Muon Source at the STFC RAL
- Tests organised in three phases:
  - Tell1 board with its components using a muon beam; **done ✔**
  - Tel62 (official firmware) board with its components using a muon beam; **done ✔**
  - Tel62 (official firmware) board with its components using a neutron beam; **done ✔**
- Ultimate goals are the study of radiation-induced single event effects, total ionization dose and displacement effects.
- Results achieved with Tel62 on FPGAs and DDR memory after exposure to neutron radiation level equivalent to NA62 particle fluence/year are:
  - NO failure/hardware damage/permanent error observed
  - Recovery procedures needed (SL+PP+DDR) every ~15days of NA62 data taking
  - Tel62 Firmware reload & Power cycle sufficient to restart the DAQ
  - Word mis-matching observed but maybe not affecting data .. bit flip in register ?

Outlook

- Neutrons are more dangerous than muons ☹
- Expected neutron dose (Evgueni's estimation with Fluka) drops from 0.4 Gy/year to 0.04 Gy/year behind a 160cm thick concrete shielding ..
- Current status of shielding upstream the KTAG readout crate is 80cm concrete block (-> see picture)

- Doubling the concrete shielding upstream the KTAG electronic rack:
  - needed at nominal beam intensity
  - supported by the radiation tests
  - will allow to run without radiation-induced recovery procedure for > 100 days of NA62 data taking

SPARES

Motivations - II

- Radiation induced effects on micro-electronics circuits can be divided into two categories:
  - **Cumulative effects**: (i.e. TID) gradual effects taking place during the whole lifetime of the electronics exposed in a radiation environment;
  - exhibit failure when the accumulated TID (or particle fluence) has reached its tolerance limits;
  - lead to a hardware damage of the electronic components of the board, resulting in a permanent error and/or stop of functionality leading to failure of the whole circuit.

Motivations - III

- Radiation induced effects on micro-electronics circuits can be divided into two categories:
  - **Single Event Effects (SEE)**: due to the energy deposited by one single particle in the electronic device;
  - can happen in any moment since the beginning of operation in the radiation environment (probability expressed in terms of cross-section);
  - can cause hardware errors, e.g. Single Event Latch-ups (SEL);
  - can lead to static errors, e.g. Single Event Upsets (SEU)
  - Possible radiation damages to:
    - Firmware;
    - Configuration;
    - Data storage.

Single Event Effects (SEE)

- **Hardware errors**:
- destructive events leading to a permanent error
- E.g: when latch-up occurs, the chip symptomatically draws a large current and it can fail if power is not turned off quickly.
- **Static errors**:
- can overwrite information stored in the circuit
- E.g: an upset in the content of a memory cell in the chip can interrupt logic functions of an FPGA.
- Static errors can affect several level of the firmware:
- damages at the **executable level** can lead to data corruption and/or interruption of the data acquisition;
- damages at the **configuration level** can lead to data corruption and/or partial data acquisition.
- Different kind of studies are foreseen to investigate on different radiation induced errors.