Bump Bonding status

R.Arcidiacono, F. Marchetto

Universita' del Piemonte Orientale
and INFN Torino

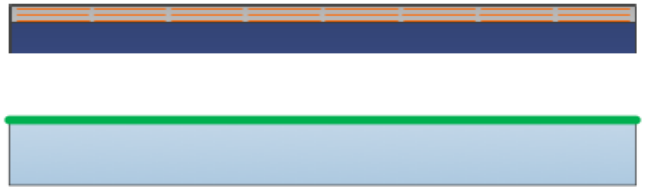
Outline

- GTK Bump Bonding: procedure for thin chips
- Pre-series assemblies:
  - the good and the bad ones → analysis of the faults
- Real assemblies:
  - first detectors received
  - What comes next and when

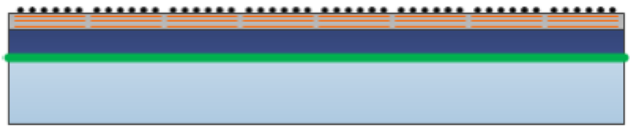
Flip-chip of thin TDCpix chips

Process steps for the assembly of thinned read-out wafers with sensor wafer

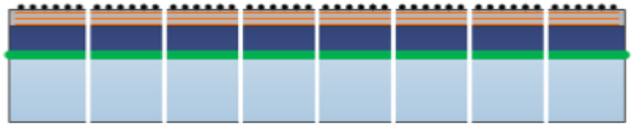
1. Backside grinding



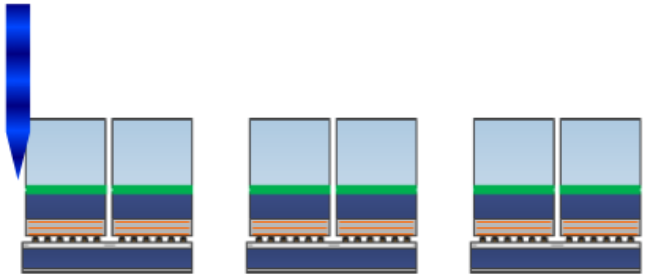
2. Support wafer bonding



3. Bump deposition

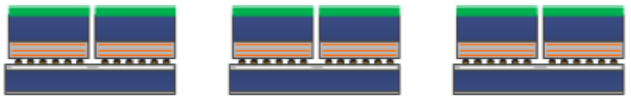


4. wafer stack dicing



5. Flip chip assembly

6. Laser induced debonding

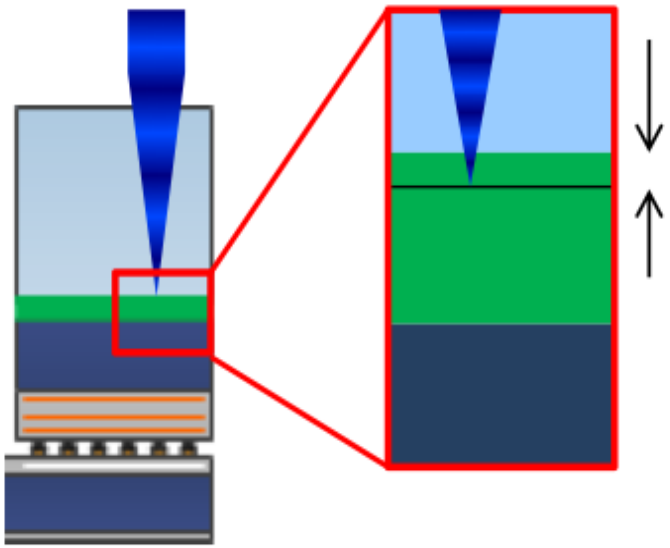


7. Support chip removal

The Glass Carrier Release

One of the most delicate steps, requiring careful handling.
New machine in house at IZM.

Polyimid based glue material



Laser light fully absorbed in a 200nm thick glue film – decomposition and opening of the bonding zone

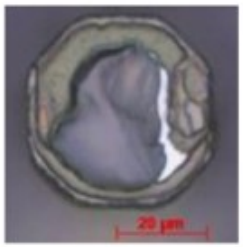
Pre-series Assemblies

- **Most of the pre-series is at CERN**
  - Gain experience with testing, probe positioning for TDCpix wafer testing, full integration chain etc → ongoing

- **Bad Modules 6,9,10 @IZM have been scrutinized in detail. Full report delivered 2 weeks ago.**
- **Assemblies desoldered and inspected:**
  - **very small number of not soldered bumps.**
  - **many lifted bumps found, which indicates a strong pull force at temperatures below the solder melting point. Sometimes the lifted bumps had remaining silicon chips on the backside.**
    The bump lift can occur at several process steps in the chain, like during the glass carrier release, or during the handling (picking the module out of a gel pack etc).

Pre-series: the bad ones

Various types of problem found:

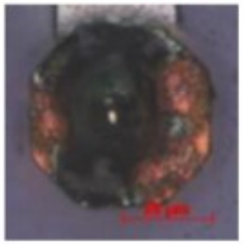


Cratering Chip:
Silicon cratering on chip side
→ Bump incl. pad from chip side remained on substrate
→ Si on top of pad backside

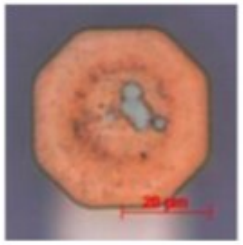
Cratering Substrate:
Silicon cratering on substrate side
→ Bump and pad incl. piece of Si pulled off the substrate
→ Crater in Si remained on Substrate

Padlift Chip:
Padlift on chip side
→ Bump incl. pad from chip side remained on substrate

Padlift Substrate:
Padlift on substrate side
→ Bump incl. pad pealed off the substrate



NG Wetting:
$N_{ot}G_{ood}$ Wetting
→ Partial wetting on pad
→ # mentioned in the colored square

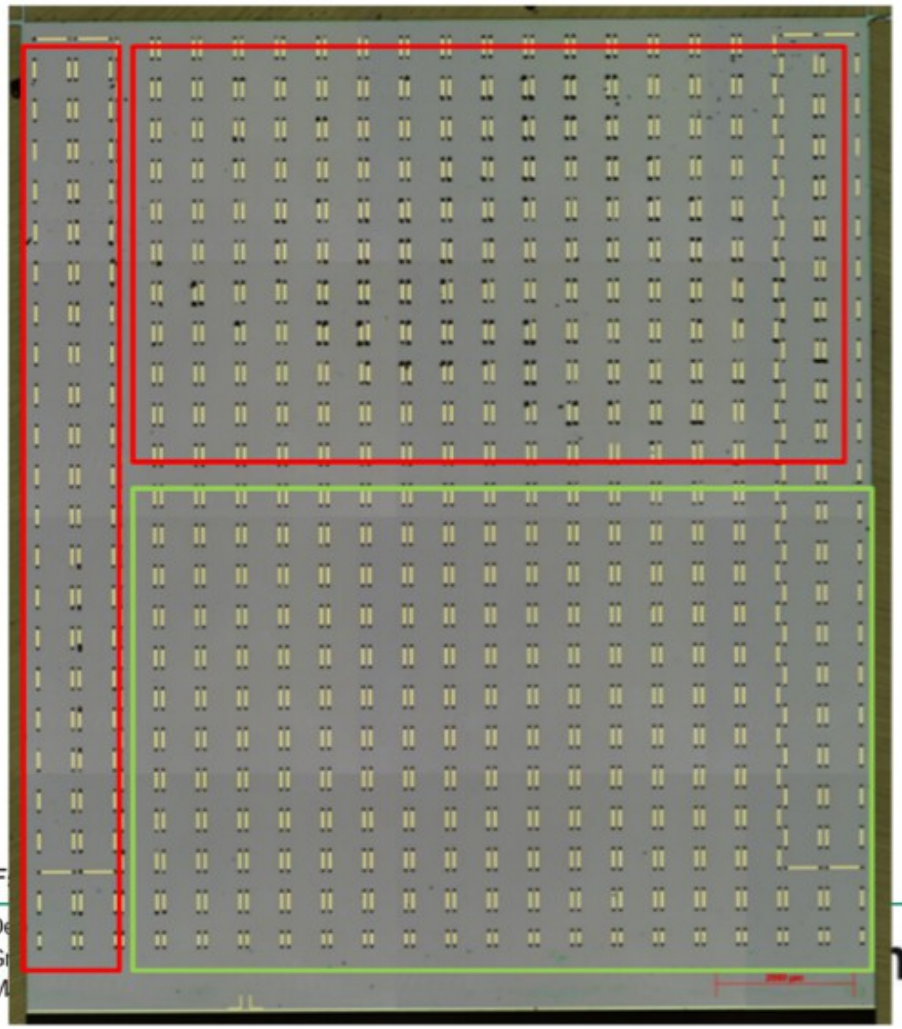


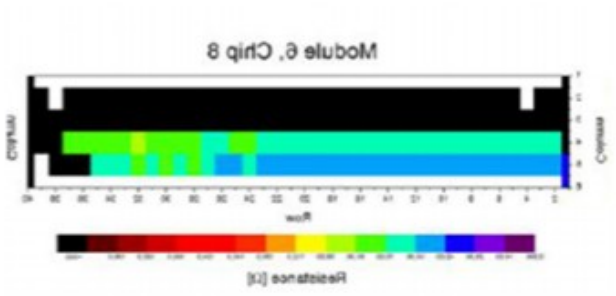
No Wetting:
Not wetted pad
→ # mentioned in the colored square

Pre-series: the bad ones

EX: module 6 chip 8

Module 6 – Chip 8_sensor side





- Alot cratering chip
- Cratering chip and padlift chip
- Good wetting

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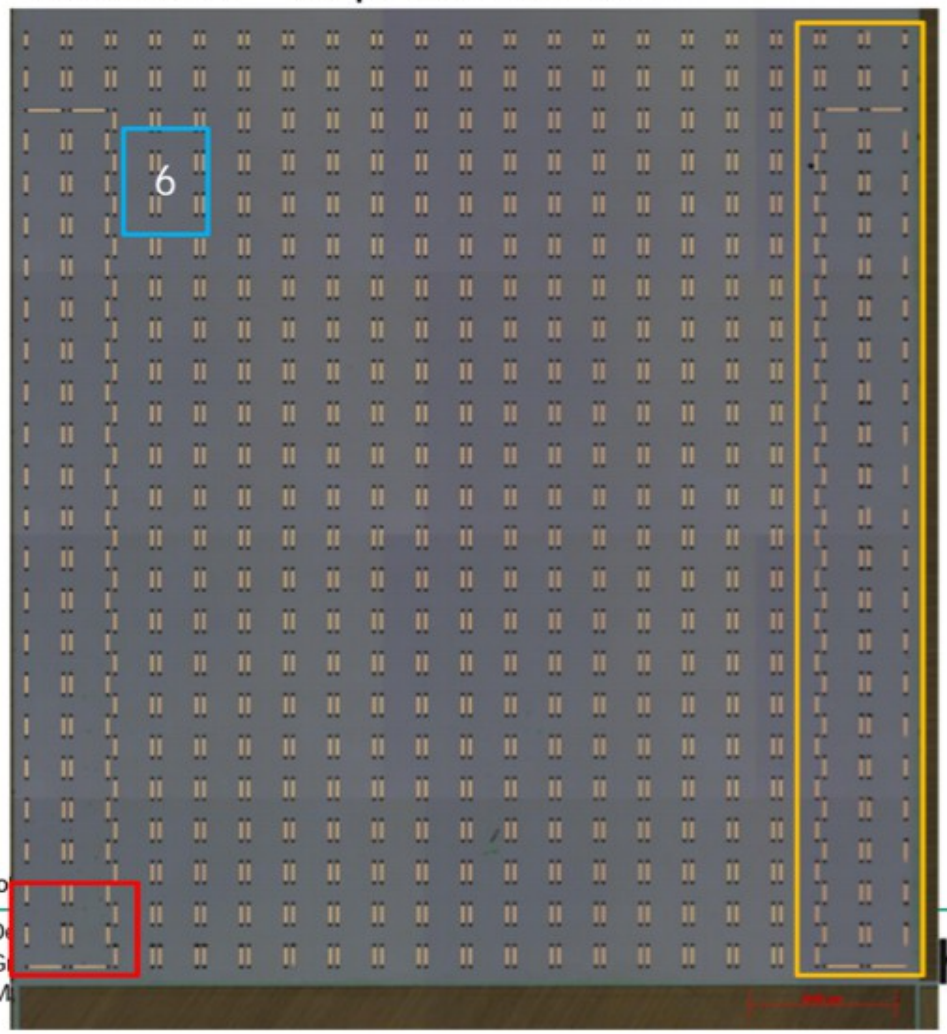
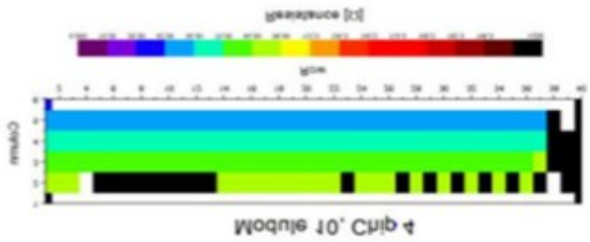
Pre-series: the bad ones

EX: module 10 chip 4





- 6 NG Wetting, cratering chip
- Padlifts Substrat, cratering chip
- NG Wetting

Summary to be discussed with IZM soon

hofer IZM

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Technische Universität Berlin
Forschungsschwerpunkt Technologien der Mikroperipherik

Real Assemblies Plans

FAST TRACK

One ROC wafer not thinned (3 weeks saved) + **2** sensor wafer processed for bump-bonding

After 6 weeks, two full module + 6 single chips should be ready

Started on May 20 → expected for beginning of July

REGULAR TRACK

Two ROC wafers **thinned to 250 and 100 μm** + all sensor wafers (type 1 p-on-n) processed for bump-bonding

After ~ 3 months, assemblies (6 full modules + 12 single chips) should be ready

Started mid May.

→ **mid August**

FROM JUNE GTK WG

First Real Assemblies @ CERN

First Assemblies from the fast track (high priority) arrived at CERN July 1st .

- **Deadline has been met successfully !**
- Important to notice:
  - **2 full modules (instead of 1)**
  - **6 single chips (instead of 3)**
- **All read-out chips have been thinned to 450 microns** (by scrubbing the assemblies after bump bonding)

First Real Assemblies @ CERN

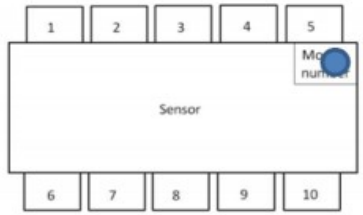
First Assemblies from the fast track (high priority) arrived at CERN July 1st .

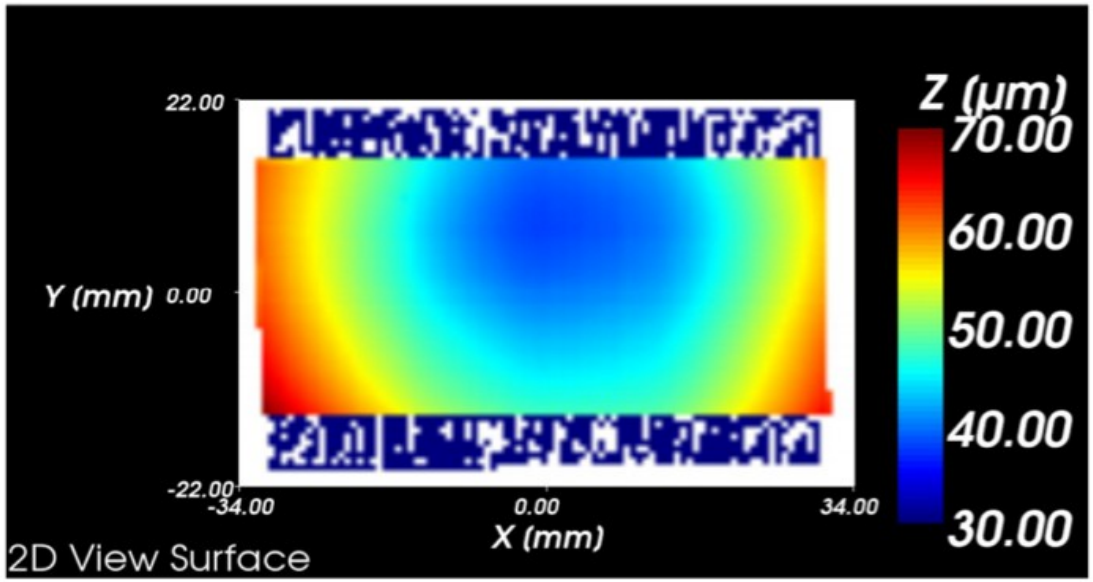
- All **single chip detectors** wired bonded and under tests in the demonstrator by Mat:
  - So far no problems encountered
  - Polarized up to 450 V
- Full module waiting to be integrated: as soon as the cooling plates arrive (Michel &co testing and preparing the two GTK carriers)

First Real Assemblies: Bow

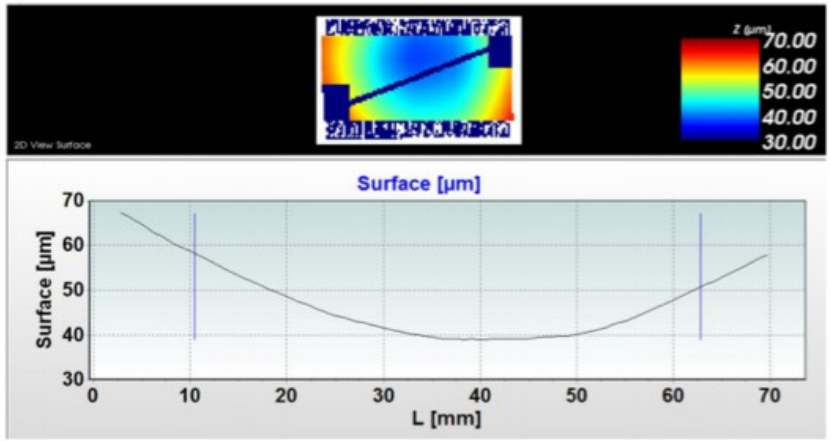
mmenfassung_Fast trackBatch_sens_13_14.pdf Open with

NA62_Modul14_sensor



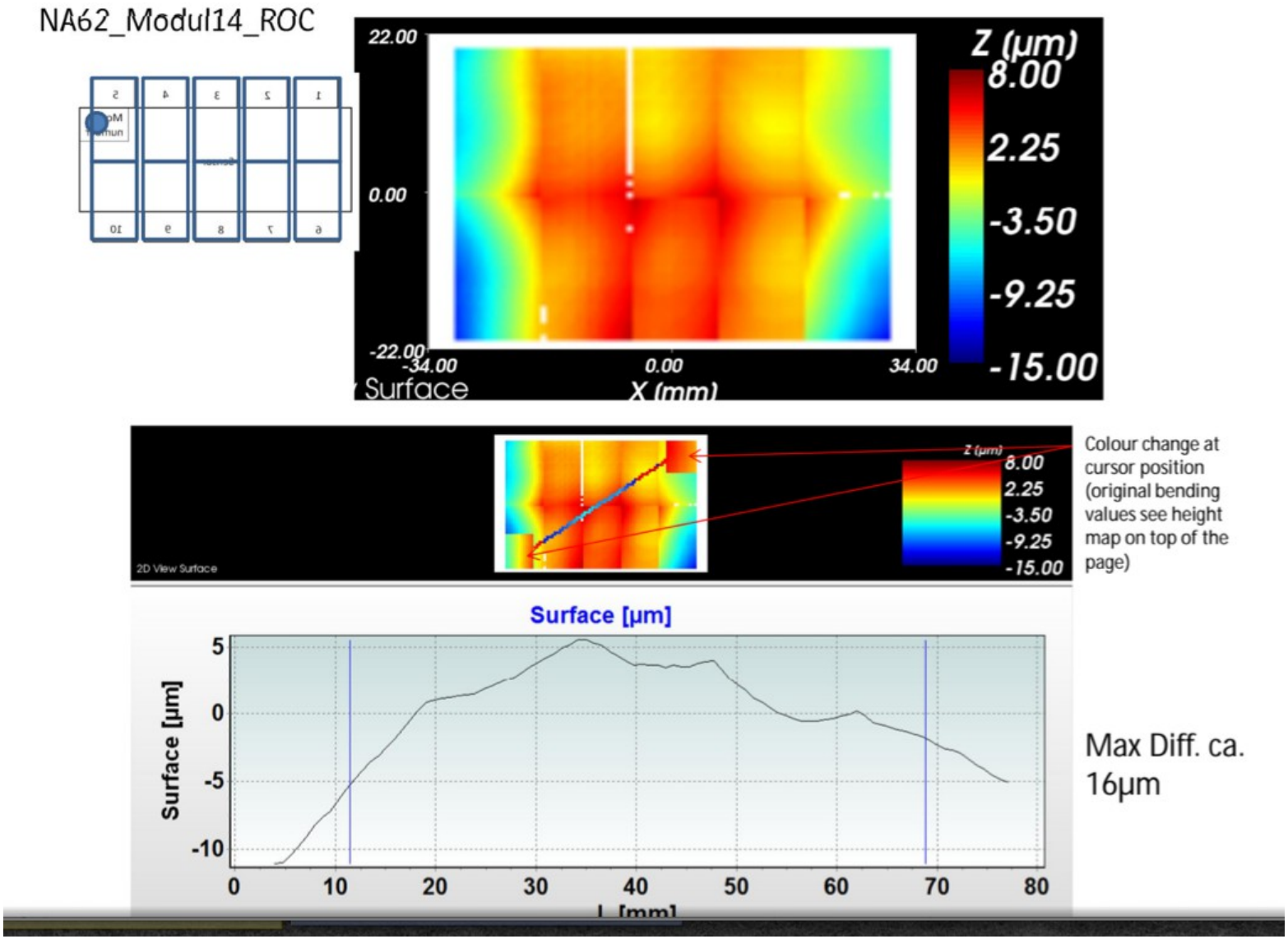


Max Diff. Ca. 30µm



Bow on sensor side - better than dummies

First Real Assemblies: Bow



Bow on ROC side - better than dummies

Status of thin detectors

Some disruptions due to vacation period determined a 3 weeks delay

→ delivery now foreseen for end of week 36

7/9/2014

To be delivered to CERN soon:

- **3 full modules + 6 single chips thinned to 250 μm**
- **3 full modules + 6 single chips thinned to 100 μm**

Week 34: modules prepared for laser debonding. Need best operator for this step.

Week 35: Laser debonding (glass carrier release)

Week 36: measurement of planarity, shipment to CERN.

Outlook

- **Final assessment on pre-series quality and weak point identifications**
- **Looking forward to the arrival of the thin detectors**
- **Looking forward to see some BB efficiencies of the existing real assemblies**
- **Test plan for the thin single chip assemblies (thermal cycles etc)**