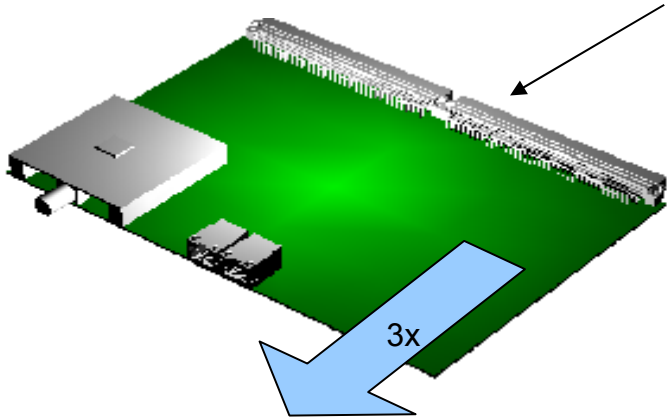
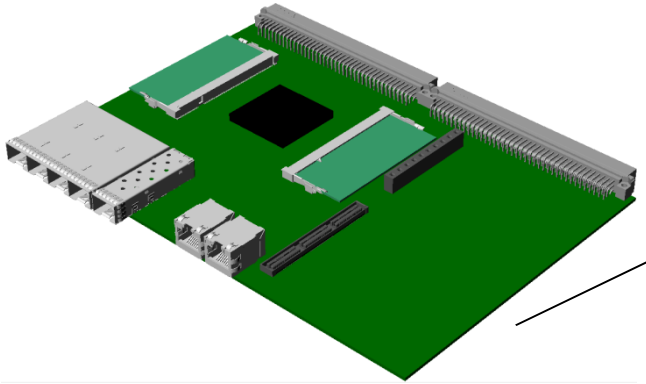
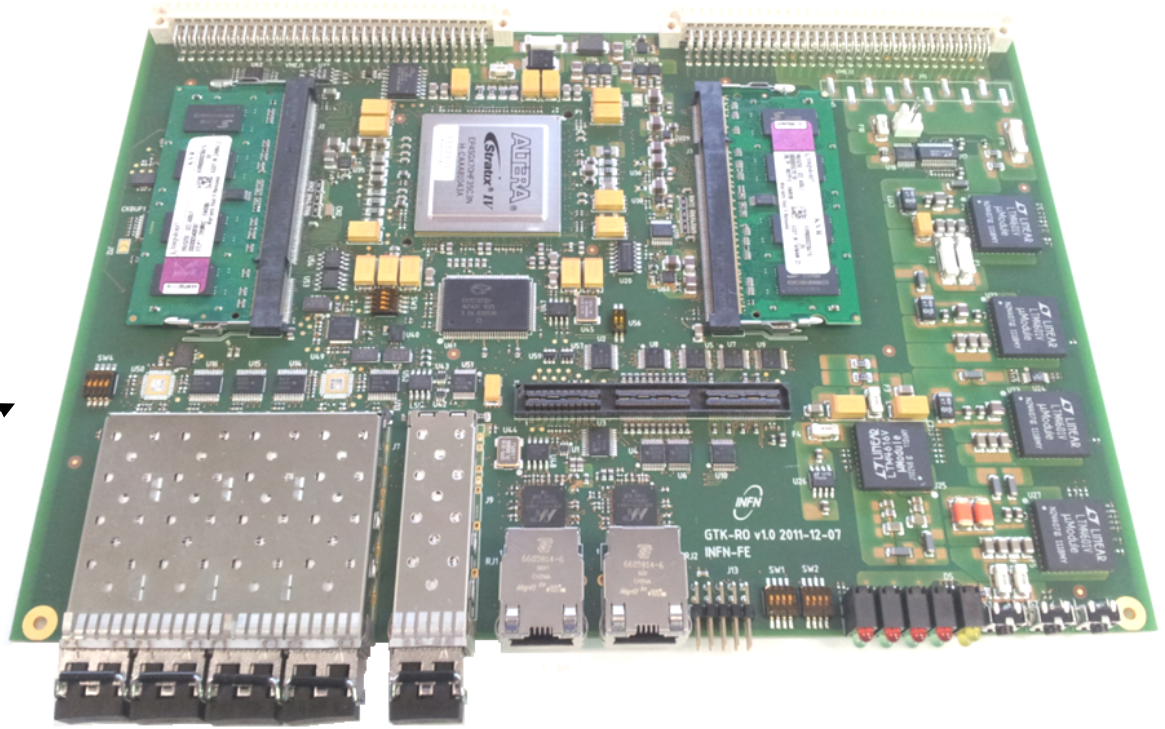
Update on TTC interface card and timing generator

TTCINT / GTKTTC interface

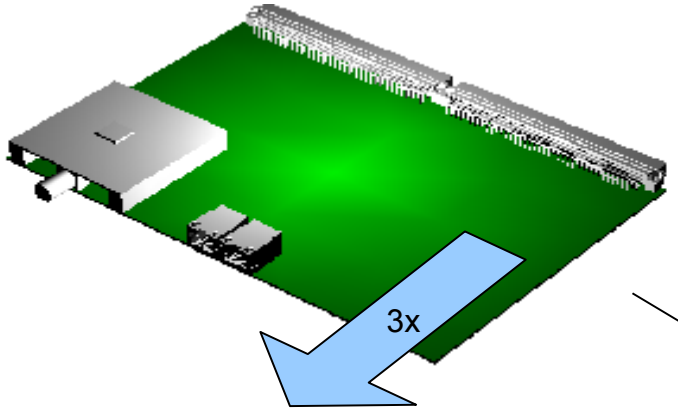


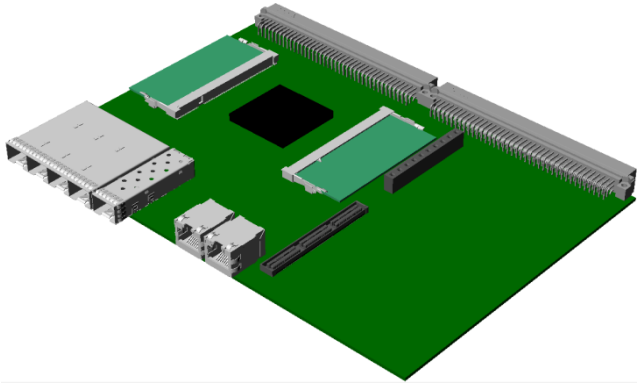




GTK_RO main board

Update on TTC interface card and timing generator

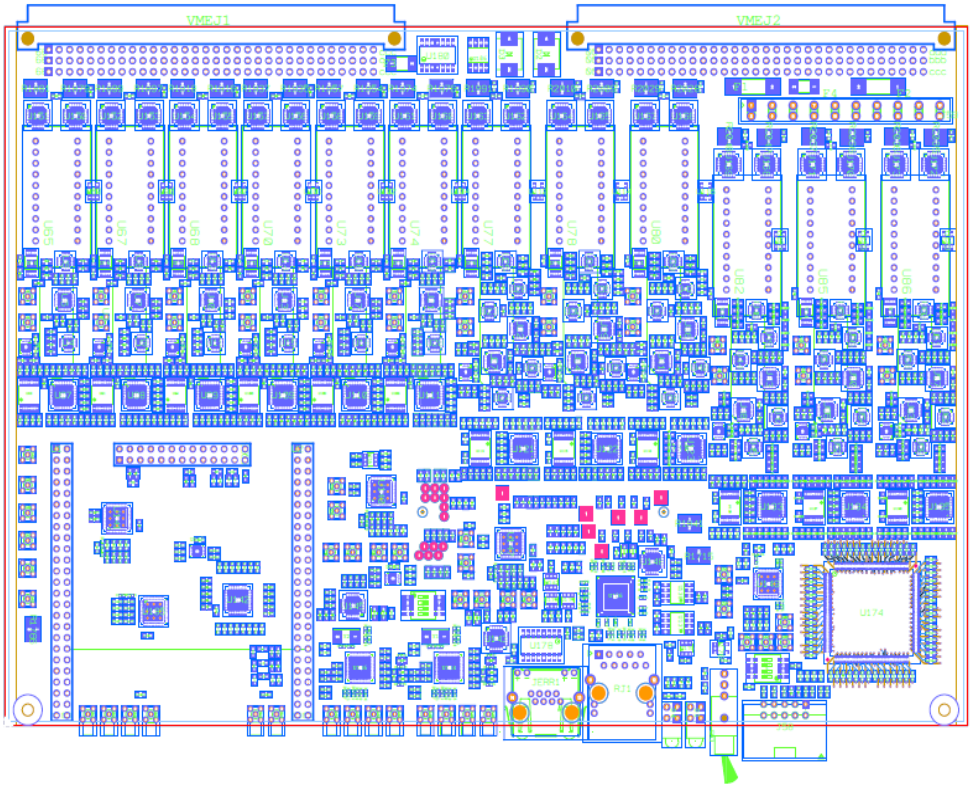




GTK_RO main board

TTCINT / GTKTTC interface

Final PCB placement (01/08/2014)



Update on TTC interface card and timing generator

The TTC interface card is a daughter module for the GTK_RO main board configurable in two different modes:

TTCINT mode

- **Interfacing with NA62 TTC system (one TTCrq module per GTK_RO board)**
- **Choke/Error port interface (full crate wide, single slot wide)**
- **Gigabit ethernet port for additional board management (not interferring with ports dedicated to high speed DAQ stream)**

GTKTTC mode

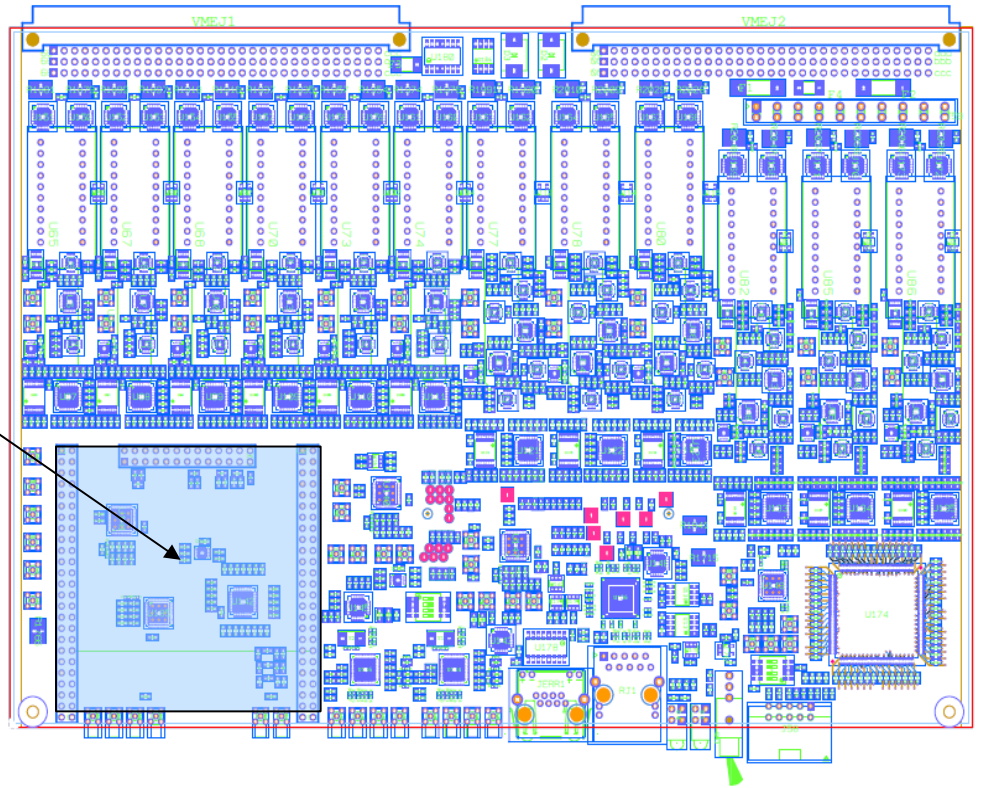
- **DLL clock, Digital clock, Test pulse and Reset signals generated for all GTK stations (3x optical transmitters)**
- **DLL clock signal with jitter as low as possible and skew across 3 station as stable as possible (fixed frequency 320MHz)**
- **Test pulse and Reset signals with adjustable time position for both positive and negative edges respect to the clock period (pulses shorter than a clock period can be generated)**
- **Digital clock with selectable frequency (240 Mhz, 320MHz and 480MHz)**

Update on TTC interface card and timing generator

TTCINT / GTKTTC mode

TTCrq module receives NA62clock, Level-0 Trigger signal, Trigger qualifiers, Start of burst, End of burst signals.

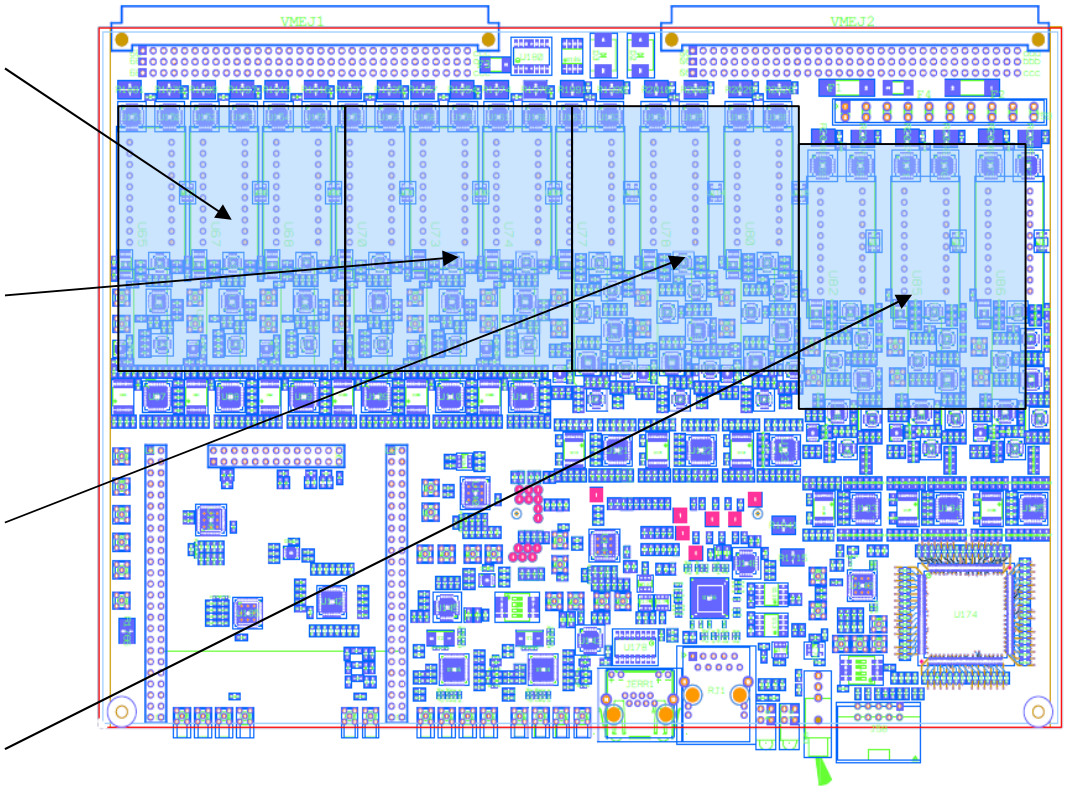
TTCrq module is installed for both TTCINT / GTKTTC modes.



Update on TTC interface card and timing generator

GTKTTC mode

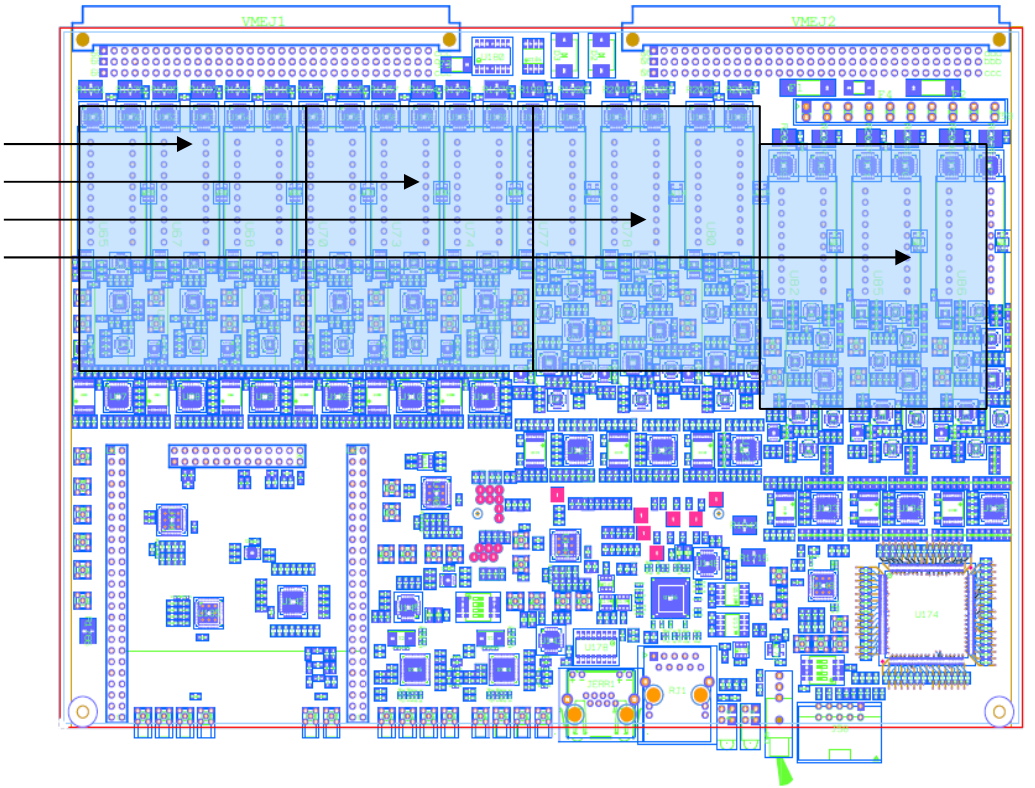
- **Digital clock to all GTK stations (3 x STX24 optical transmitters)**
- **HiQ clock to all GTK stations (3 x STX24 optical Transmitters)**
- **Reset to all GTK stations (3 x STX24 optical Transmitters)**
- **Test Pulse to all GTK stations (3 x STX24 optical transmitters)**



Update on TTC interface card and timing generator

GTKTTC mode

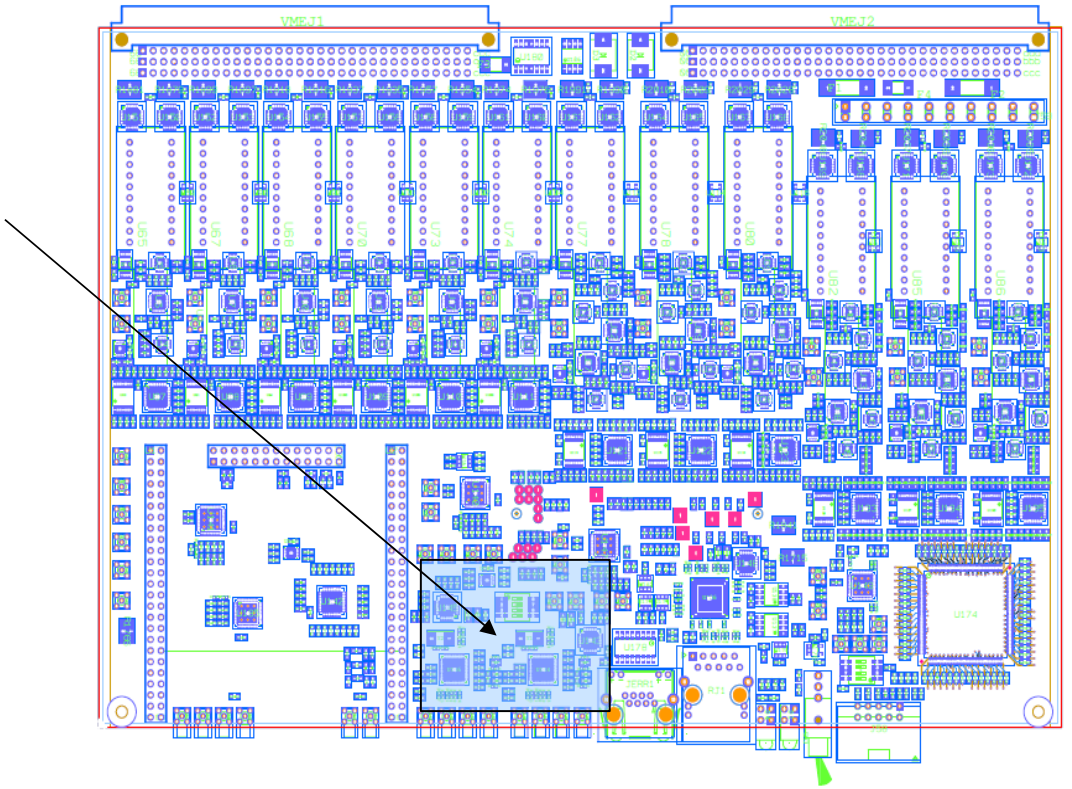
Signals driving optical modules should have a programmable phase delay respect to the NA62clock and a precise timing adjustment with sub-nanosecond resolution



Update on TTC interface card and timing generator

GTKTTC mode

The board includes a group of PLL working as clock jitter cleaner and frequency synthesizer. These devices are driven by the NA62 reference clock received by TTCrq module.

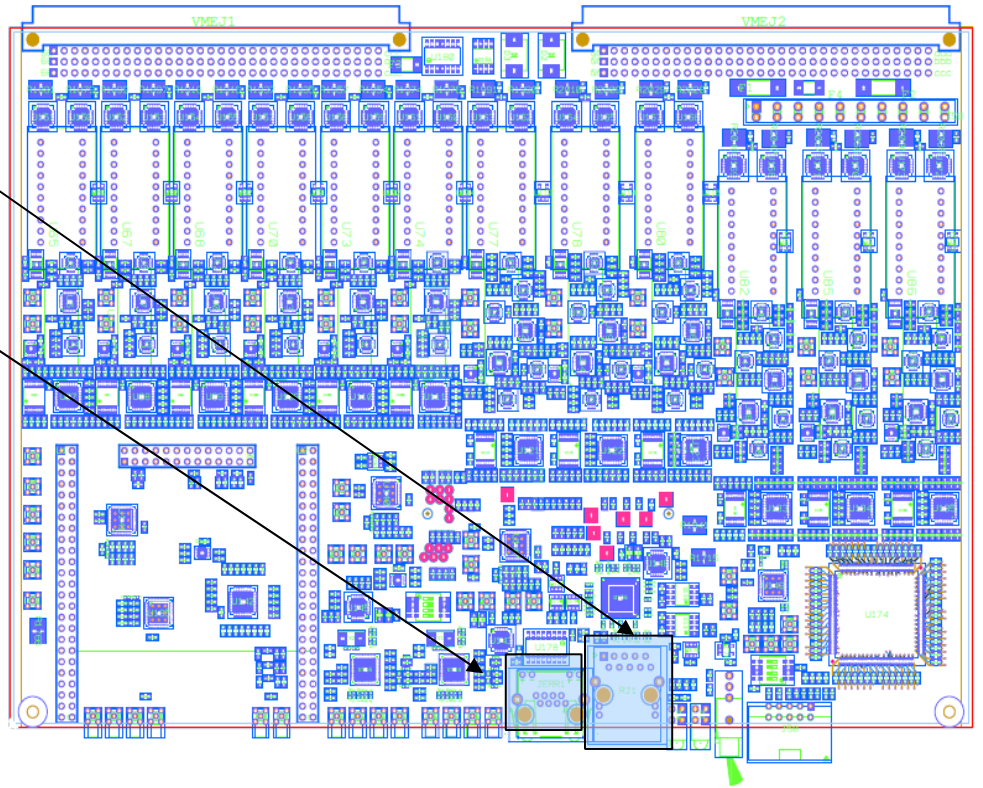


Update on TTC interface card and timing generator

TTCINT mode

Gbit ethernet port for additional board management

Choke / Error interface port



Boards configured for TTCINT mode work as TTCrq interfaces, Choke / Error interfaces and extend the ethernet ports controlled by the main board FPGA.
TTCINT boards do not mount optical transmitters.

Update on TTC interface card and timing generator

Current status:

- **Project submitted to the PCB layout facility at the end of May 2014**
- **Placement operations have required a total time of 2 months: the PCB is quite dense and many different strategies of placement has been tried until the final placement layout (01/08/2014).**
- **Some PCB components (selected at the end of 2011 and apparently with a big on-stock availability) suddenly became obsolete/out-of-stock: searching for alternatives has required many interactions with distributors but now all most critical components for both PCB variations has been received**
- **The first prototypes of the TTC interface board is foreseen at the end of september 2014...hopefully we can test the first group of GTK_RO main boards using a different TTCINT daughter board (developed by Ferrara for the GAP project) so we should obtain the first test results in the mid of september**
- **The firmware for the GTKTTC interface is under development**