"off-detector" readout electronics for the Gigatracker: status update

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"off-detector" readout electronics for the Gigatracker (GTKRO): status update

- preparing for the test of interconnection to the TDCpix
- GTKRO motherboard production
- TTCINT / GTKTTC daughter card production

- preparing for the test of interconnection to the TDCpix

A test of interconnection between GTKRO and the TDCpix through optical fibers is foreseen for next week

The goal of the interconnection test is :

- to check that the TDCpix serial link controller implemented on board the GTKRO FPGA is actually capable of exchange data at the physical level with the TDCpix
- to advance with the adaptation of the TDCpix configuration programs developed by Matt Noy's to the Gigatracker subdetector PC environment
- to verify the proper reception of the 3.2Gbps data stream on the part of the GTKRO transceivers and FPGA

- preparing for the test of interconnection to the TDCpix

To prepare the interconnection test:

- a model of TDCpix-side serial link controller which includes the generation of dummy reply token has been implemented (a.c.r.) on board the GTKRO FPGA
- a firmware module ("eth_link_to_slowcontrol.v") has been developed to link this TDCpix dummy module and the subdetector PC via Ethernet has been developed (a.c.r.) and preliminarly tested with a C++ program developed by Enrico Gamberini and based on Stefano's "terminal_udp"

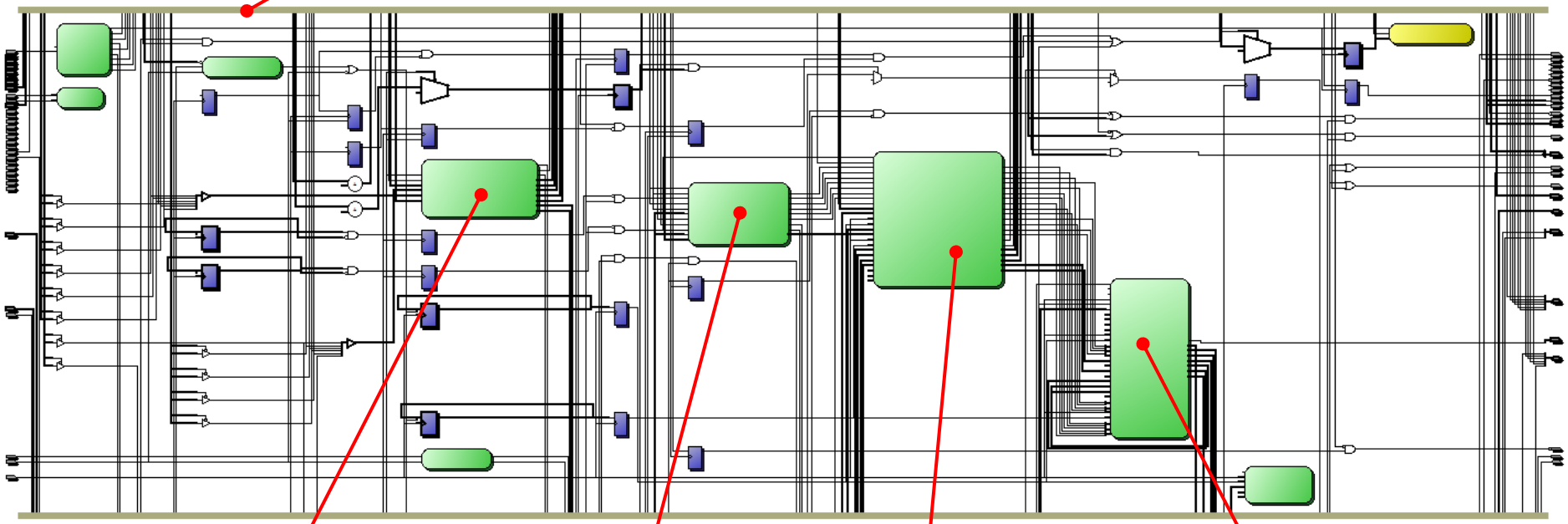
The "eth_link_to_slowcontrol.v" allows to interface, by exchanging Ethernet UDP packets properly formatted and tagged for loss of packet detection, the Gigatracker subdetector PC to the slow control resources implemented in the GTKRO FPGA :

- the TDCpix serial link controller (FPGA side)
- DAQ related status registers (error flags, counter of L1Accept received, counter of L1Accept served)
- GTKRO board control / status register (Timestamp offset, FPGA Temperature, optical link received power..) through the intermediation of the NIOS microprocessor implemented in the FPGA

The "eth_link_to_slowcontrol.v" will be used in the GTKRO system to implement the physical layer of Matthew Noy's TDCpix configuration program suite, based on PCIe communication layer between CPU and link controller FPGA.

- preparing for the test of interconnection to the TDCpix

RTL view of the "GX110_NIOS_MAC_TDCpix_link_top" project prepared for this test



NIOS soft processor running board housekeeping routines

"eth_link_to_slowcontrol.v"

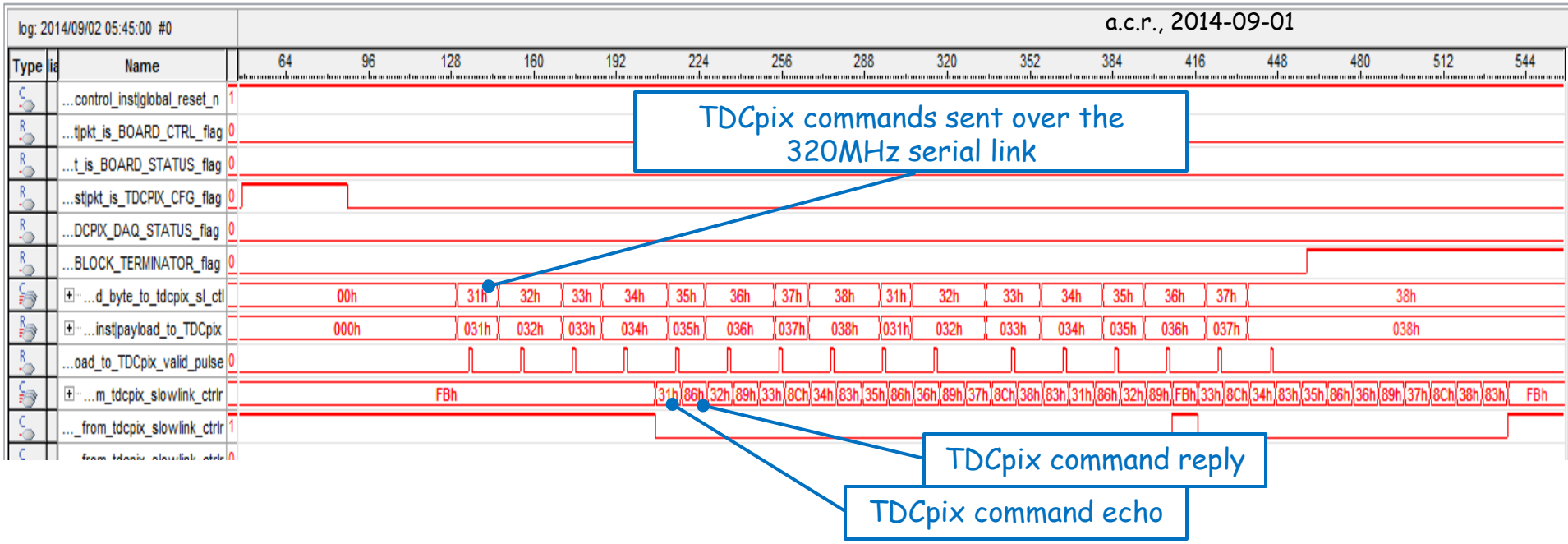
"tdcpixslowcontrol_lb.v" : combination of the FPGA sideTDCpix serial link controller and the dummy TDCpix serial controller target

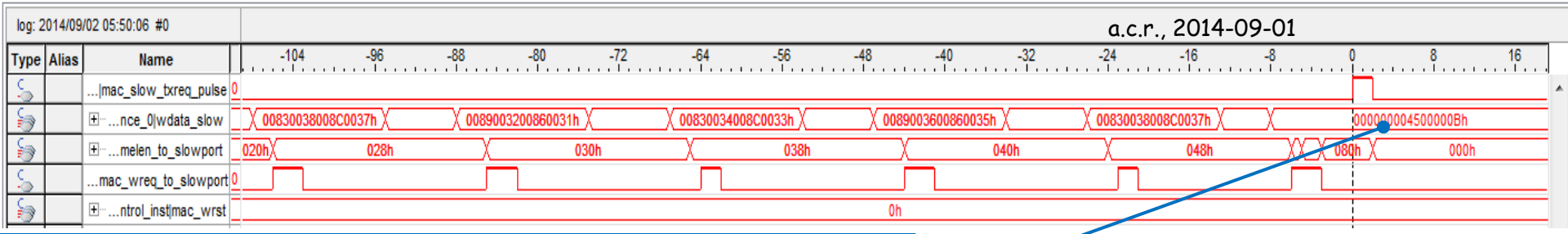
Stefano's ethernet MAC

NIOS firmware controlling the I2C link to on board sensors (XCVR link input optical power; FPGA temperature) was developed by R. Malaguti, INFN-FE

- preparing for the test of interconnection to the TDCpix

"eth_link_to_slowcontrol.v" activity recorded by the ALTERA SignalTap logic analyzer:



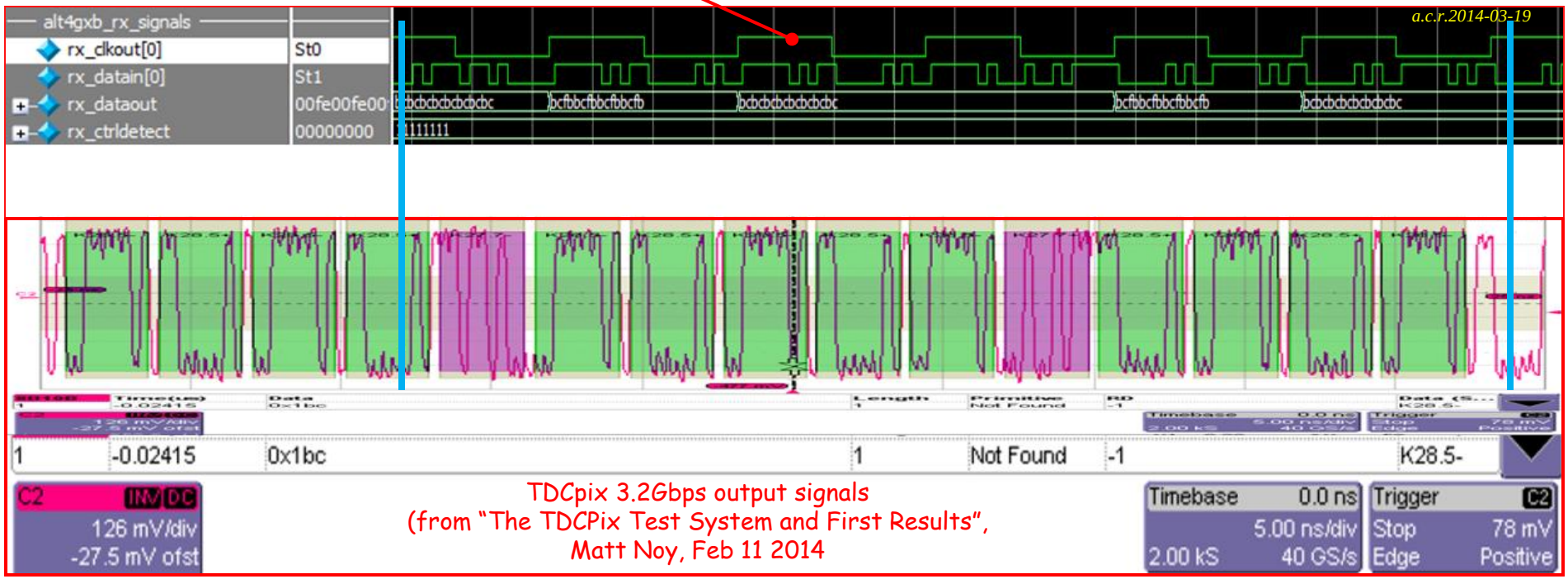


End of a UDP packet returning to the host PC echoes and replies from the TDCpix slow link

"off-detector" readout electronics for the Gigatracker (GTKRO): status update

- preparing for the test of interconnection to the TDCpix: high speed serial data link
- preparing for the test of interconnection to the TDCpix: configuration link
- GTKRO motherboard production

GTKRO simulation of 3.2Gbps signals



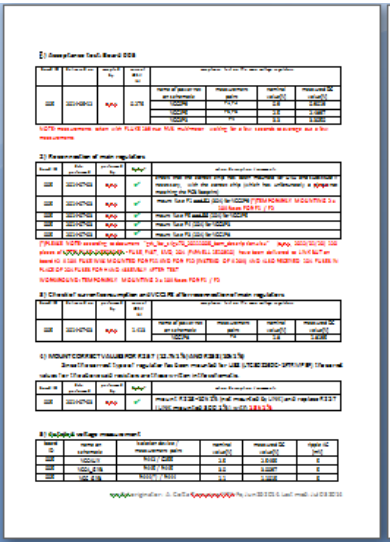
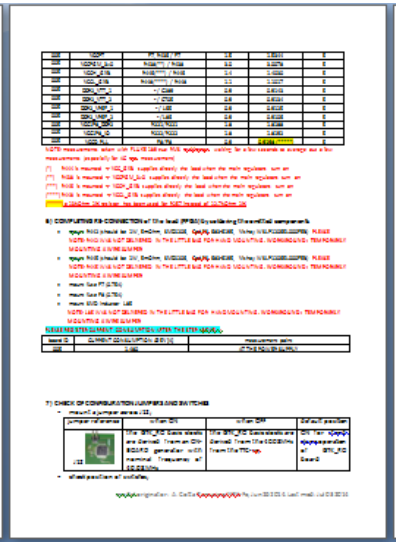
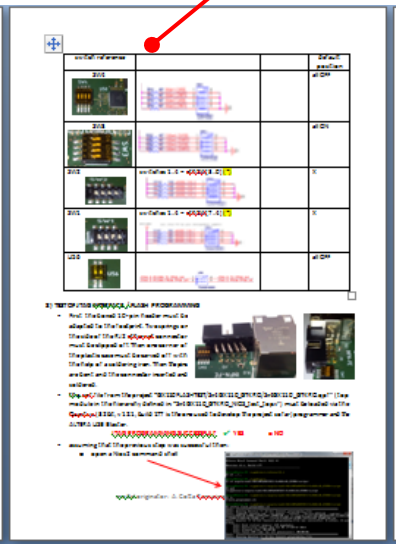
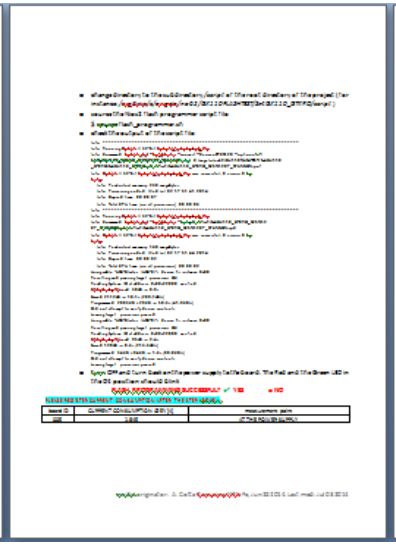
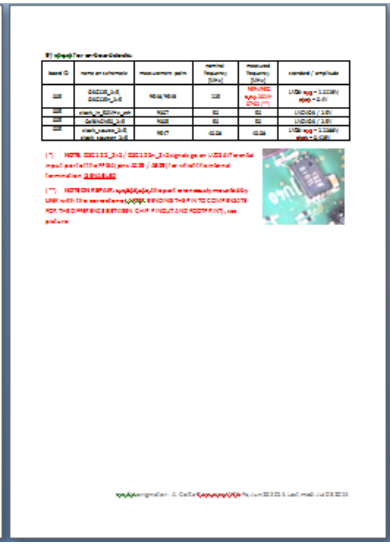
TDCpix 3.2Gbps output signals
(from "The TDCPix Test System and First Results",
Matt Noy, Feb 11 2014

The simulated data pattern matches the pattern (idle characters) published by Matt.

- GTKRO motherboard production

- 6 boards received on 2014-06-12 and tested (5 accepted)
- 10 boards delivered today
- remaining 18 boards to be delivered by 3rd week of September

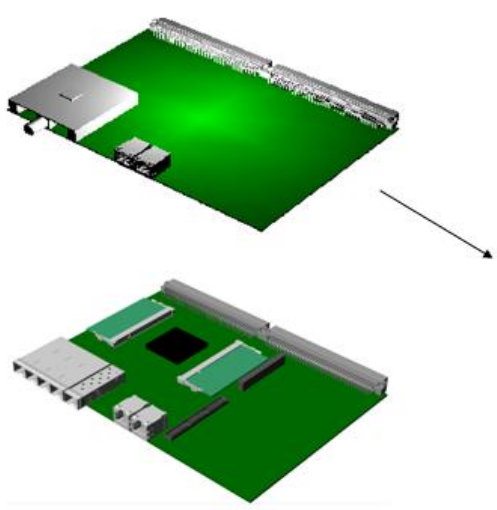
GTTRO motherboard test sheet

- TTCINT / GTKTTC daughter card production

- at an advanced layout stage
- stuffed boards expected by beginning of October
- details in Stefano's presentation

Update on TTC interface card and timing generator



GTK_RO main board

TTCINT / GTKTTC interface

Final PCB placement (01/08/2014)

Stefano Chiozzi – INFN sez. Ferrara

GTK working group meeting 02/09/2014